

To our customers,

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## Old Company Name in Catalogs and Other Documents

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Renesas Electronics website: <http://www.renesas.com>

April 1<sup>st</sup>, 2010  
Renesas Electronics Corporation

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# **Phase-out/Discontinued**

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P1 98.2

MOS FIELD EFFECT POWER TRANSISTOR  
**2SK1992/2SK1993**

**Phase-out/Discontinued**

SWITCHING  
 N-CANNEL POWER MOS FET  
 INDUSTRIAL USE

**DESCRIPTION**

The 2SK1992/2SK1993 is N-channel MOS Field Effect Transistor designed for high voltage switching applications.

**FEATURES**

- Low On-state Resistance  
 $R_{DS(on)} \leq 0.9/1.0 \Omega$  ( $V_{GS} = 10 V, I_D = 3.0 A$ )
- Low  $C_{iss}$   $C_{iss} = 1\ 060\ pF$  TYP.
- Built-in G-S Gate Protection Diode
- High Avalanche Capability Ratings

**QUALITY GRADE**

Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

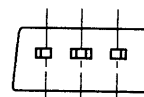
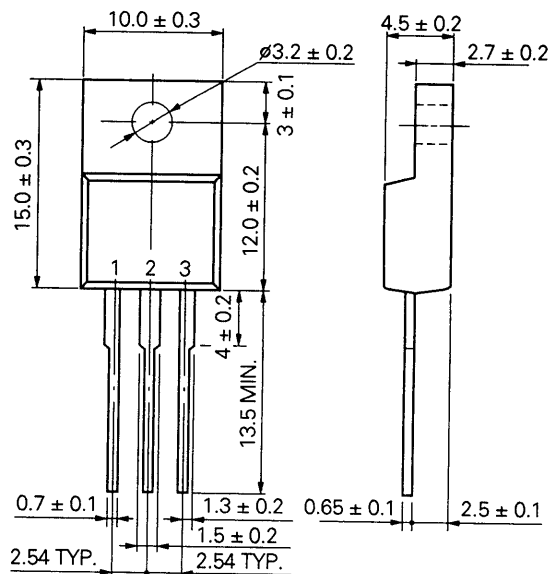
**ABSOLUTE MAXIMUM RATINGS ( $T_a = 25\ ^\circ C$ )**

Drain to Source Voltage	$V_{DSS}$	450/500	V
Gate to Source Voltage	$V_{GSS}$	$\pm 30$	V
Drain Current (DC)	$I_{D(DC)}$	$\pm 6.0$	A
Drain Current (pulse)	$I_{D(pulse)^*}$	$\pm 24$	A
Total Power Dissipation ( $T_C = 25\ ^\circ C$ )	$P_{T1}$	35	W
Total Power Dissipation ( $T_a = 25\ ^\circ C$ )	$P_{T2}$	2.0	W
Channel Temperature	$T_{ch}$	150	$^\circ C$
Storage Temperature	$T_{stg}$	-55 to +150	$^\circ C$
Single Avalanche Current	$I_{AS}^{**}$	9.0	A
Single Avalanche Energy	$E_{AS}^{**}$	243	mJ

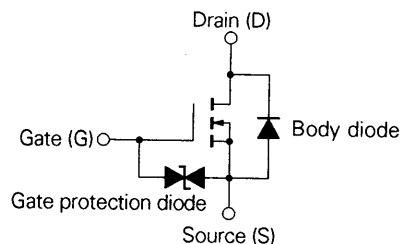
\*  $PW \leq 10\ \mu s$ , Duty Cycle  $\leq 1\ %$

\*\* Starting  $T_{ch} = 25\ ^\circ C$ ,  $R_G = 25\ \Omega$ ,  $V_{GS} = 20\ V \rightarrow 0$

**PACKAGE DIMENSIONS**  
 (in millimeters)



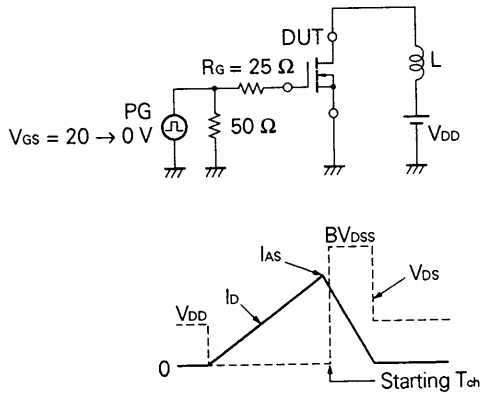
- 1. Gate
- 2. Drain
- 3. Source



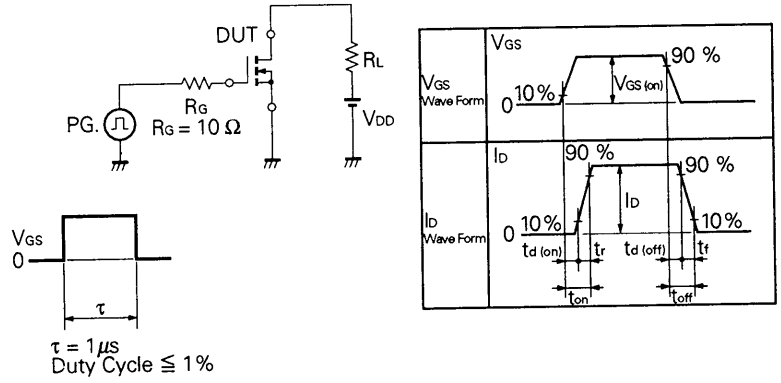
**ELECTRICAL CHARACTERISTICS (T<sub>a</sub> = 25 °C)**

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Drain to Source On-state Resistance (2SK1992)	R <sub>DS(on)</sub>		0.7	0.9	Ω	V <sub>GS</sub> = 10 V, I <sub>b</sub> = 3.0 A
Drain to Source On-state Resistance (2SK1993)			0.8	1.0	Ω	V <sub>GS</sub> = 10 V, I <sub>b</sub> = 3.0 A
Gate to Source Cutoff Voltage	V <sub>GS(off)</sub>	2.5		3.5	V	V <sub>DS</sub> = 10 V, I <sub>b</sub> = 1 mA
Forward Transfer Admittance	y <sub>fs</sub>	2.8			S	V <sub>DS</sub> = 10 V, I <sub>b</sub> = 3.0 A
Drain Leakage Current (2SK1992/1993)	I <sub>DSS</sub>			100	μA	V <sub>DS</sub> = 450/500 V, V <sub>GS</sub> = 0
Gate to Source Leakage Current	I <sub>GSS</sub>			±10	μA	V <sub>GS</sub> = ±30 V, V <sub>DS</sub> = 0
Input Capacitance	C <sub>iss</sub>		1 060		pF	V <sub>DS</sub> = 10 V
Output Capacitance	C <sub>oss</sub>		340		pF	V <sub>GS</sub> = 0
Reverse Transfer Capacitance	C <sub>res</sub>		150		pF	f = 1 MHz
Turn-On Delay Time	t <sub>d(on)</sub>		20		ns	V <sub>GS</sub> = 10 V V <sub>DD</sub> = 150 V I <sub>b</sub> = 3.0 A, R <sub>G</sub> = 10 Ω R <sub>L</sub> = 50 Ω
Rise Time	t <sub>r</sub>		30		ns	
Turn-Off Delay Time	t <sub>d(off)</sub>		70		ns	
Fall Time	t <sub>f</sub>		20		ns	
Total Gate Charge	Q <sub>G</sub>		36		nC	V <sub>GS</sub> = 10 V I <sub>b</sub> = 6 A V <sub>DD</sub> = 400 V
Gate to Source Charge	Q <sub>GS</sub>		7		nC	
Gate to Drain Charge	Q <sub>GD</sub>		21		nC	
Diode Forward Voltage	V <sub>F(S-D)</sub>		0.9		V	I <sub>F</sub> = 6 A, V <sub>GS</sub> = 0
Reverse Recovery Time	t <sub>rr</sub>		420		ns	I <sub>F</sub> = 6 A di/dt = 50 A/μs
Reverse Recovery Charge	Q <sub>rr</sub>		2.0		μC	

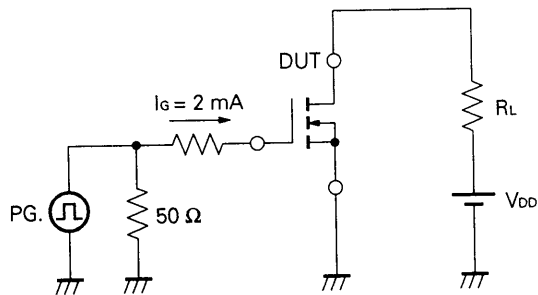
**Test Circuit 1: Avalanche Capability**



**Test Circuit 2: Switching Time**

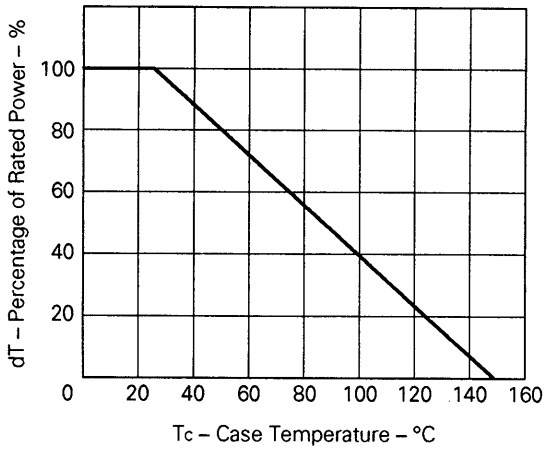


**Test Circuit 3: Gate Charge**

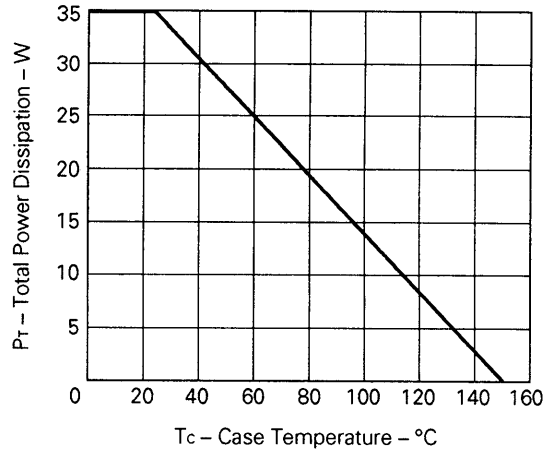


**TYPICAL CHARACTERISTICS (T<sub>a</sub> = 25 °C)**

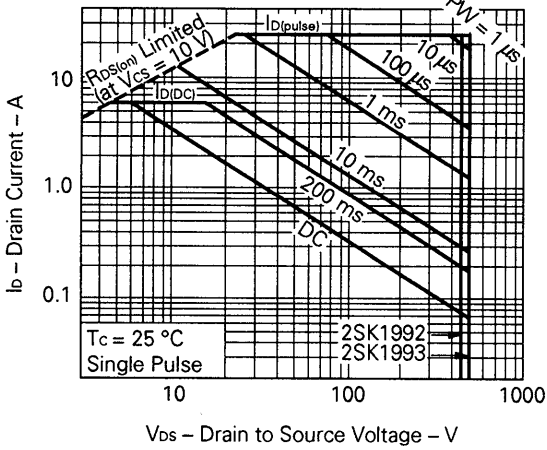
**DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA**



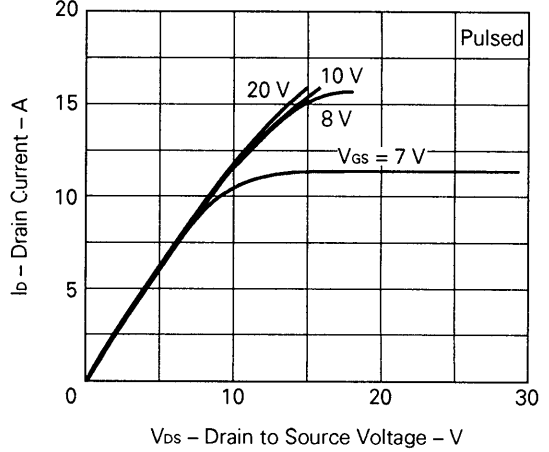
**TOTAL POWER DISSIPATION vs. CASE TEMPERATURE**



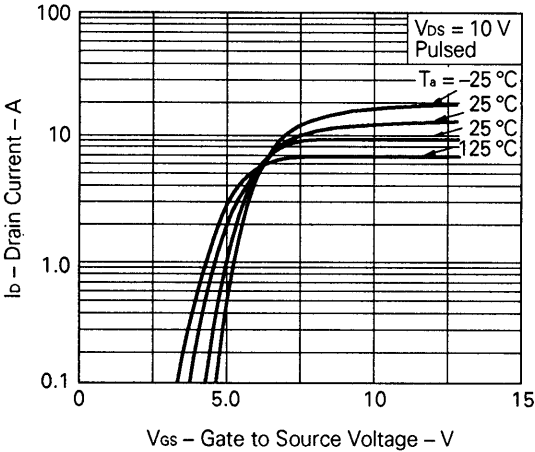
**FORWARD BIAS SAFE OPERATING AREA**



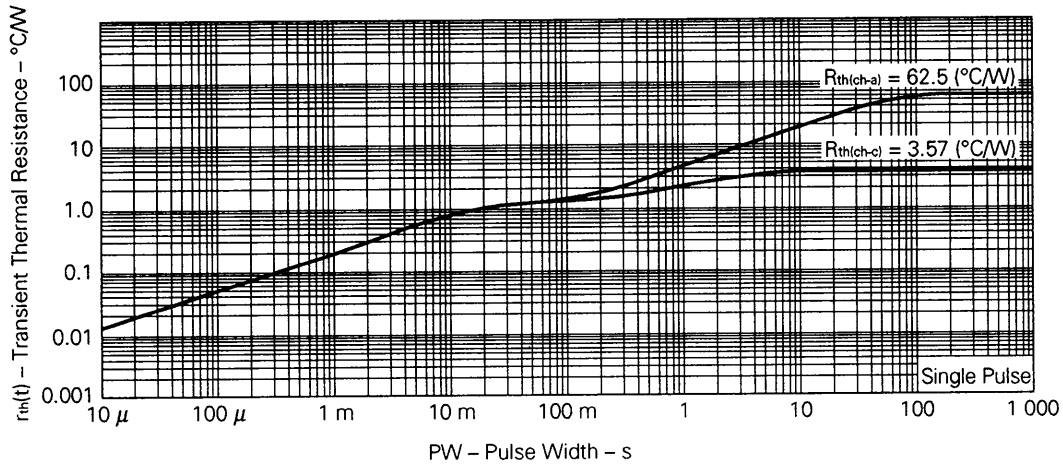
**DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE**



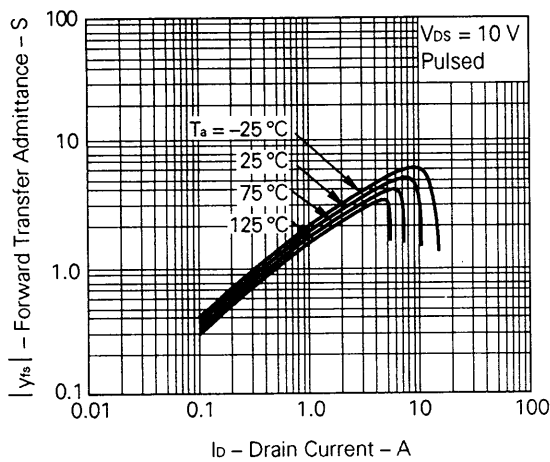
**TRANSFER CHARACTERISTICS**



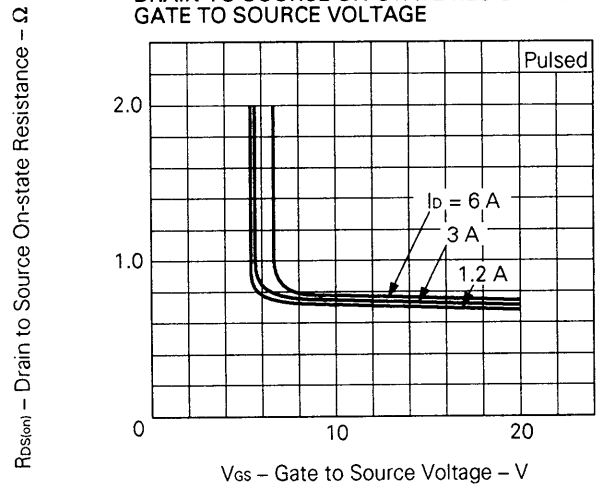
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



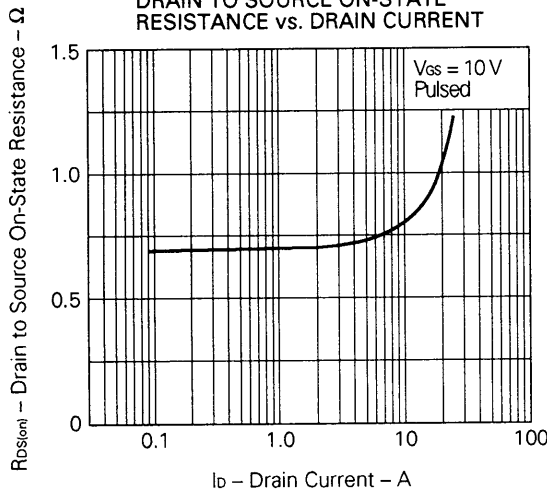
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



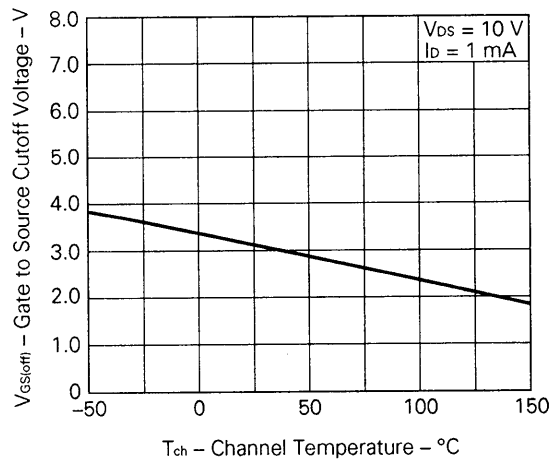
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



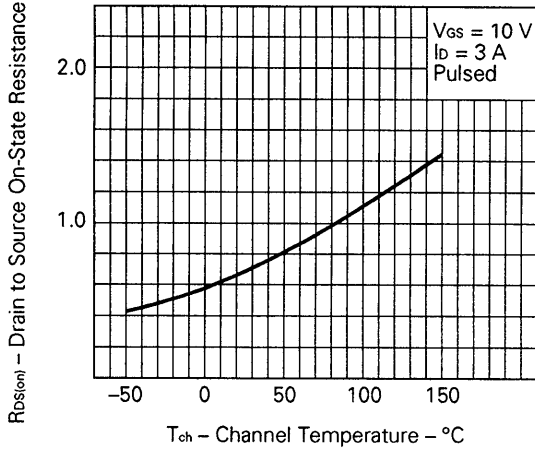
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



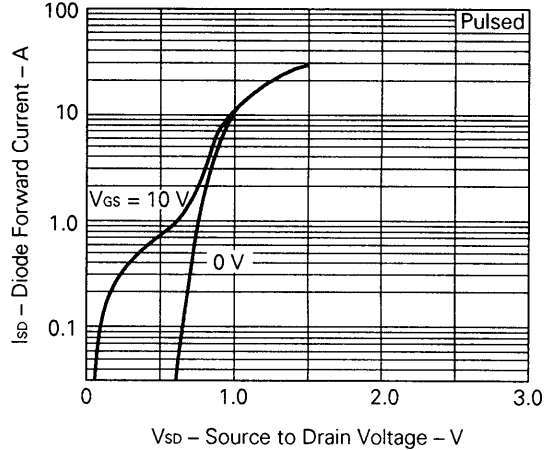
GATE TO SOURCE CUTOFF VOLTAGE vs. CHANNEL TEMPERATURE



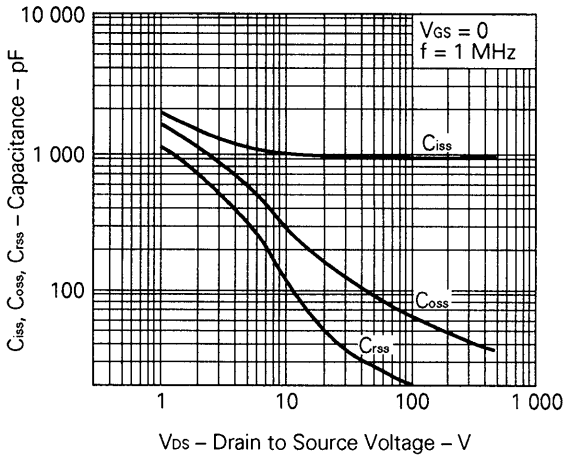
**DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE**



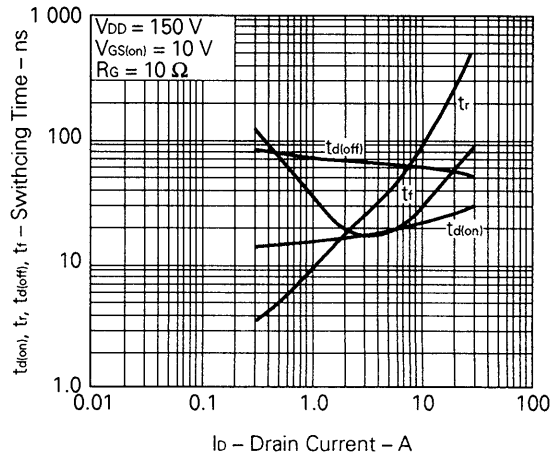
**SOURCE TO DRAIN DIODE FORWARD VOLTAGE**



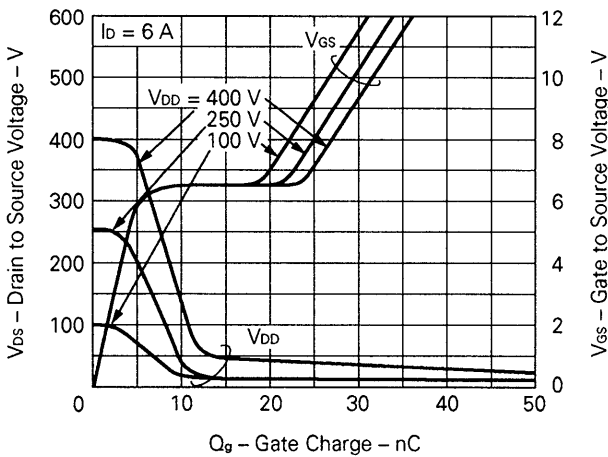
**CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE**



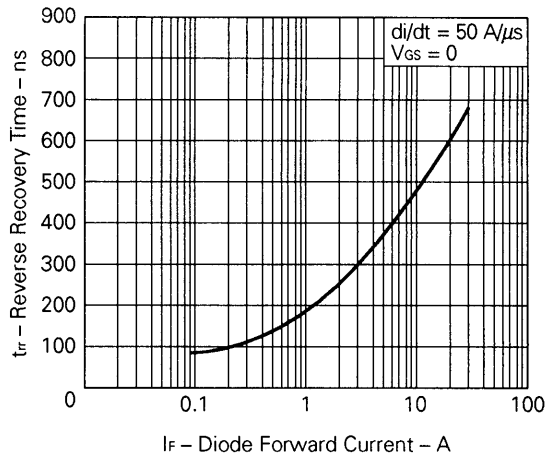
**SWITCHING CHARACTERISTICS**



**DYNAMIC INPUT CHARACTERISTICS**

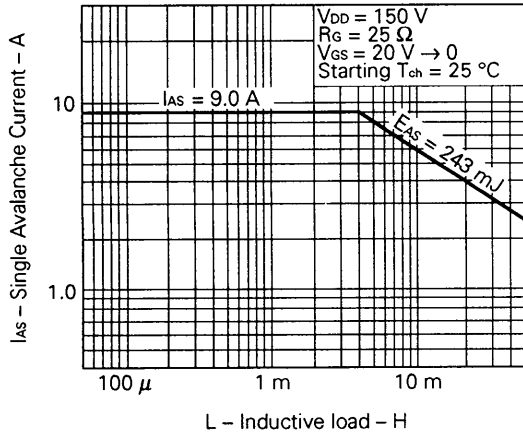


**REVERSE RECOVERY TIME vs. DIODE FORWARD CURRENT**

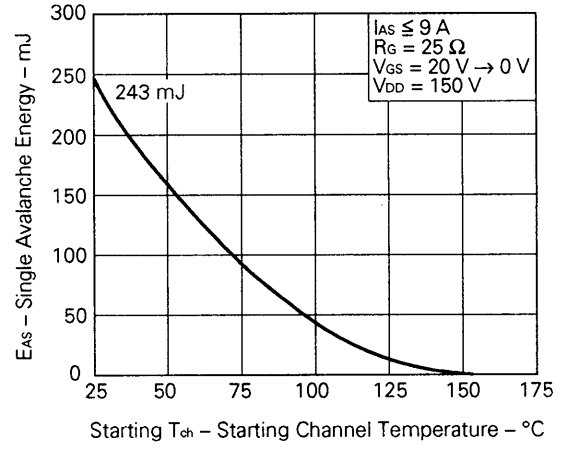




SINGLE AVALANCHE CURRENT vs. INDUCTIVE LOAD



SINGLE AVALANCHE ENERGY vs. STARTING CHANNEL TEMPERATURE



**Reference**

Application note name	No.
Safe operating area of Power MOS FET.	TEA-1034
Application circuit using Power MOS FET.	TEA-1035
Quality control of NEC semiconductors devices.	TEI-1202
Quality control guide of semiconductors devices.	MEI-1202
Assembly manual of semiconductors devices.	IEI-1207

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