To our customers,

Old Company Name in Catalogs and Other Documents

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Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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DATA SHEET

MOS FIELD EFFECT POWER TRANSISTOR
2SK1988, 1989

Phase-out/Discontinued

SWITCHING
N-CHANNEL POWER MOS FET
INDUSTRIAL USE

DESCRIPTION

The 2SK1988, 1989 is N-channel MOS Field Effect Transistor designed for high voltage switching applications.

FEATURES

- Low On-state Resistance
  - 2SK1988 $R_{DS(on)}$ = 2.8 Ω MAX. (V_{GS} = 10 V, I_D = 1.5 A)
  - 2SK1989 $R_{DS(on)}$ = 3.0 Ω MAX. (V_{GS} = 10 V, I_D = 1.5 A)
- Low C_{iss} C_{iss} = 350 pF TYP.
- Built-in G-S Gate Protection Diode
- High Avalanche Capability Ratings

QUALITY GRADE

Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

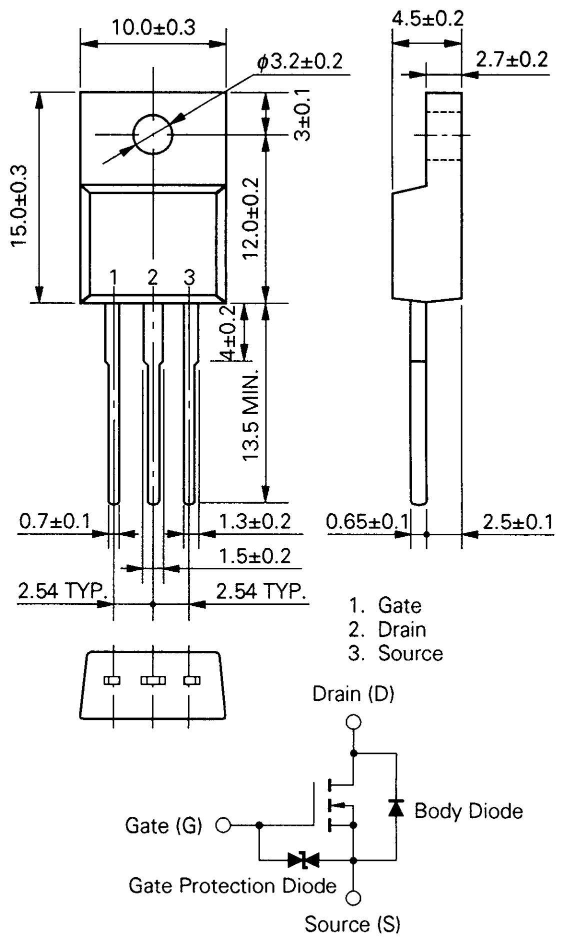
ABSOLUTE MAXIMUM RATINGS (T_a = 25°C)

Drain to Source Voltage	V_{DSS}	450/500	V
Gate to Source Voltage	V_{GSS}	±30	V
Drain Current (DC)	$I_{D(DC)}$	±2.5	A
Drain Current (pulse)	$I_{D(pulse)}$*	±10	A
Single Avalanche Current	I_{AS}	3.75	A
Single Avalanche Energy	E_{AS}	73.8	mJ
Total Power Dissipation (T_c = 25 °C)	P_{T1}	30	W
Total Power Dissipation (T_a = 25 °C)	P_{T2}	2.0	W
Channel Temperature	T_{ch}	150	°C
Storage Temperature	T_{stg}	–55 to +150	°C

* PW ≦ 10 μs, Duty Cycle ≦ 1 %

** Starting T_{ch} = 25 °C, R_G = 25 Ω, V_{GS} = 20 V → 0

PACKAGE DIMENSIONS
(in millimeters)



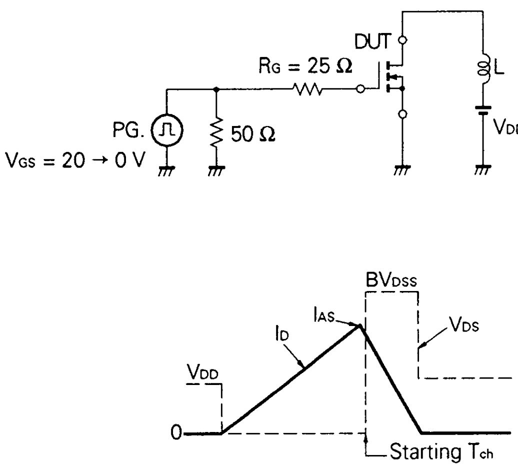
Document No. TC–2449
(O.D. No. TC–7912)
Date Published August 1993 M
Printed in Japan

Phase-out/Discontinued

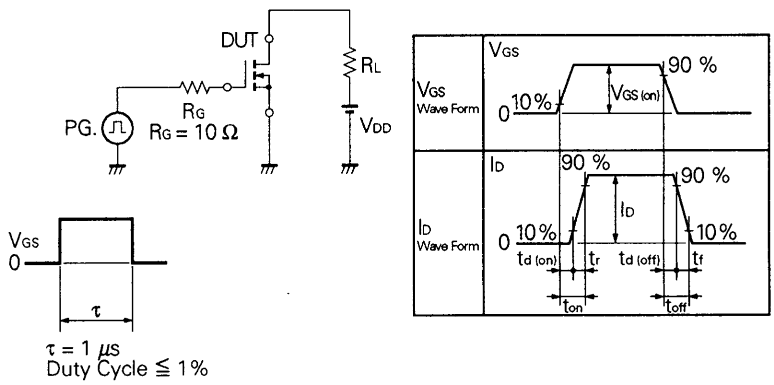
ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Drain to Source On-state Resistance (2SK1988)	$R_{DS(on)}$		2.2	2.8	Ω	V_{GS} = 10 V, I_D = 1.5 A
Drain to Source On-state Resistance (2SK1989)	$R_{DS(on)}$		2.4	3.0	Ω	V_{GS} = 10 V, I_D = 1.5 A
Gate to Source Cutoff Voltage	$V_{GS(off)}$	2.5		3.5	V	V_{DS} = 10 V, I_D = 1 mA
Forward Transfer Admittance	$\|y_{fs}\|$	0.9			S	V_{DS} = 10 V, I_D = 1.5 A
Drain Leakage Current	I_{DSS}			100	μA	V_{DS} = 450/500 V, V_{GS} = 0
Gate to Source Leakage Current	I_{GSS}			±10	μA	V_{GS} = ±30 V, V_{DS} = 0
Input Capacitance	C_{iss}		350		pF	V_{DS} = 10 V V_{GS} = 0 f = 1 MHz
Output Capacitance	C_{oss}		120		pF	
Reverse Transfer Capacitance	C_{rss}		45		pF	
Turn-On Delay Time	$t_{d(on)}$		10		ns	V_{GS} = 10 V V_{DD} = 150 V I_D = 1.5 A, R_G = 10 Ω R_L = 100 Ω
Rise Time	t_r		10		ns	
Turn-Off Delay Time	$t_{d(off)}$		30		ns	
Fall Time	t_f		10		ns	
Total Gate Charge	Q_G		12		nC	V_{GS} = 10 V I_D = 2.5 A V_{DD} = 400 V
Gate to Source Charge	Q_{GS}		3.0		nC	
Gate to Drain Charge	Q_{GD}		7.0		nC	
Diode Forward Voltage	$V_{F(S-D)}$		0.9		V	I_F = 2.5 A, V_{GS} = 0
Reverse Recovery Time	t_{rr}		310		ns	I_F = 2.5 A di/dt = 50 A/μs
Reverse Recovery Charge	Q_{rr}		1.2		μC	

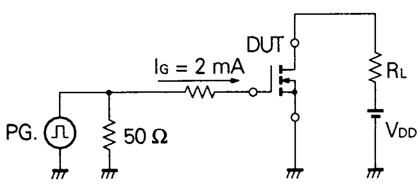
Test Circuit 1: Avalanche Capability



Test Circuit 2: Switching Time

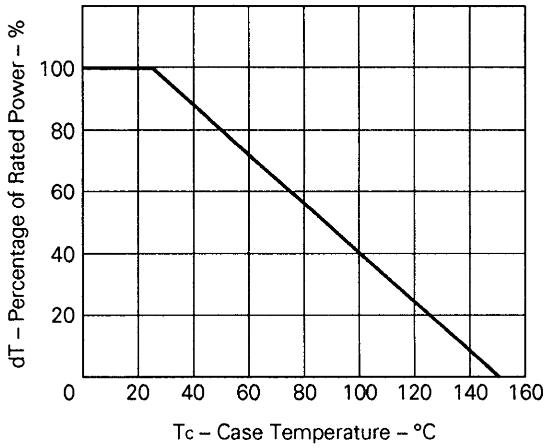


Test Circuit 3: Gate Charge

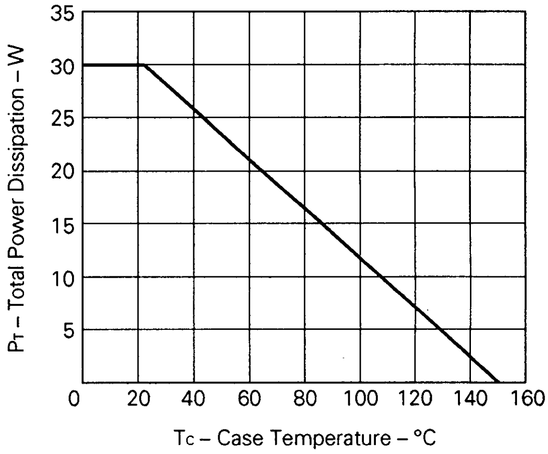


TYPICAL CHARACTERISTICS (T_a = 25 °C)

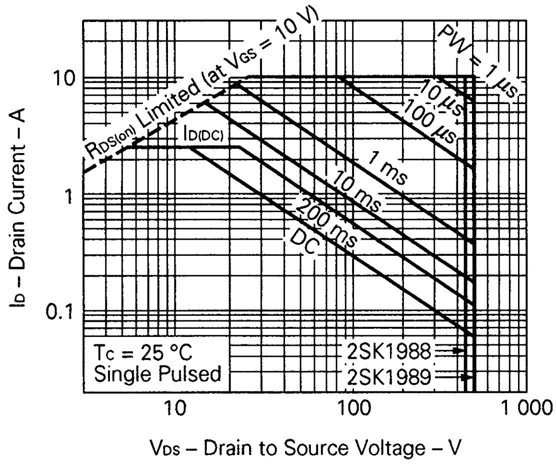
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



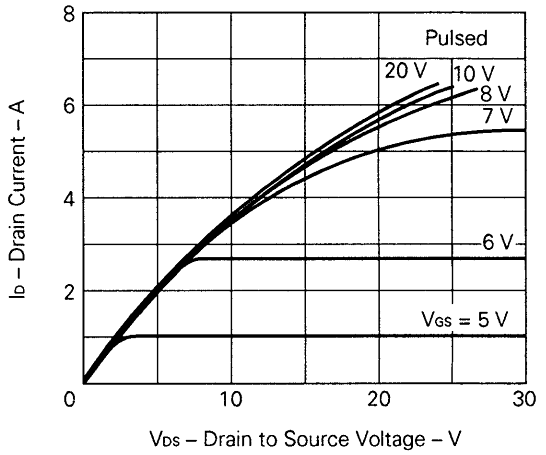
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



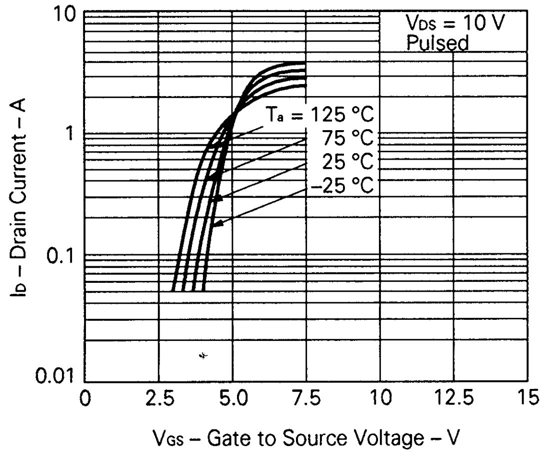
FORWARD BIAS SAFE OPERATING AREA



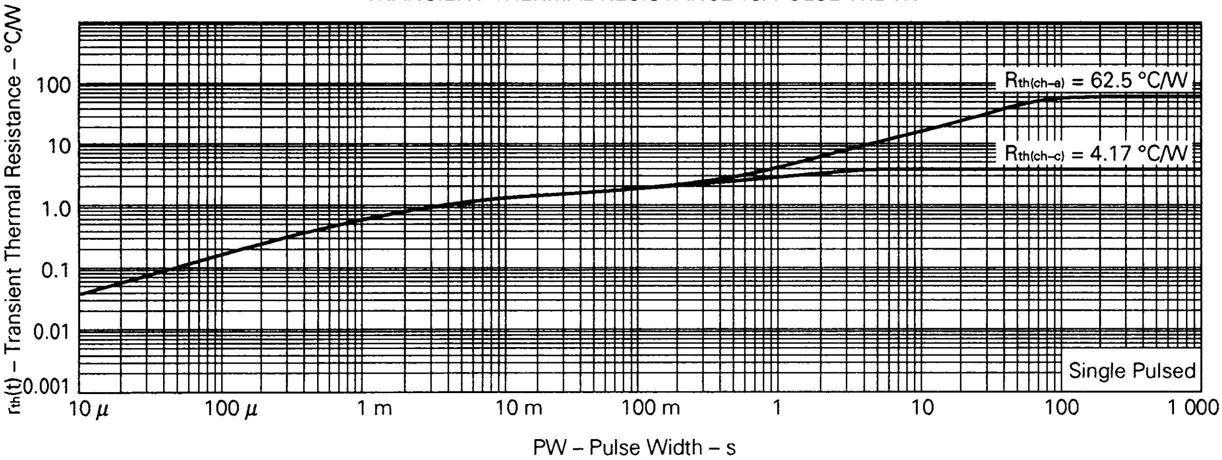
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



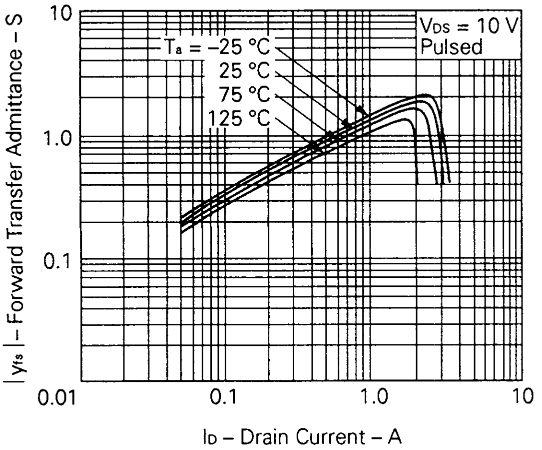
TRANSFER CHARACTERISTICS



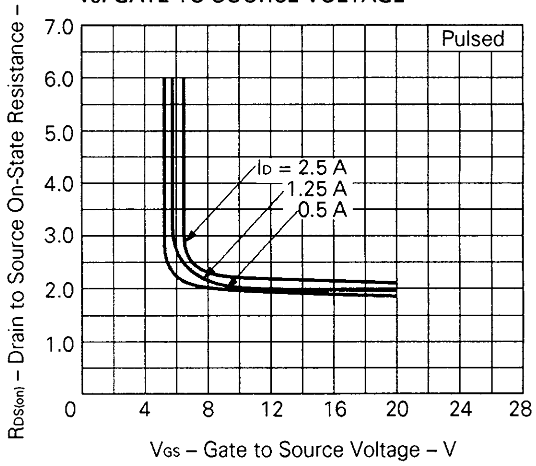
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



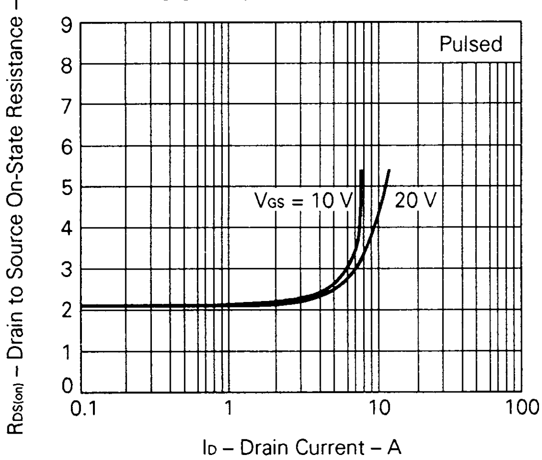
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



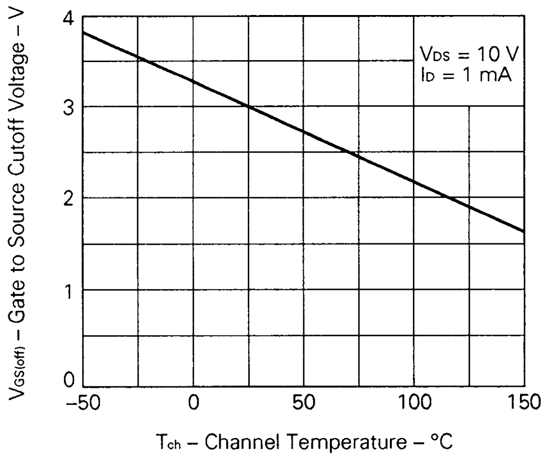
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

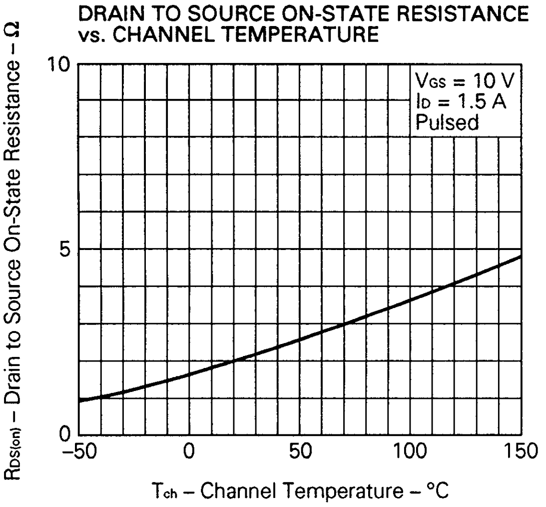


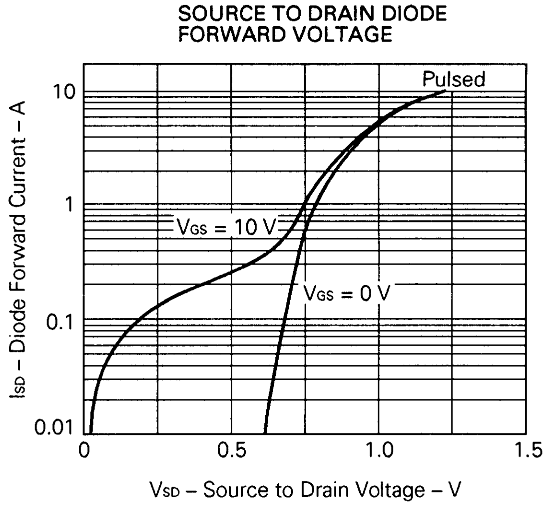
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT

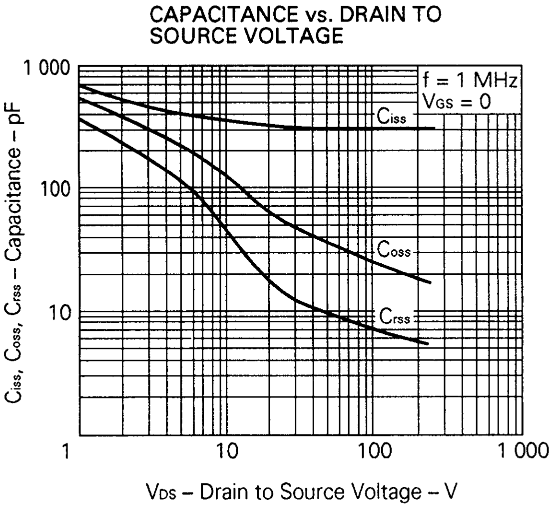


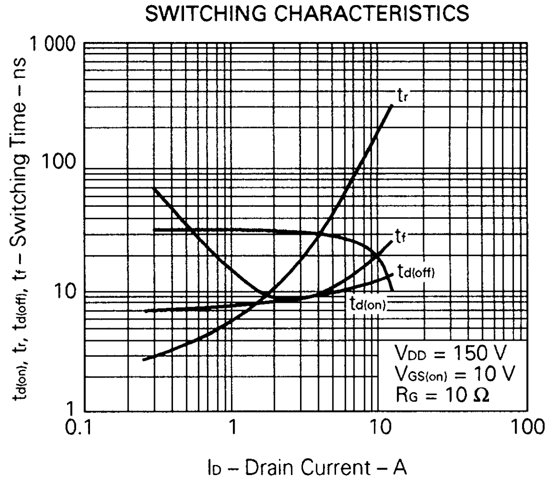
GATE TO SOURCE CUTOFF VOLTAGE vs. CHANNEL TEMPERATURE

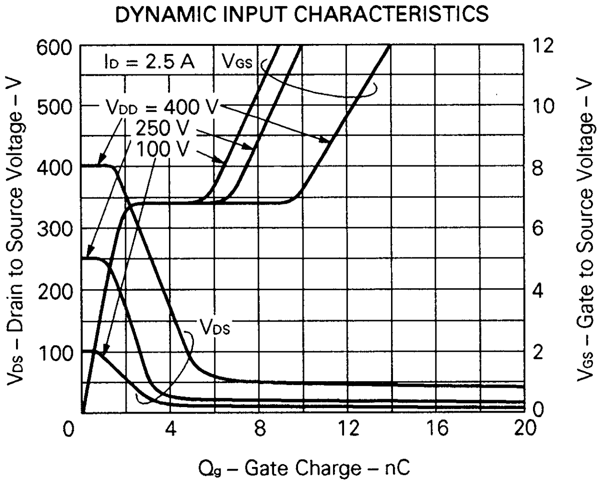


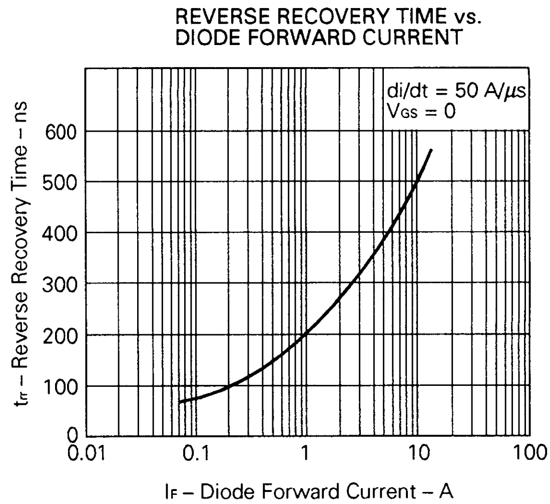

DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE
VGS = 10 V
ID = 1.5 A
Pulsed
RDS(on) – Drain to Source On-State Resistance – Ω
Tch – Channel Temperature – °C


SOURCE TO DRAIN DIODE FORWARD VOLTAGE
Pulsed
VGS = 10 V
VGS = 0 V
ISD – Diode Forward Current – A
VSD – Source to Drain Voltage – V

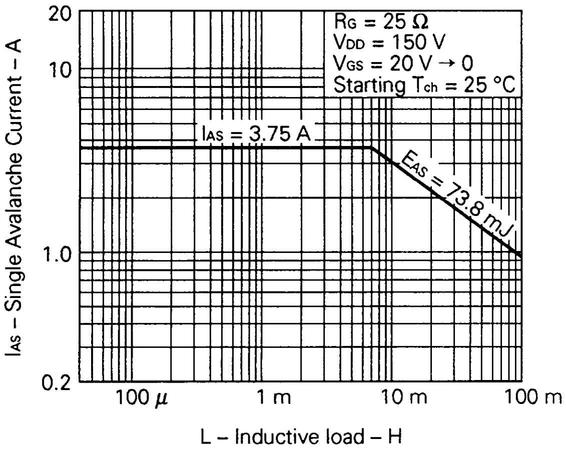

CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE
f = 1 MHz
VGS = 0
Ciss
Coss
Crss
Ciss, Coss, Crss – Capacitance – pF
VDS – Drain to Source Voltage – V


SWITCHING CHARACTERISTICS
tr
tf
td(off)
td(on)
VDD = 150 V
VGS(on) = 10 V
RG = 10 Ω
td(on), tr, td(off), tf – Switching Time – ns
ID – Drain Current – A

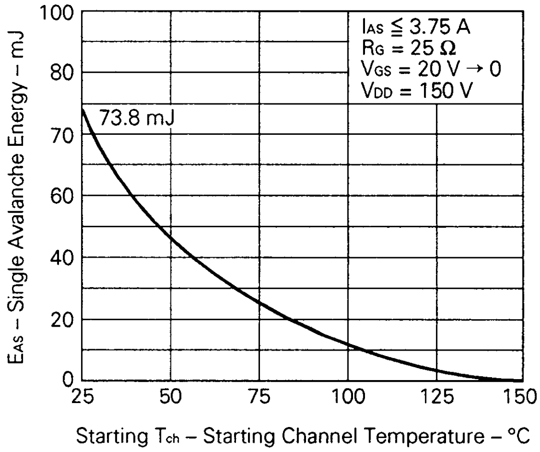

DYNAMIC INPUT CHARACTERISTICS
ID = 2.5 A
VGS
VDD = 400 V
250 V
100 V
VDS
VDS – Drain to Source Voltage – V
VGS – Gate to Source Voltage – V
Qg – Gate Charge – nC


REVERSE RECOVERY TIME vs. DIODE FORWARD CURRENT
di/dt = 50 A/μs
VGS = 0
trr – Reverse Recovery Time – ns
IF – Diode Forward Current – A

SINGLE AVALANCHE CURRENT vs. INDUCTIVE LOAD



SINGLE AVALANCHE ENERGY vs. STARTING CHANNEL TEMPERATURE



Reference

Application note name	No.
Safe operating area of Power MOS FET.	TEA-1034
Application circuit using Power MOS FET.	TEA-1035
Quality control of NEC semiconductors devices.	TEI-1202
Quality control guide of semiconductors devices.	MEI-1202
Assembly manual of semiconductors devices.	IEI-1207

[MEMO]

M4 92.6