

To our customers,

Old Company Name in Catalogs and Other Documents

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Renesas Electronics website: <http://www.renesas.com>

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

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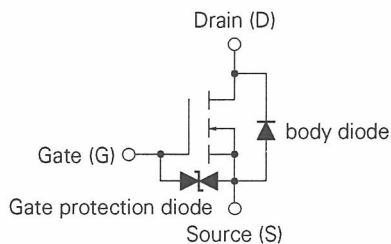
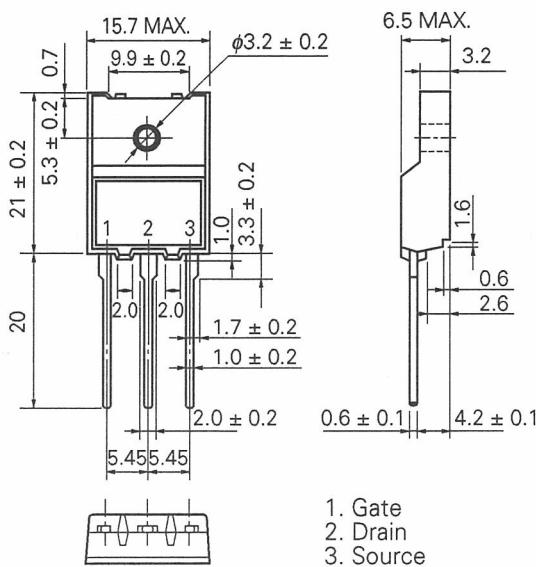
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RENESAS
N-CHANNEL MOS FIELD EFFECT POWER TRANSISTOR
Phase-out/Discontinued
2SK1149

SWITCHING
N-CHANNEL POWER MOS FET
INDUSTRIAL USE

PACKAGE DIMENSIONS
(in millimeters)


DESCRIPTION

The 2SK1149 is N-channel MOS Field Effect Transistor designed for solenoid, motor and lamp driver.

FEATURES

- Low On-state Resistance
 $R_{DS(on)} \leq 50 \text{ m}\Omega \text{ MAX. (} V_{GS} = 10 \text{ V, } I_D = 20 \text{ A)}$
 $R_{DS(on)} \leq 70 \text{ m}\Omega \text{ MAX. (} V_{GS} = 4 \text{ V, } I_D = 20 \text{ A)}$
- Low C_{iss} $C_{iss} = 3\,300 \text{ pF TYP.}$
- Built-in G-S Gate Protection Diodes

QUALITY GRADE
Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

ABSOLUTE MAXIMUM RATINGS
Maximum Temperatures

Storage Temperature	-55 to +150 °C
Channel Temperature	150 MAX. °C

Maximum Power Dissipation

Total Power Dissipation ($T_a = 25 \text{ °C}$)	3.5	W
Total Power Dissipation ($T_c = 25 \text{ °C}$)	75	W

Maximum Voltages and Currents ($T_a = 25 \text{ °C}$)

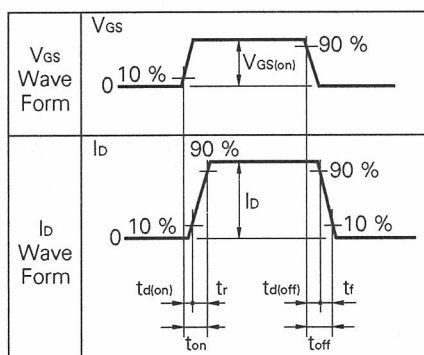
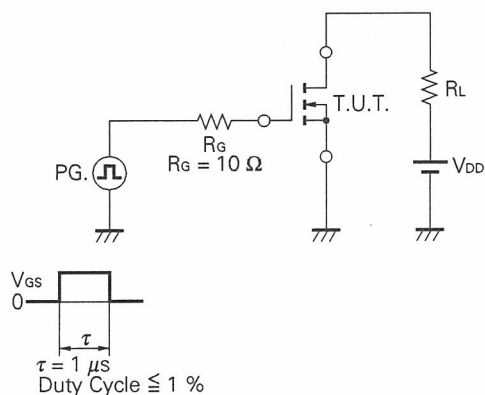
V_{DSS}	Drain to Source Voltage	100	V
$V_{GSS(AC)}$	Gate to Source Voltage	±20	V
$I_D(DC)$	Drain Current (DC)	±40	A
$I_D(pulse)^*$	Drain Current (pulse)	±160	A

* $PW \leq 10 \text{ }\mu\text{s}$, Duty Cycle $\leq 1 \%$

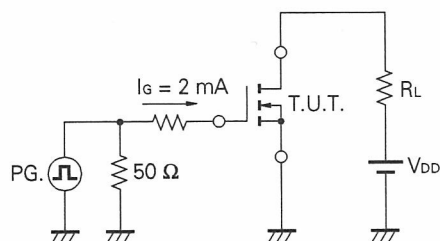
ELECTRICAL CHARACTERISTICS ($T_a = 25\text{ }^{\circ}\text{C}$)

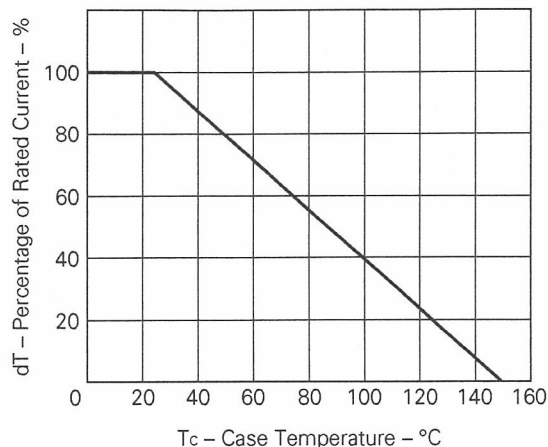
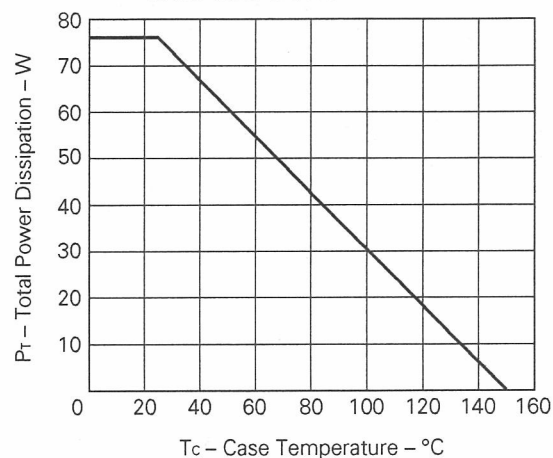
CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Drain to Source On-state Resistance	$R_{DS(on)}$		42	50	$\text{m}\Omega$	$V_{GS} = 10\text{ V}$, $I_D = 20\text{ A}$
Drain to Source On-state Resistance	$R_{DS(on)}$		50	70	$\text{m}\Omega$	$V_{GS} = 4.0\text{ V}$, $I_D = 20\text{ A}$
Gate to Source Cutoff Voltage	$V_{GS(off)}$	1.0		2.5	V	$V_{DS} = 10\text{ V}$, $I_D = 1\text{ mA}$
Forward Transfer Admittance	$ y_{fs} $	12			S	$V_{DS} = 10\text{ V}$, $I_D = 20\text{ A}$
Drain Leakage Current	I_{DSS}			10	μA	$V_{DS} = 100\text{ V}$, $V_{GS} = 0$
Gate to Source Leakage Current	I_{GSS}			± 10	μA	$V_{GS} = \pm 20\text{ V}$, $V_{DS} = 0$
Input Capacitance	C_{iss}		3 300		pF	$V_{DS} = 10\text{ V}$
Output Capacitance	C_{oss}		800		pF	$V_{GS} = 0$
Reverse Transfer Capacitance	C_{rss}		200		pF	$f = 1\text{ MHz}$
Turn-On Delay Time	$t_{d(on)}$		40		ns	$V_{GS(on)} = 10\text{ V}$ $V_{DD} = 50\text{ V}$ $I_D = 20\text{ A}$, $R_G = 10\text{ }\Omega$ $R_L = 2.5\text{ }\Omega$
Rise Time	t_r		210		ns	
Turn-Off Delay Time	$t_{d(off)}$		210		ns	
Fall Time	t_f		155		ns	
Total Gate Charge	Q_G		80		nC	$V_{GS} = 10\text{ V}$ $I_D = 40\text{ A}$ $V_{DD} = 80\text{ V}$
Gate to Source Charge	Q_{GS}		10		nC	
Gate to Drain Charge	Q_{GD}		30		nC	
Diode Forward Voltage	V_{SD}		1.2		V	$I_{SD} = 40\text{ A}$, $V_{GS} = 0$
Reverse Recovery Time	t_{rr}		210		ns	$I_F = 40\text{ A}$, $V_{GS} = 0$ $di/dt = 50\text{ A}/\mu\text{s}$
Reverse Recovery Charge	Q_{rr}		600		μC	

Test Circuit 1: Switching Time

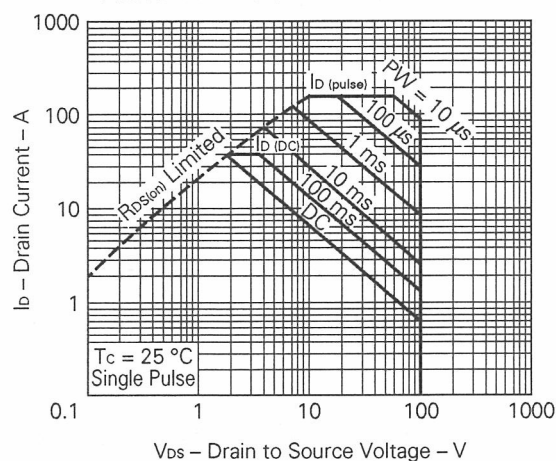
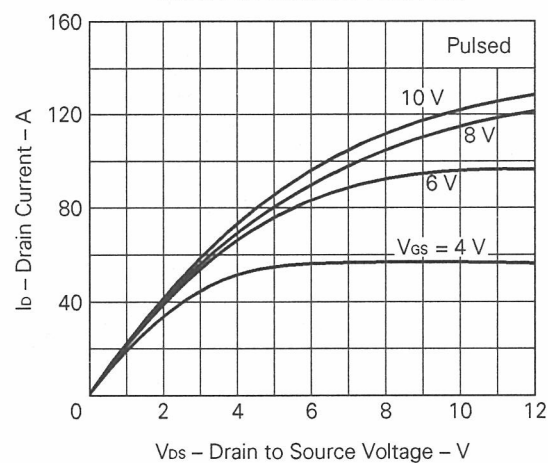


Test Circuit 2: Gate Charge

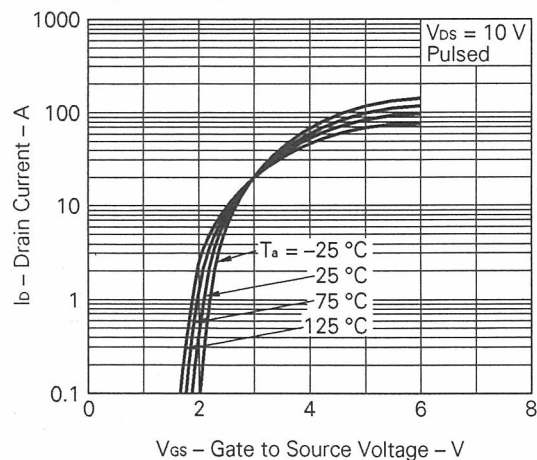


TYPICAL CHARACTERISTICS ($T_a = 25^\circ\text{C}$)DERATING FACTOR OF FORWARD BIAS
SAFE OPERATING AREATOTAL POWER DISSIPATION vs.
CASE TEMPERATURE

FORWARD BIAS SAFE OPERATING AREA

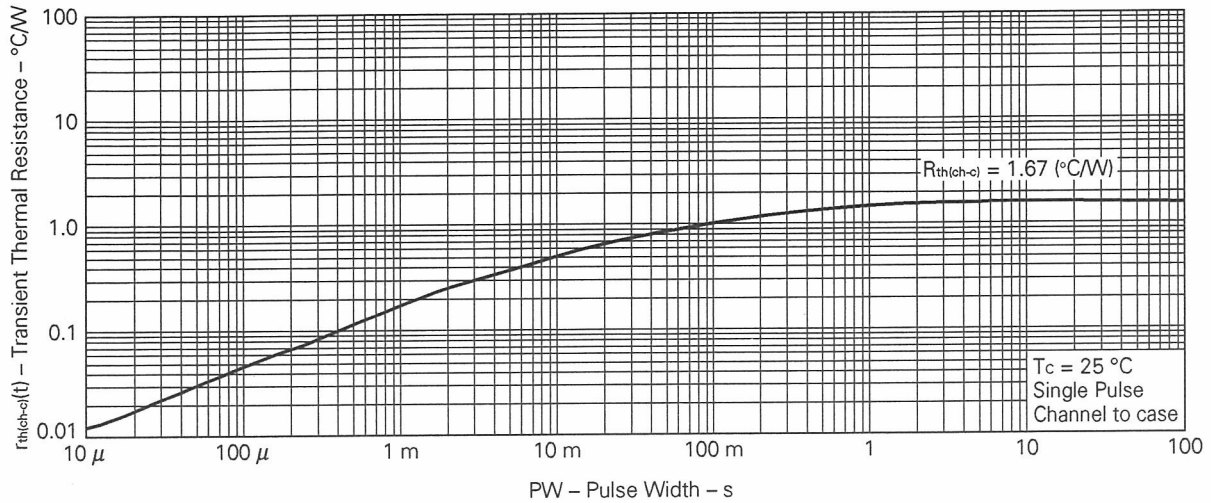
DRAIN CURRENT vs.
DRAIN TO SOURCE VOLTAGE

TRANSFER CHARACTERISTICS

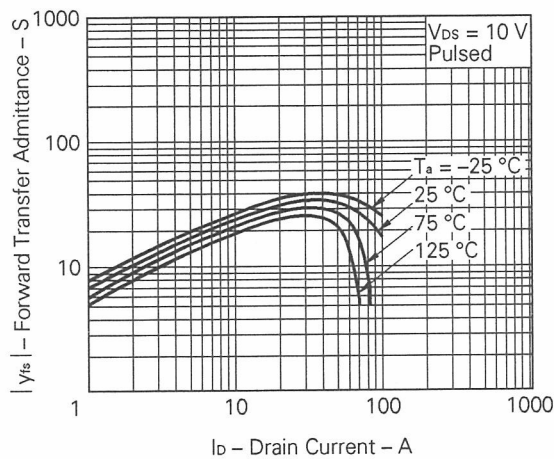


Phase-out/Discontinued

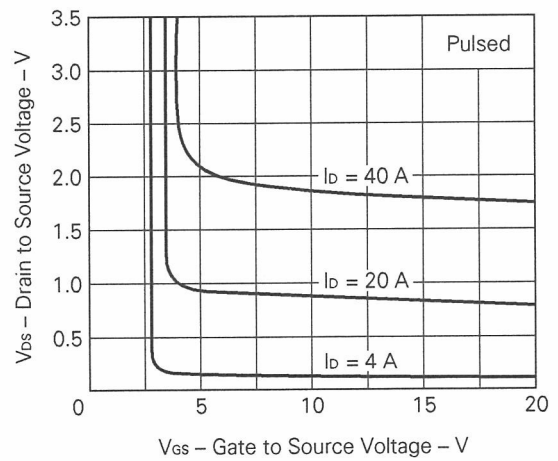
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



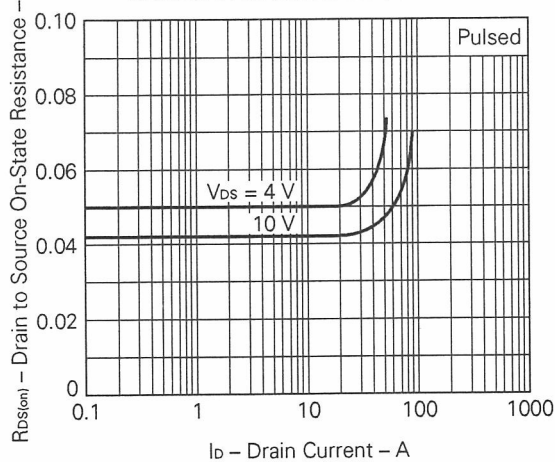
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



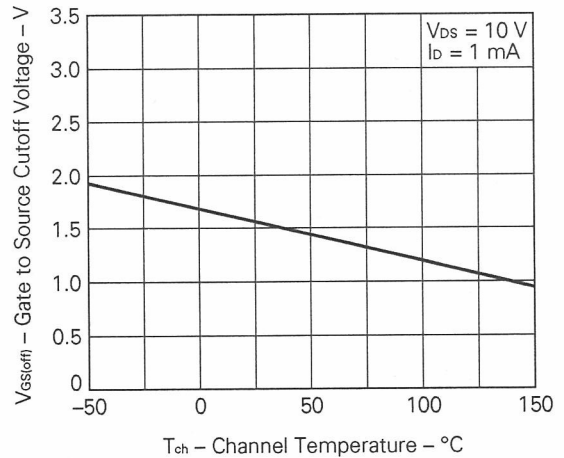
DRAIN TO SOURCE VOLTAGE vs. GATE TO SOURCE VOLTAGE

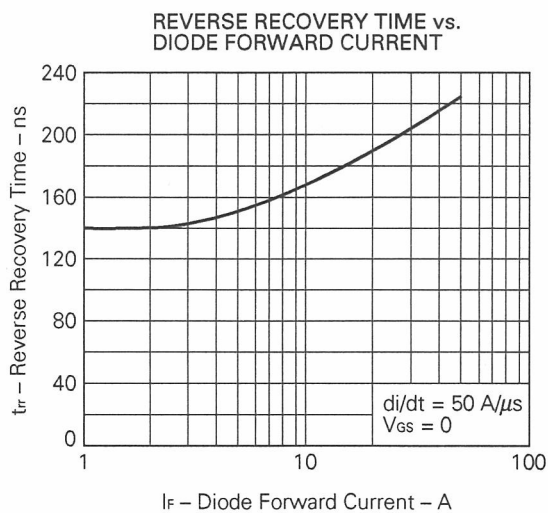
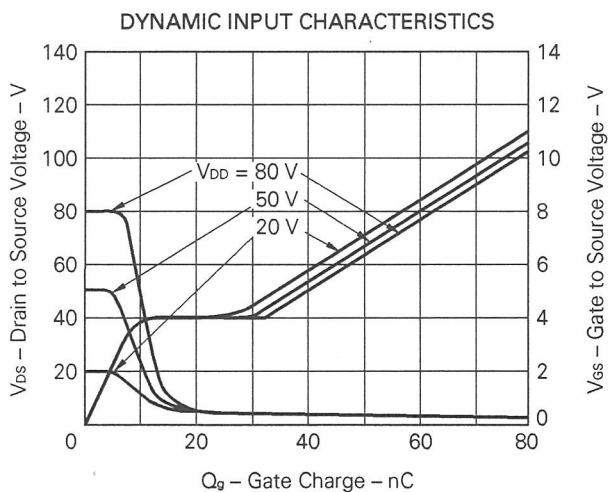
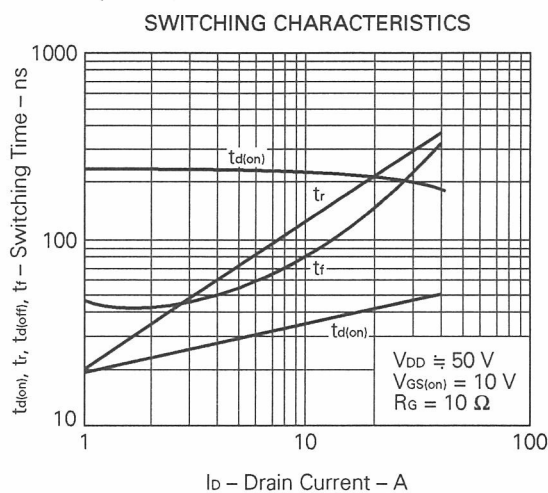
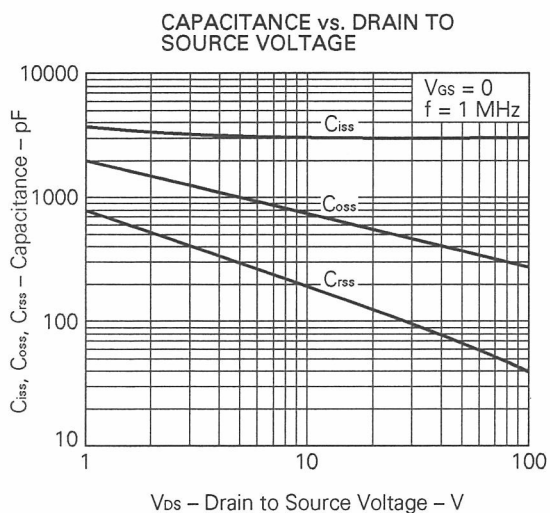
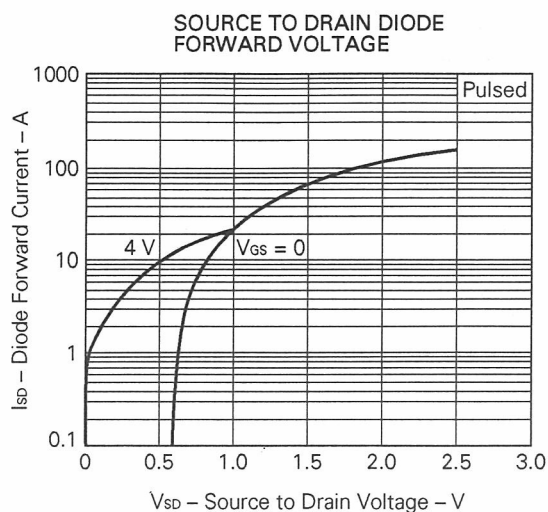
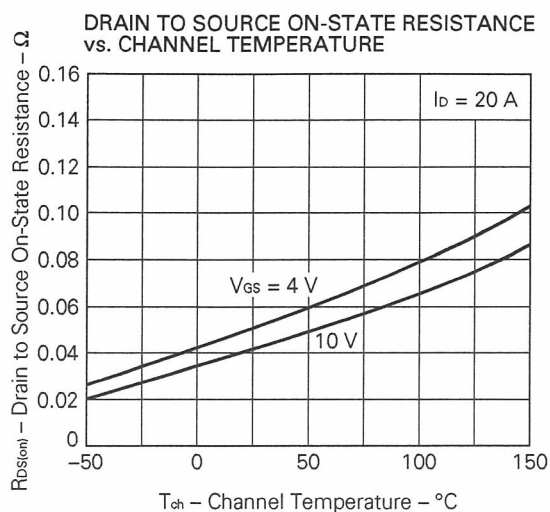


DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



GATE TO SOURCE CUTOFF VOLTAGE vs. CHANNEL TEMPERATURE





Reference

Application note name	No.
Safe operating area of Power MOS FET.	TEA-1034
Application circuit using Power MOS FET.	TEA-1035
Quality control of NEC semiconductors devices.	TEI-1202
Quality control guide of semiconductors devices.	MEI-1202
Assembly manual of semiconductors devices.	IEI-1207

Phase-out/Discontinued

[MEMO]

[MEMO]

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