To our customers,

Old Company Name in Catalogs and Other Documents

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Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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RENESAS

SILICON POWER TRANSISTOR

Phase-out/Discontinued

2SD2164

NPN SILICON EPITAXIAL TRANSISTOR
FOR LOW-FREQUENCY POWER AMPLIFIERS AND LOW-SPEED SWITCHING

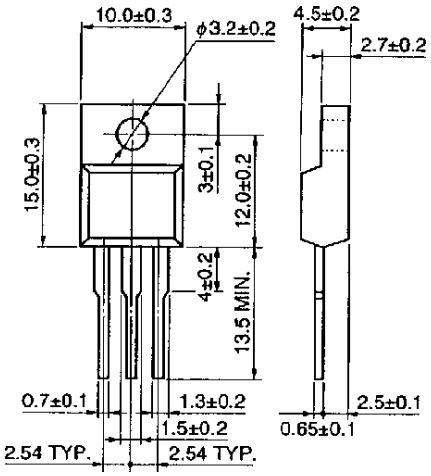
The 2SD2164 is a single power transistor developed especially for high h_{FE}. This transistor is ideal for simplifying drive circuits and reducing power dissipation because its h_{FE} is as high as that of Darlington transistors, but it is a single transistor.

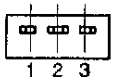
In addition, this transistor features a small resin insulated package, thus contributing to high-density mounting and mounting cost reduction.

FEATURES

- High h_{FE} and low $V_{CE(sat)}$:
  $h_{FE} \cong$ 1,300 TYP. (V_{CE} = 5.0 V, I_C = 0.5 A)
  $V_{CE(SAT)} \cong$ 0.3 V TYP. (I_C = 2.0 A, I_B = 20 mA)
- Full mold package that does not require an insulating board or insulation bushing

PACKAGE DRAWING (UNIT: mm)





Electrode Connection
1. Base
2. Collector
3. Emitter

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

Parameter	Symbol	Ratings	Unit
Collector to base voltage	V_{CBO}	60	V
Collector to emitter voltage	V_{CEO}	60	V
Emitter to base voltage	V_{EBO}	7.0	V
Collector current (DC)	$I_{C(DC)}$	3.0	A
Collector current (pulse)	$I_{C(pulse)}$	5.0[Note]	A
Base current (DC)	$I_{B(DC)}$	0.5	A
Total power dissipation	P_T (T_C = 25°C)	20	W
Total power dissipation	P_T (T_A = 25°C)	2.0	W
Junction temperature	T_j	150	°C
Storage temperature	T_{stg}	−55 to +150	°C

Note PW ≤ 300 μs, duty cycle ≤ 10%

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ELECTRICAL CHARACTERISTICS (T_A = 25°C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Collector cutoff current	I_{CBO}	V_{CB} = 60 V, I_E = 0 A			10	μA
Emitter cutoff current	I_{EBO}	V_{EB} = 7.0 V, I_C = 0 A			10	μA
DC current gain	h_{FE1}	V_{CE} = 5.0 V, I_C = 0.5 A[Note]	800	1,300	3,200	
DC current gain	h_{FE2}	V_{CE} = 5.0 V, I_C = 3.0 A[Note]	500	1,000		
Collector saturation voltage	$V_{CE(sat)}$	I_C = 2.0 A, I_B = 20 mA[Note]		0.3	0.5	V
Base saturation voltage	$V_{BE(sat)}$	I_C = 2.0 A, I_B = 20 mA[Note]			1.2	V
Gain bandwidth product	f_T	V_{CE} = 5.0 V, I_C = 0.1 A		110		MHz
Collector capacitance	C_{ob}	V_{CB} = 10 V, I_E = 0 A, f = 1.0 MHz		50		pF

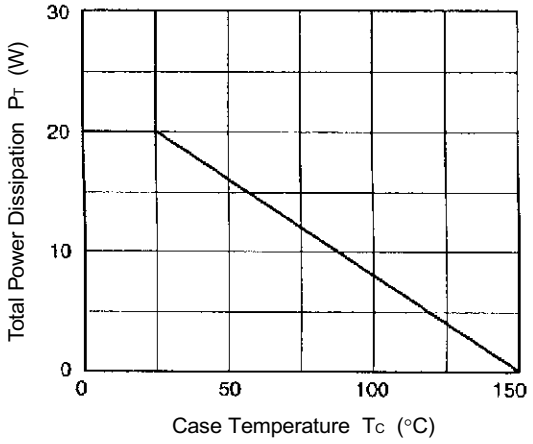
Note Pulse test PW ≤ 350 μs, duty cycle ≤ 2%

h_{FE1} CLASSIFICATION

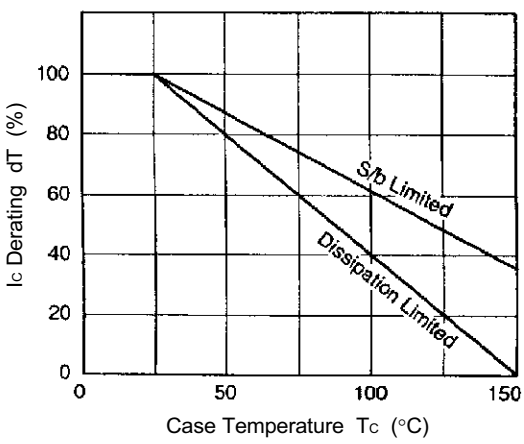
Marking	M	L	K
h_{FE1}	800 to 1,600	1,000 to 2,000	1,600 to 3,200

TYPICAL CHARACTERISTICS (T_A = 25°C)

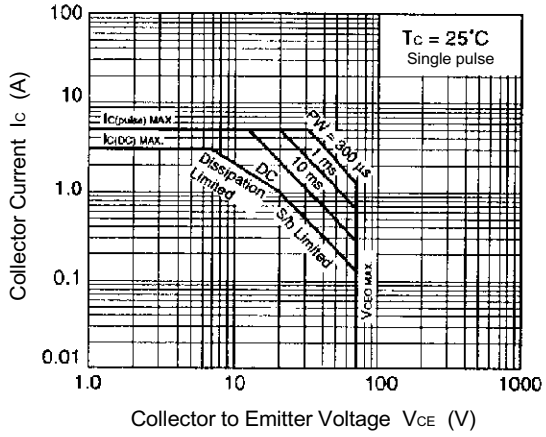
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



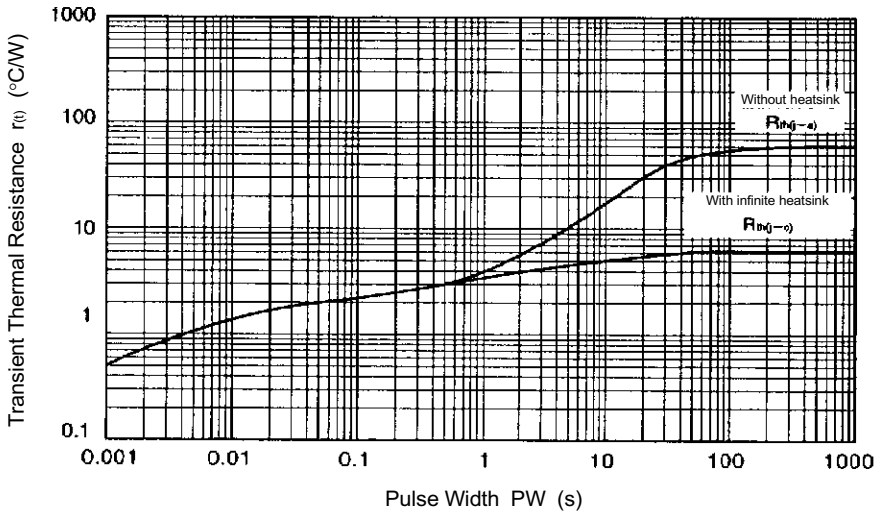
DERATING CURVE OF SAFE OPERATING AREA



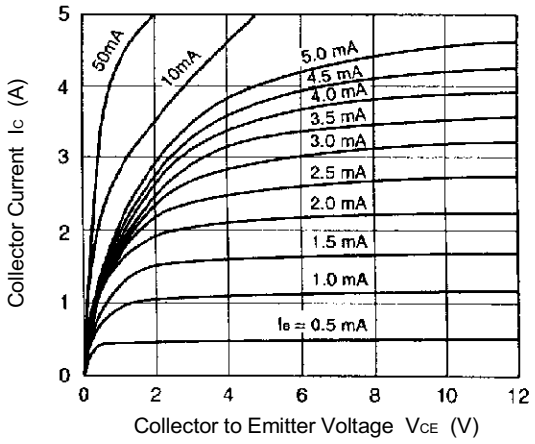
FORWARD BIAS SAFE OPERATING AREA



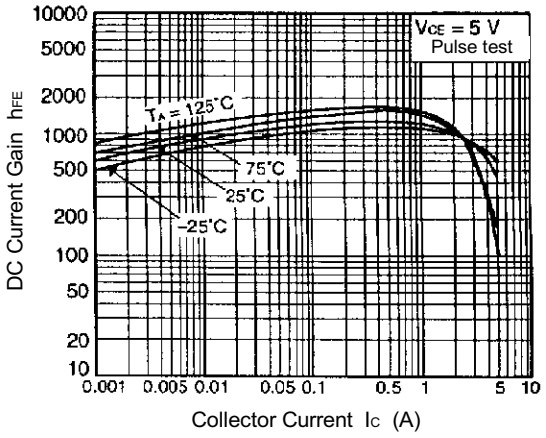
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



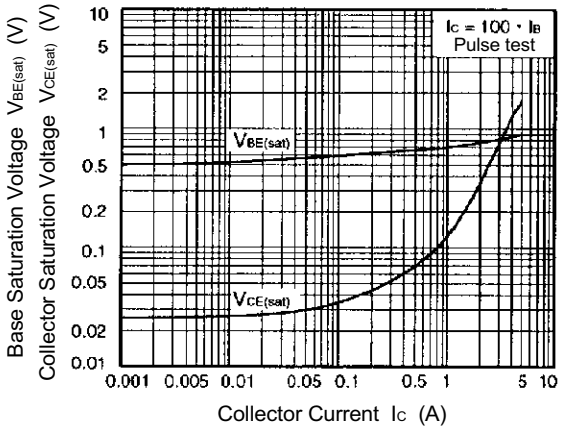
COLLECTOR CURRENT vs.
COLLECTOR TO EMITTER VOLTAGE



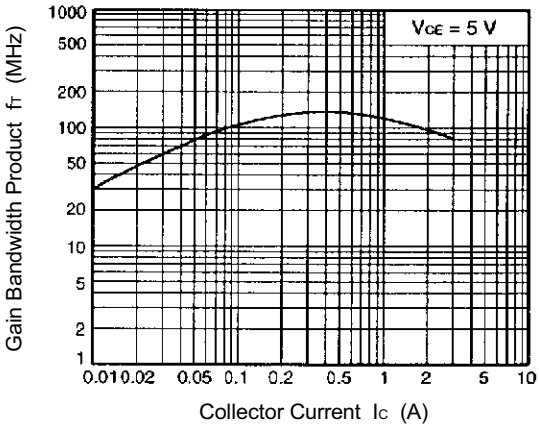
DC CURRENT GAIN vs.
COLLECTOR CURRENT



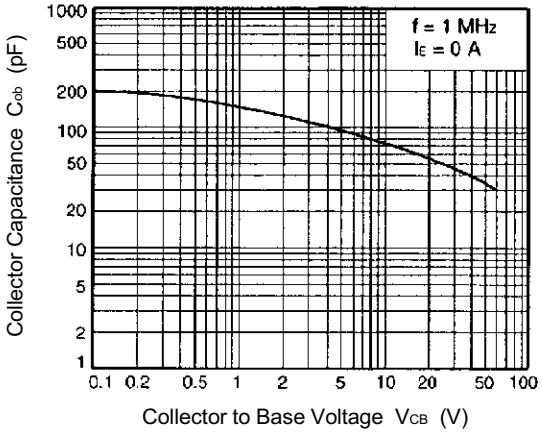
COLLECTOR AND BASE SATURATION
VOLTAGE vs. COLLECTOR CURRENT



GAIN BANDWIDTH PROFDUCT vs.
COLLECTOR CURRENT



OUTPUT CAPACITANCE vs.
COLLECTOR TO BASE VOLTAGE



[MEMO]

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