

2SD1164-Z

R07DS0254EJ0400

Rev.4.00

Feb 24, 2011

SILICON POWER TRANSISTOR

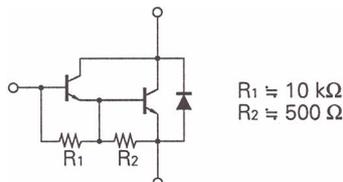
DESCRIPTION

The 2SD1164-Z is designed for Low Frequency Amplifier and Switching, especially in Hybrid Integrated Circuits.

FEATURES

- High $h_{FE} = 2\ 000$ to $30\ 000$

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ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$)

CHARACTERISTICS	SYMBOL	RATINGS	UNIT
Collector to Base Voltage	V_{CBO}	150	V
Collector to Emitter Voltage	V_{CEO}	60	V
Base to Emitter Voltage	V_{EBO}	8.0	V
Collector Current (DC)	$I_{C(DC)}$	2	A
Collector Current (pulse) ^{Note 1}	$I_{C(pulse)}$	4	A
Total Power Dissipation ($T_A = 25^\circ\text{C}$) ^{Note 2}	P_T	2.0	W
Junction Temperature	T_j	150	$^\circ\text{C}$
Storage Temperature	T_{stg}	-55 to +150	$^\circ\text{C}$

Notes 1. $PW \leq 10\ ms$, Duty Cycle $\leq 50\%$

2. When mounted on ceramic substrate of $7.5\ cm^2 \times 0.7\ mm$

The mark <R> shows major revised points.

The revised points can be easily searched by copying an "<R>" in the PDF file and specifying it in the "Find what:" field.

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

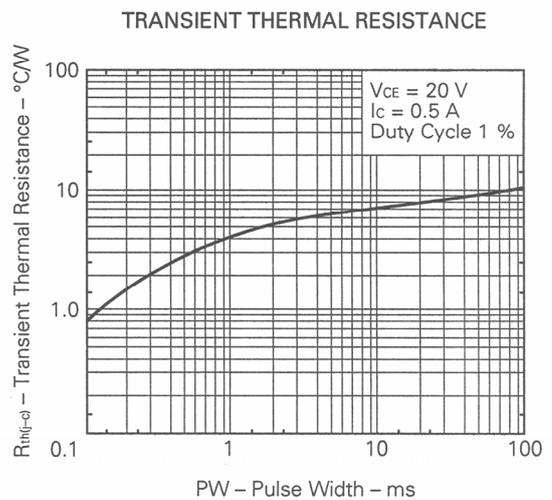
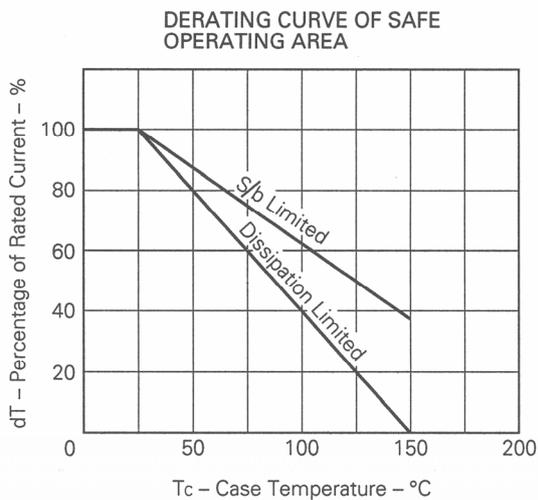
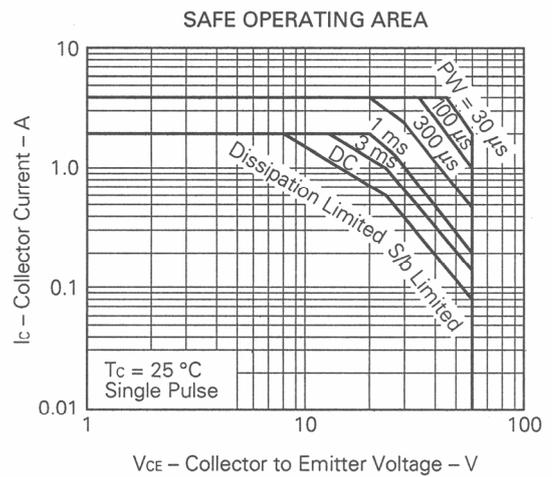
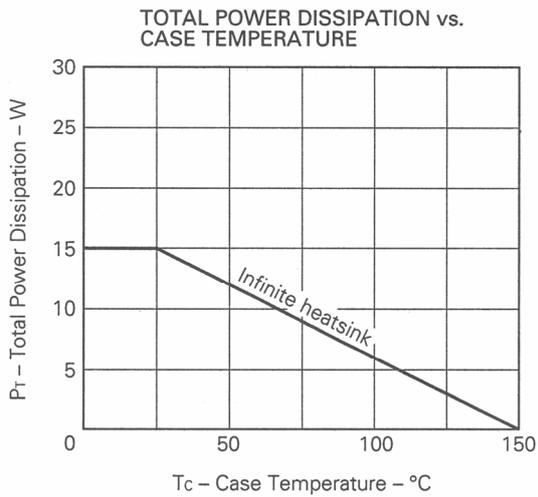
CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Collector Cutoff Current	I _{CB0}			10	μA	V _{CB} = 60 V, I _E = 0
Emitter Cutoff Current	I _{EB0}			1.0	mA	V _{EB} = 5.0 V, I _C = 0
DC Current Gain	h _{FE1} *	1 000				V _{CE} = 2.0 V, I _C = 0.5 A
DC Current Gain	h _{FE2} *	2 000		30 000		V _{CE} = 2.0 V, I _C = 1.0 A
Collector Saturation Voltage	V _{CE(sat)} *			1.5	V	I _C = 1.0 A, I _B = 1.0 mA
Base Saturation Voltage	V _{BE(sat)} *			2.0	V	I _C = 1.0 A, I _B = 1.0 mA
Turn-on Time	t _{on}		0.5		μs	I _C = 1.0 A, I _{B1} = -I _{B2} = 1.0 mA V _{CC} = 50 V, R _L = 50 Ω
Storage Time	t _{stg}		1.0		μs	
Fall Time	t _f		1.0		μs	

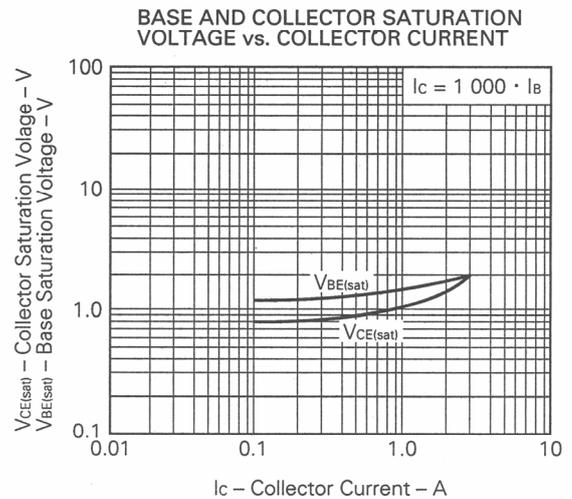
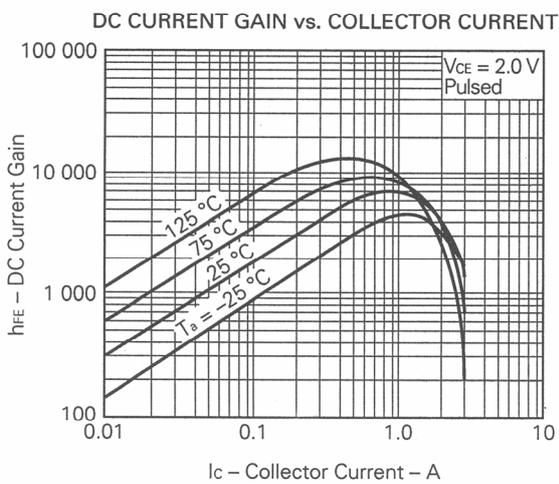
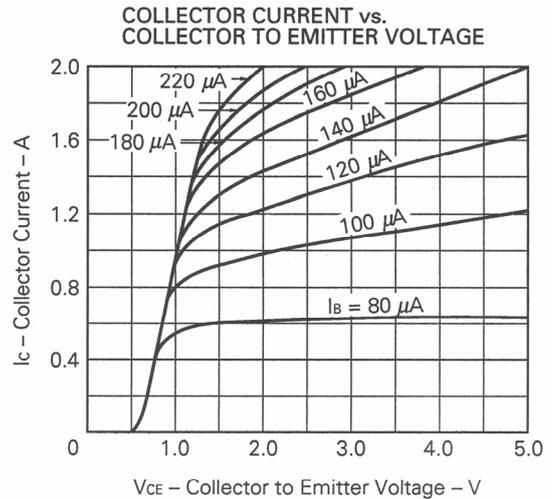
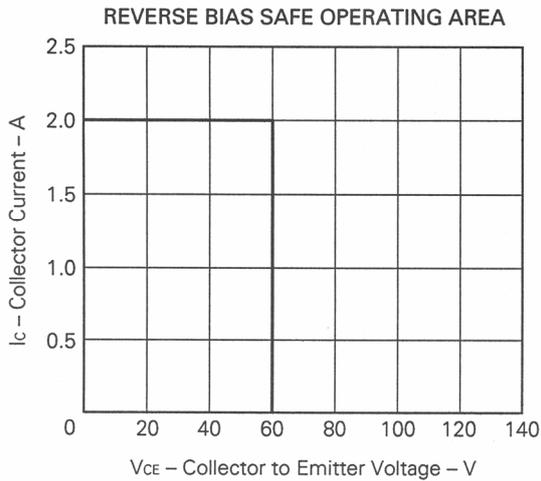
*Pulsed: PW ≤ 350 μs, Duty Cycle ≤ 2 %

h_{FE} Classification

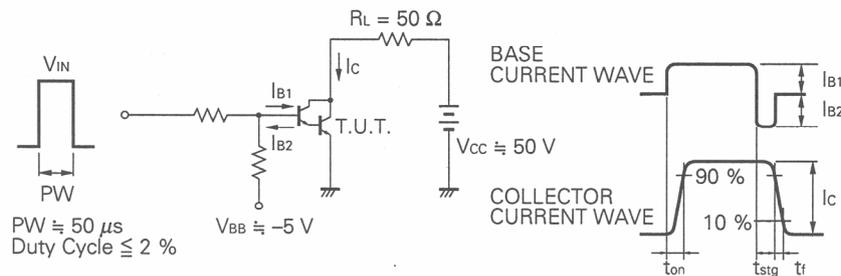
MARKING	M	L	K
h _{FE2}	2 000 to 5 000	4 000 to 10 000	8 000 to 30 000

TYPICAL CHARACTERISTICS (T_a = 25 °C)



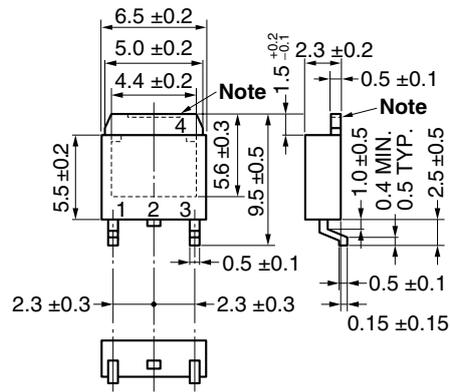


SWITCHING TIME (t_{on} , t_{stg} , t_f) TEST CIRCUIT



PACKAGE DRAWING (Unit: mm)

TO-252 (MP-3Z)



- 1. Base
- 2. Collector
- 3. Emitter
- 4. Collector Fin

Note The depth of notch at the top of the fin is from 0 to 0.2 mm.

Revision History	2SD1164-Z Data Sheet
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Rev.	Date	Description	
		Page	Summary
-	Jul 2006	-	Previous No. : D18286EJ3V0DS00
4.00	Feb 24, 2011	p.1	Modification of equivalent circuit

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