

RC38208A204

FemtoClock3 Family Custom Configuration

General Description

This document details the custom configuration that is programmed into the one time programmable (OTP) memory of the RC38208A204. Please refer to the device datasheet for further information about the device.

Output Frequency Overview

Output	OUT1	OUT2	OUT4	OUT5
Freq	-	-	-	-

Output	OUT6	OUT7	OUT8	OUT10
Freq	-	-	-	-

Note: Frequencies shown in parentheses indicates that the output is in disabled state by default.

Serial Interface Configuration

Config Index	Serial Port Configuration
config_0	I2C (1-byte address), 7-bit address: 0 0 0 1 A2 A1 A0

I2C Address Selection Bits

Config Index	I2C Address Bit A2	I2C Address Bit A1	I2C Address Bit A0
config_0	0	SDO (PIN G3)	nCS (PIN D4)

GPIO Startup Configuration

Pin Number	GPIO	Function Description
F6	GPIO0	NOT_USED
E6	GPIO1	NOT_USED

VDD Pins

Property	Value
VDD_VCO	1.8V
VDDXO_DCD	1.8V
VDD_FAN	1.8V
VDD_REP	1.8V
VDD_DIG	1.8V
VDD_CLK	1.8V
VDD_FOD0	1.8V
VDD_FOD1	1.8V
VDD_FOD2	1.8V
VDDO1	1.8V
VDDO2	1.8V
VDDO4	1.8V
VDDO5	1.8V
VDDO6	1.8V
VDDO7	1.8V
VDDO8	1.8V
VDDO10	1.8V

General Overview

Property	Value
Serial Interface	I2C (1-byte address), 7-bit address: 0 0 0 1 A2 A1 A0
Operation Mode DPLL0	Synthesizer
Operation Mode DPLL1	Synthesizer
External EEPROM Load	Enabled
XIN	54MHz
Crystal CL	8pF
VCO Frequency	9.5GHz
CLKIN0	DISABLED
CLKIN2	DISABLED
APLL Loop BW	~501.9263kHz
DPLL0 Lock BW	~63.5208Hz
DPLL0 Acquire BW	~9.147kHz
DPLL0 Ref Mux Control	Controlled by dpll_ref_sel / CLKIN0
DPLL1 Lock BW	~63.5208Hz
DPLL1 Acquire BW	~9.147kHz
DPLL1 Ref Mux Control	Controlled by dpll_ref_sel / CLKIN0

Note: This dash code has TOP.GLOBAL.DEVICE_CNFG.i2c_addr_sel set to 0x3, meaning that bit 0 of the I2C address comes from pin nCS and bit 1 from pin SDO.

The nCS and SDO pins have an internal pull up. Example: If both nCS and SDO are left floating, the resulting I2C address will be 0x0B at device power up.

GPIO Settings

Pin Number	GPIO	Function Description	Internal PU	Internal PD	Output Drive Strength
F6	GPIO0	General purpose input (input)	Enable	Disable	N/A
E6	GPIO1	APLL lock (from frequency-based lock detect) (output)	Enable	Disable	CMOS Output mode and power supply of 1.8V.

Output Overview

Output	IOD Mux Selection	Frequency	Status	Output Type	Output Boost
OUT1	VCO/N	-	disabled	powered down (hi-z)	-
OUT2	VCO/N	-	disabled	powered down (hi-z)	-
OUT4	VCO/N	-	disabled	powered down (hi-z)	-
OUT5	VCO/N	-	disabled	powered down (hi-z)	-
OUT6	VCO/N	-	disabled	powered down (hi-z)	-
OUT7	VCO/N	-	disabled	powered down (hi-z)	-
OUT8	VCO/N	-	disabled	powered down (hi-z)	-
OUT10	VCO/N	-	disabled	powered down (hi-z)	-

Note: All VDDOs need to ramp before or at the same time as other cores power rails.

External EEPROM Settings

Property	Value
Part Number	R1EX24064ASA
Address Size	2-byte address
I2C Speed	400kHz
Length	8KB
EEPROM Load Pins	SCL_SCLK, SDA_SDIO
7-bit Address	1 0 1 0 A2 A1 A0
EEPROM Address Bit A2	0
EEPROM Address Bit A1	0
EEPROM Address Bit A0	0

Ordering Info

Part Number	Carrier Type
RC38208A204GBB#BC0	Tray
RC38208A204GBB#HC0	Tape and Reel

Notes:

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