

## RC38208A200

FemtoClock3 Family Custom Configuration

### General Description

This document details the custom configuration that is programmed into the one time programmable (OTP) memory of the RC38208A200. Please refer to the device datasheet for further information about the device.

### Configuration List

Configuration Name	Configuration Index
spi_4wire	config_0
spi_3wire	config_1
i2c_no_eeprom	config_2
i2c_with_eeprom	config_3

### Output Frequency Overview

Config Index	OUT1	OUT2	OUT4	OUT5
config_0	-	-	-	-
config_1	-	-	-	-
config_2	-	-	-	-
config_3	-	-	-	-

  

Config Index	OUT6	OUT7	OUT8	OUT10
config_0	-	-	-	-
config_1	-	-	-	-
config_2	-	-	-	-
config_3	-	-	-	-

Note: Frequencies shown in parentheses indicates that the output is in disabled state by default.

### Configuration Selection Overview: Static Multi Config

Config Slot	Config Selection 1	Config Selection 0	Config Index
slot_0	GPIO1 Low	GPIO0 Low	config_0
slot_1	GPIO1 Low	GPIO0 High	config_1
slot_2	GPIO1 High	GPIO0 Low	config_2
slot_3	GPIO1 High	GPIO0 High	config_3

## Serial Interface Configuration

Config Index	Serial Port Configuration
config_0	4-wire SPI (2-byte address)
config_1	3-wire SPI (2-byte address)
config_2	I2C (2-byte address), 7-bit address: 0 0 0 1 A2 A1 A0
config_3	I2C (2-byte address), 7-bit address: 0 0 0 1 A2 A1 A0

## I2C Address Selection Bits

Config Index	I2C Address Bit A2	I2C Address Bit A1	I2C Address Bit A0
config_0	N/A	N/A	N/A
config_1	N/A	N/A	N/A
config_2	0	SDO (PIN G3)	nCS (PIN D4)
config_3	0	SDO (PIN G3)	nCS (PIN D4)

## GPIO Startup Configuration

Pin Number	GPIO	Function Description
F6	GPIO0	CONFIG_SEL0
E6	GPIO1	CONFIG_SEL1

## VDD Pins

Property	Value
VDD_VCO	1.8V
VDDXO_DCD	1.8V
VDD_FAN	1.8V
VDD_REP	1.8V
VDD_DIG	1.8V
VDD_CLK	1.8V
VDD_FOD0	1.8V
VDD_FOD1	1.8V
VDD_FOD2	1.8V
VDDO1	1.8V
VDDO2	1.8V
VDDO4	1.8V
VDDO5	1.8V
VDDO6	1.8V
VDDO7	1.8V
VDDO8	1.8V
VDDO10	1.8V

## spi\_4wire (config\_0) General Overview

Property	Value
Serial Interface	4-wire SPI (2-byte address)
Operation Mode DPLL0	Synthesizer
Operation Mode DPLL1	Synthesizer
External EEPROM Load	Disabled
XIN	68
Crystal CL	8.24pF
VCO Frequency	9.8304GHz
CLKIN0	DISABLED
CLKIN2	DISABLED
APLL Loop BW	~707.0569kHz
DPLL0 Lock BW	~63.7413Hz
DPLL0 Acquire BW	N/A
DPLL0 Ref Mux Control	Controlled by dpll_ref_sel / CLKIN0
DPLL1 Lock BW	~63.7413Hz
DPLL1 Acquire BW	N/A
DPLL1 Ref Mux Control	Controlled by dpll_ref_sel / CLKIN0

Note: This dash code has TOP.GLOBAL.DEVICE\_CNFG.i2c\_addr\_sel set to 0x3, meaning that bit 0 of the I2C address comes from pin nCS and bit 1 from pin SDO.

The nCS and SDO pins have an internal pull up. Example: If both nCS and SDO are left floating, the resulting I2C address will be 0x0B at device power up.

## spi\_4wire (config\_0) GPIO Settings

Pin Number	GPIO	Function Description	Internal PU	Internal PD	Output Drive Strength
F6	GPIO0	General purpose input (input)	Enable	Disable	N/A
E6	GPIO1	APLL lock (from frequency-based lock detect) (output)	Enable	Disable	Open drain Output mode. Fast mode.

## spi\_4wire (config\_0) Output Overview

Output	IOD Mux Selection	Frequency	Status	Output Type	Output Boost
OUT1	VCO/N	-	disabled	powered down (hi-z)	-
OUT2	VCO/N	-	disabled	powered down (hi-z)	-
OUT4	VCO/N	-	disabled	powered down (hi-z)	-
OUT5	VCO/N	-	disabled	powered down (hi-z)	-
OUT6	Static high (Minimal power) [Reserved]	-	disabled	powered down (hi-z)	-
OUT7	Static high (Minimal power) [Reserved]	-	disabled	powered down (hi-z)	-
OUT8	Static high (Minimal power) [Reserved]	-	disabled	powered down (hi-z)	-
OUT10	Static high (Minimal power) [Reserved]	-	disabled	powered down (hi-z)	-

Note: All VDDOs need to ramp before or at the same time as other cores power rails.

## spi\_3wire (config\_1) General Overview

Property	Value
Serial Interface	3-wire SPI (2-byte address)
Operation Mode DPLL0	Synthesizer
Operation Mode DPLL1	Synthesizer
External EEPROM Load	Disabled
XIN	68
Crystal CL	8.24pF
VCO Frequency	9.8304GHz
CLKIN0	DISABLED
CLKIN2	DISABLED
APLL Loop BW	~707.0569kHz
DPLL0 Lock BW	~63.7413Hz
DPLL0 Acquire BW	N/A
DPLL0 Ref Mux Control	Controlled by dpll_ref_sel / CLKIN0
DPLL1 Lock BW	~63.7413Hz
DPLL1 Acquire BW	N/A
DPLL1 Ref Mux Control	Controlled by dpll_ref_sel / CLKIN0

Note: This dash code has TOP.GLOBAL.DEVICE\_CNFG.i2c\_addr\_sel set to 0x3, meaning that bit 0 of the I2C address comes from pin nCS and bit 1 from pin SDO.

The nCS and SDO pins have an internal pull up. Example: If both nCS and SDO are left floating, the resulting I2C address will be 0x0B at device power up.

## spi\_3wire (config\_1) GPIO Settings

Pin Number	GPIO	Function Description	Internal PU	Internal PD	Output Drive Strength
F6	GPIO0	General purpose input (input)	Enable	Disable	N/A
E6	GPIO1	APLL lock (from frequency-based lock detect) (output)	Enable	Disable	Open drain Output mode. Fast mode.

## spi\_3wire (config\_1) Output Overview

Output	IOD Mux Selection	Frequency	Status	Output Type	Output Boost
OUT1	VCO/N	-	disabled	powered down (hi-z)	-
OUT2	VCO/N	-	disabled	powered down (hi-z)	-
OUT4	VCO/N	-	disabled	powered down (hi-z)	-
OUT5	VCO/N	-	disabled	powered down (hi-z)	-
OUT6	Static high (Minimal power) [Reserved]	-	disabled	powered down (hi-z)	-
OUT7	Static high (Minimal power) [Reserved]	-	disabled	powered down (hi-z)	-
OUT8	Static high (Minimal power) [Reserved]	-	disabled	powered down (hi-z)	-
OUT10	Static high (Minimal power) [Reserved]	-	disabled	powered down (hi-z)	-

Note: All VDDOs need to ramp before or at the same time as other cores power rails.

## i2c\_no\_eeprom (config\_2) General Overview

Property	Value
Serial Interface	I2C (2-byte address), 7-bit address: 0 0 0 1 A2 A1 A0
Operation Mode DPLL0	Synthesizer
Operation Mode DPLL1	Synthesizer
External EEPROM Load	Disabled
XIN	68
Crystal CL	8.24pF
VCO Frequency	9.8304GHz
CLKIN0	DISABLED
CLKIN2	DISABLED
APLL Loop BW	~707.0569kHz
DPLL0 Lock BW	~63.7413Hz
DPLL0 Acquire BW	N/A
DPLL0 Ref Mux Control	Controlled by dpll_ref_sel / CLKIN0
DPLL1 Lock BW	~63.7413Hz
DPLL1 Acquire BW	N/A
DPLL1 Ref Mux Control	Controlled by dpll_ref_sel / CLKIN0

Note: This dash code has TOP.GLOBAL.DEVICE\_CNFG.i2c\_addr\_sel set to 0x3, meaning that bit 0 of the I2C address comes from pin nCS and bit 1 from pin SDO.

The nCS and SDO pins have an internal pull up. Example: If both nCS and SDO are left floating, the resulting I2C address will be 0x0B at device power up.

## i2c\_no\_eeprom (config\_2) GPIO Settings

Pin Number	GPIO	Function Description	Internal PU	Internal PD	Output Drive Strength
F6	GPIO0	General purpose input (input)	Enable	Disable	N/A
E6	GPIO1	APLL lock (from frequency-based lock detect) (output)	Enable	Disable	Open drain Output mode. Fast mode.

## i2c\_no\_eeprom (config\_2) Output Overview

Output	IOD Mux Selection	Frequency	Status	Output Type	Output Boost
OUT1	VCO/N	-	disabled	powered down (hi-z)	-
OUT2	VCO/N	-	disabled	powered down (hi-z)	-
OUT4	VCO/N	-	disabled	powered down (hi-z)	-
OUT5	VCO/N	-	disabled	powered down (hi-z)	-
OUT6	Static high (Minimal power) [Reserved]	-	disabled	powered down (hi-z)	-
OUT7	Static high (Minimal power) [Reserved]	-	disabled	powered down (hi-z)	-
OUT8	Static high (Minimal power) [Reserved]	-	disabled	powered down (hi-z)	-
OUT10	Static high (Minimal power) [Reserved]	-	disabled	powered down (hi-z)	-

Note: All VDDOs need to ramp before or at the same time as other cores power rails.

## i2c\_with\_eeprom (config\_3) General Overview

Property	Value
Serial Interface	I2C (2-byte address), 7-bit address: 0 0 0 1 A2 A1 A0
Operation Mode DPLL0	Synthesizer
Operation Mode DPLL1	Synthesizer
External EEPROM Load	Enabled
XIN	68
Crystal CL	8.24pF
VCO Frequency	9.8304GHz
CLKIN0	DISABLED
CLKIN2	DISABLED
APLL Loop BW	~707.0569kHz
DPLL0 Lock BW	~63.7413Hz
DPLL0 Acquire BW	N/A
DPLL0 Ref Mux Control	Controlled by dpll_ref_sel / CLKIN0
DPLL1 Lock BW	~63.7413Hz
DPLL1 Acquire BW	N/A
DPLL1 Ref Mux Control	Controlled by dpll_ref_sel / CLKIN0

Note: This dash code has TOP.GLOBAL.DEVICE\_CNFG.i2c\_addr\_sel set to 0x3, meaning that bit 0 of the I2C address comes from pin nCS and bit 1 from pin SDO.

The nCS and SDO pins have an internal pull up. Example: If both nCS and SDO are left floating, the resulting I2C address will be 0x0B at device power up.

## i2c\_with\_eeprom (config\_3) GPIO Settings

Pin Number	GPIO	Function Description	Internal PU	Internal PD	Output Drive Strength
F6	GPIO0	General purpose input (input)	Enable	Disable	N/A
E6	GPIO1	APLL lock (from frequency-based lock detect) (output)	Enable	Disable	Open drain Output mode. Fast mode.

## i2c\_with\_eeprom (config\_3) Output Overview

Output	IOD Mux Selection	Frequency	Status	Output Type	Output Boost
OUT1	VCO/N	-	disabled	powered down (hi-z)	-
OUT2	VCO/N	-	disabled	powered down (hi-z)	-
OUT4	VCO/N	-	disabled	powered down (hi-z)	-
OUT5	VCO/N	-	disabled	powered down (hi-z)	-
OUT6	Static high (Minimal power) [Reserved]	-	disabled	powered down (hi-z)	-
OUT7	Static high (Minimal power) [Reserved]	-	disabled	powered down (hi-z)	-
OUT8	Static high (Minimal power) [Reserved]	-	disabled	powered down (hi-z)	-
OUT10	Static high (Minimal power) [Reserved]	-	disabled	powered down (hi-z)	-

Note: All VDDOs need to ramp before or at the same time as other cores power rails.

## i2c\_with\_eeprom (config\_3) External EEPROM Settings

Property	Value
Part Number	24LC64
Address Size	2-byte address
I2C Speed	400kHz
Length	8KB
EEPROM Load Pins	GPIO0, GPIO1
7-bit Address	1 0 1 0 A2 A1 A0
EEPROM Address Bit A2	0
EEPROM Address Bit A1	0
EEPROM Address Bit A0	0

## Ordering Info

Part Number	Carrier Type
RC38208A200GBB#BC0	Tray
RC38208A200GBB#HC0	Tape and Reel

Notes:

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