

## RC32312A004

FemtoClock3 Family Custom Configuration

### General Description

This document details the custom configuration that is programmed into the one time programmable (OTP) memory of the RC32312A004. Please refer to the device datasheet for further information about the device.

### Configuration List

Configuration Name	Configuration Index
default	config_0
LOAD_EEPROM	config_1

### Output Frequency Overview

Config Index	OUT0	OUT1	OUT2	OUT3	OUT4	OUT5
config_0	156.25MHz	156.25MHz	156.25MHz	156.25MHz	156.25MHz	156.25MHz
config_1	-	-	-	-	-	-

  

Config Index	OUT6	OUT7	OUT8	OUT9	OUT10	OUT11
config_0	156.25MHz	156.25MHz	156.25MHz	156.25MHz	156.25MHz	-
config_1	-	-	-	-	-	-

### Configuration Selection Overview: Static Multi Config

Config Slot	Config Selection 1	Config Selection 0	Config Index
slot_0	not assigned Low	GPIO0 Low	config_0
slot_1	not assigned Low	GPIO0 High	config_1
slot_2	not assigned High	GPIO0 Low	config_0
slot_3	not assigned High	GPIO0 High	config_1

### Serial Interface Configuration

Config Index	Serial Port Configuration
config_0	I2C (1-byte address), 7-bit address: 0x09
config_1	I2C (1-byte address), 7-bit address: 0x09

### I2C Address Selection Bits

Config Index	I2C Address Bit A2	I2C Address Bit A1	I2C Address Bit A0
config_0	0	0	1
config_1	0	0	1

## GPIO Startup Configuration

Pin Number	GPIO	Function Description
62	GPIO0	CONFIG_SEL0
41	GPIO1	N/A
40	GPIO2	N/A
36	GPIO3	N/A
63	GPIO4	N/A
49	GPIO5	N/A
45	GPIO6	N/A
2	LOCK	N/A

## VDD Pins

Property	Value
VDD_VCO	1.8V
VDDXO_DCD	1.8V
VDDD33_SERIAL	1.8V
VDDD33_DIA	1.8V
VDD_CLK	1.8V
VDDO0	1.8V
VDDO1_FOD0	1.8V
VDDO2	1.8V
VDDO3	1.8V
VDDO4	1.8V
VDDO5	1.8V
VDDO6	1.8V
VDDO7	1.8V
VDDO8_FOD1	1.8V
VDDO9	1.8V
VDDO10_FOD2	1.8V
VDDO11	1.8V

## default (config\_0) General Overview

Property	Value
Serial Interface	I2C (1-byte address), 7-bit address: 0x09
Operation Mode	Jitter Attenuator
External EEPROM Load	Disabled
XIN	54
Crystal CL	8.24pF
VCO Frequency	10GHz
CLKIN0	25MHz (LVCMOS_DC_COUPLED)
nCLKIN0	None (LVCMOS_DC_COUPLED)
CLKIN1	DISABLED
CLKIN2	DISABLED
CLKIN3	DISABLED
APLL Loop BW	~513.5731kHz
Lock BW	~23.8203Hz
Acquire BW	~238.2028Hz

## default (config\_0) GPIO Settings

Pin Number	GPIO	Function Description	Internal PU	Internal PD	Output Drive Strength
62	GPIO0	General purpose input (input)	Enable	Disable	N/A
41	GPIO1	General purpose input (input)	Enable	Disable	N/A
40	GPIO2	General purpose input (input)	Enable	Disable	N/A
36	GPIO3	General purpose input (input)	Enable	Disable	N/A
63	GPIO4	General purpose input (input)	Enable	Disable	N/A
49	GPIO5	General purpose input (input)	Enable	Disable	N/A
45	GPIO6	General purpose input (input)	Enable	Disable	N/A
2	GPIO8	DPLL lock (output)	Enable	Disable	CMOS Output mode and power supply of 1.8V.

## default (config\_0) Output Overview

Output	IOD Mux Selection	Frequency	Status	Output Type	Output Boost
OUT0	VCO/2	156.25MHz	enabled	HCSL (internally terminated) Amplitude: 950mV	disabled
OUT1	VCO/2	156.25MHz	enabled	HCSL (internally terminated) Amplitude: 950mV	disabled
OUT2	VCO/2	156.25MHz	enabled	HCSL (internally terminated) Amplitude: 950mV	disabled

## RC32312A004 Datasheet Addendum

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OUT3	VCO/2	156.25MHz	enabled	HCSL (internally terminated) Amplitude: 950mV	disabled
OUT4	VCO/2	156.25MHz	enabled	HCSL (internally terminated) Amplitude: 950mV	disabled
OUT5	VCO/2	156.25MHz	enabled	HCSL (internally terminated) Amplitude: 950mV	disabled
OUT6	VCO/2	156.25MHz	enabled	HCSL (internally terminated) Amplitude: 950mV	disabled
OUT7	VCO/2	156.25MHz	enabled	HCSL (internally terminated) Amplitude: 950mV	disabled
OUT8	VCO/2	156.25MHz	enabled	HCSL (internally terminated) Amplitude: 950mV	disabled
OUT9	VCO/2	156.25MHz	enabled	HCSL (internally terminated) Amplitude: 950mV	disabled
OUT10	VCO/2	156.25MHz	enabled	HCSL (internally terminated) Amplitude: 950mV	disabled
OUT11	VCO/2	-	disabled	DISABLED (Hi-Z/Hi-Z)	-

Note: All VDDOs need to ramp before or at the same time as other cores power rails.

## LOAD\_EEPROM (config\_1) General Overview

Property	Value
Serial Interface	I2C (1-byte address), 7-bit address: 0x09
Operation Mode	Jitter Attenuator
External EEPROM Load	Enabled
XIN	54MHz
Crystal CL	8.24pF
VCO Frequency	10GHz
CLKIN0	DISABLED
CLKIN1	DISABLED
CLKIN2	DISABLED
CLKIN3	DISABLED
APLL Loop BW	~513.5731kHz
Lock BW	~23.8203Hz
Acquire BW	~238.2028Hz

## LOAD\_EEPROM (config\_1) GPIO Settings

Pin Number	GPIO	Function Description	Internal PU	Internal PD	Output Drive Strength
62	GPIO0	General purpose input (input)	Enable	Disable	N/A
41	GPIO1	General purpose input (input)	Enable	Disable	N/A
40	GPIO2	General purpose input (input)	Enable	Disable	N/A
36	GPIO3	General purpose input (input)	Enable	Disable	N/A
63	GPIO4	General purpose input (input)	Enable	Disable	N/A
49	GPIO5	General purpose input (input)	Enable	Disable	N/A
45	GPIO6	General purpose input (input)	Enable	Disable	N/A
2	GPIO8	Device Ready (startup sequence complete) (output)	Enable	Disable	CMOS Output mode and power supply of 1.8V.

## LOAD\_EEPROM (config\_1) Output Overview

Output	IOD Mux Selection	Frequency	Status	Output Type	Output Boost
OUT0	VCO/2	-	disabled	DISABLED (Hi-Z/Hi-Z)	-
OUT1	VCO/2	-	disabled	DISABLED (Hi-Z/Hi-Z)	-
OUT2	VCO/2	-	disabled	DISABLED (Hi-Z/Hi-Z)	-
OUT3	VCO/2	-	disabled	DISABLED (Hi-Z/Hi-Z)	-
OUT4	VCO/2	-	disabled	DISABLED (Hi-Z/Hi-Z)	-
OUT5	VCO/2	-	disabled	DISABLED (Hi-Z/Hi-Z)	-

OUT6	VCO/2	-	disabled	DISABLED (Hi-Z/Hi-Z)	-
OUT7	VCO/2	-	disabled	DISABLED (Hi-Z/Hi-Z)	-
OUT8	VCO/2	-	disabled	DISABLED (Hi-Z/Hi-Z)	-
OUT9	VCO/2	-	disabled	DISABLED (Hi-Z/Hi-Z)	-
OUT10	VCO/2	-	disabled	DISABLED (Hi-Z/Hi-Z)	-
OUT11	VCO/2	-	disabled	DISABLED (Hi-Z/Hi-Z)	-

Note: All VDDOs need to ramp before or at the same time as other cores power rails.

### LOAD\_EEPROM (config\_1) External EEPROM Settings

Property	Value
Part Number	R1EX24064ASA
Address	0x50
Address Size	2-byte address
I2C Speed	100kHz
Length	8KB

## Ordering Info

Part Number	Carrier Type
RC32312A004GN1#BB0	Tray
RC32312A004GN1#KB0	Tape and Reel

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