RC22312A003

FemtoClock3 Family Custom Configuration

General Description

This document details the custom configuration that is programmed into the one time programmable (OTP) memory of the RC22312A003. Please refer to the device datasheet for further information about the device.

Configuration List

Configuration Name	Configuration Index
oceanranch	config_0
superset	config_1

Output Frequency Overview

Config Index	OUT0	OUT1	OUT2	OUT3	OUT4	OUT5
config_0	25MHz	25MHz	-	156.25MHz	156.25MHz	156.25MHz
config_1	25MHz	25MHz	156.25MHz	156.25MHz	156.25MHz	156.25MHz

Config Index	OUT6	OUT7	OUT8	OUT9	OUT10	OUT11
config_0	156.25MHz	156.25MHz	-	-	-	100MHz
config_1	156.25MHz	156.25MHz	156.25MHz	156.25MHz	50MHz	100MHz

Configuration Selection Overview: Static Multi Config

Config Slot	Config Selection 1	Config Selection 0	Config Index
slot_0	GPIO2 Low	GPIO1 Low	config_0
slot_1	GPIO2 Low	GPIO1 High	config_1
slot_2	GPIO2 High	GPIO1 Low	config_0
slot_3	GPIO2 High	GPIO1 High	config_1

Serial Interface Configuration

Config Index	Serial Port Configuration
config_0	I2C (1-byte address), 7-bit address: 0x08
config_1	I2C (1-byte address), 7-bit address: 0x08

I2C Address Selection Bits

Config Index	I2C Address Bit A2	I2C Address Bit A1	I2C Address Bit A0
config_0	0	0	0
config_1	0	0	0

GPIO Startup Configuration

Pin Number	GPIO	Function Description
62	GPIO0	N/A
41	GPIO1	CONFIG_SEL0
40	GPIO2	CONFIG_SEL1
36	GPIO3	N/A
63	GPIO4	N/A
49	GPIO5	N/A
45	GPIO6	N/A
2	LOCK	N/A

VDD Pins

Property	Value
VDD_VCO	1.8V
VDDXO_DCD	1.8V
VDDD33_SERIAL	1.8V
VDDD33_DIA	1.8V
VDD_CLK	1.8V
VDDO0	1.8V
VDDO1_FOD0	1.8V
VDDO2	1.8V
VDDO3	1.8V
VDDO4	1.8V
VDDO5	1.8V
VDDO6	1.8V
VDDO7	1.8V
VDDO8_FOD1	1.8V
VDDO9	1.8V
VDDO10_FOD2	1.8V
VDDO11	1.8V

oceanranch (config_0) General Overview

Property	Value
Serial Interface	I2C (1-byte address), 7-bit address: 0x08
Operation Mode	Synthesizer
External EEPROM Load	Disabled
XIN	62.5
Crystal CL	10.1451pF
VCO Frequency	10.625GHz
CLKIN0	DISABLED
CLKIN1	DISABLED
CLKIN2	DISABLED
CLKIN3	DISABLED
APLL Loop BW	~434.9677kHz
Lock BW	~64.3295Hz
Acquire BW	N/A

oceanranch (config_0) GPIO Settings

Pin Number	GPIO	Function Description	Internal PU	Internal PD	Output Drive Strength
62	GPIO0	Global OE (input)	Disable	Enable	N/A
41	GPIO1	General purpose input (input)	Disable	Enable	N/A
40	GPIO2	General purpose input (input)	Disable	Enable	N/A
36	GPIO3	General purpose input (input)	Disable	Enable	N/A
63	GPIO4	General purpose input (input)	Disable	Enable	N/A
49	GPIO5	General purpose input (input)	Disable	Enable	N/A
45	GPIO6	General purpose input (input)	Disable	Enable	N/A
2	GPIO8	General purpose input (input)	Enable	Disable	N/A

oceanranch (config_0) Output Overview

Output	IOD Mux Selection	Frequency	Status	Output Type	Output Boost
OUT0	FOD2	25MHz	GPIO Control	HCSL (internally terminated) Amplitude: 950mV	disabled
OUT1	FOD2	25MHz	GPIO Control	HCSL (internally terminated) Amplitude: 950mV	disabled
OUT2	VCO/2	-	disabled	DISABLED (Hi-Z/Hi-Z)	-
OUT3	VCO/2	156.25MHz	GPIO Control	HCSL (internally terminated) Amplitude: 950mV	disabled

OUT4	VCO/2	156.25MHz	GPIO Control	HCSL (internally terminated) Amplitude: 950mV	disabled
OUT5	VCO/2	156.25MHz	GPIO Control	HCSL (internally terminated) Amplitude: 950mV	disabled
OUT6	VCO/2	156.25MHz	GPIO Control	HCSL (internally terminated) Amplitude: 950mV	disabled
OUT7	VCO/2	156.25MHz	GPIO Control	HCSL (internally terminated) Amplitude: 950mV	disabled
OUT8	VCO/2	-	disabled	DISABLED (Hi-Z/Hi-Z)	-
OUT9	VCO/2	-	disabled	DISABLED (Hi-Z/Hi-Z)	disabled
OUT10	FOD2	-	disabled	DISABLED (Hi-Z/Hi-Z)	-
OUT11	FOD2	100MHz	GPIO Control	HCSL (internally terminated) Amplitude: 950mV	disabled

Note: All VDDOs need to ramp before or at the same time as other cores power rails.

superset (config_1) General Overview

Property	Value
Serial Interface	I2C (1-byte address), 7-bit address: 0x08
Operation Mode	Synthesizer
External EEPROM Load	Disabled
XIN	62.5
Crystal CL	10.1451pF
VCO Frequency	10.625GHz
CLKIN0	DISABLED
CLKIN1	DISABLED
CLKIN2	DISABLED
CLKIN3	DISABLED
APLL Loop BW	~434.9677kHz
Lock BW	~64.3295Hz
Acquire BW	N/A

superset (config_1) GPIO Settings

Pin Number	GPIO	Function Description	Internal PU	Internal PD	Output Drive Strength
62	GPIO0	Global OE (input)	Disable	Enable	N/A
41	GPIO1	General purpose input (input)	Disable	Enable	N/A
40	GPIO2	General purpose input (input)	Disable	Enable	N/A
36	GPIO3	General purpose input (input)	Disable	Enable	N/A
63	GPIO4	General purpose input (input)	Disable	Enable	N/A
49	GPIO5	General purpose input (input)	Disable	Enable	N/A
45	GPIO6	General purpose input (input)	Disable	Enable	N/A
2	GPIO8	General purpose input (input)	Enable	Disable	N/A

superset (config_1) Output Overview

Output	IOD Mux Selection	Frequency	Status	Output Type	Output Boost
OUT0	FOD2	25MHz	GPIO Control	HCSL (internally terminated) Amplitude: 950mV	disabled
OUT1	FOD2	25MHz	GPIO Control	HCSL (internally terminated) Amplitude: 950mV	disabled
OUT2	VCO/2	156.25MHz	GPIO Control	HCSL (internally terminated) Amplitude: 950mV	disabled
OUT3	VCO/2	156.25MHz	GPIO Control	HCSL (internally terminated) Amplitude: 950mV	disabled

OUT4	VCO/2	156.25MHz	GPIO Control	HCSL (internally terminated) Amplitude: 950mV	disabled
OUT5	VCO/2	156.25MHz	GPIO Control	HCSL (internally terminated) Amplitude: 950mV	disabled
OUT6	VCO/2	156.25MHz	GPIO Control	HCSL (internally terminated) Amplitude: 950mV	disabled
OUT7	VCO/2	156.25MHz	GPIO Control	HCSL (internally terminated) Amplitude: 950mV	disabled
OUT8	VCO/2	156.25MHz	GPIO Control	HCSL (internally terminated) Amplitude: 950mV	disabled
OUT9	VCO/2	156.25MHz	GPIO Control	HCSL (internally terminated) Amplitude: 950mV	disabled
OUT10	FOD2	50MHz	GPIO Control	HCSL (internally terminated) Amplitude: 950mV	disabled
OUT11	FOD2	100MHz	GPIO Control	HCSL (internally terminated) Amplitude: 950mV	disabled

Note: All VDDOs need to ramp before or at the same time as other cores power rails.

Ordering Info

Part Number	Carrier Type
RC22312A003GN1#BB0	Tray
RC22312A003GN1#KB0	Tape and Reel

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