RC22312A002

FemtoClock3 Family Custom Configuration

General Description

This document details the custom configuration that is programmed into the one time programmable (OTP) memory of the RC22312A002. Please refer to the device datasheet for further information about the device.

Configuration List

Configuration Name	Configuration Index
config0	config_0
config1	config_1
config2	config_2
config3	config_3

Output Frequency Overview

Config Index	OUT0	OUT1	OUT2	OUT3	OUT4	OUT5
config_0	-	-	-	-	-	-
config_1	312.5MHz	312.5MHz	312.5MHz	312.5MHz	312.5MHz	312.5MHz
config_2	-	-	-	-	-	-
config_3	-	-	-	-	-	-

Config Index	OUT6	OUT7	OUT8	OUT9	OUT10	OUT11
config_0	-	-	-	-	-	-
config_1	312.5MHz	312.5MHz	156.25MHz	-	50MHz	50MHz
config_2	-	-	-	-	-	-
config_3	-	-	-	-	-	-

Configuration Selection Overview: Static Multi Config

Config Slot	Config Selection 1	Config Selection 0	Config Index
slot_0	GPIO1 Low	GPIO0 Low	config_0
slot_1	GPIO1 Low	GPIO0 High	config_1
slot_2	GPIO1 High	GPIO0 Low	config_2
slot_3	GPIO1 High	GPIO0 High	config_3

Serial Interface Configuration

Config Index	Serial Port Configuration
config_0	I2C (1-byte address), 7-bit address: 0 0 0 1 A2 A1 A0

config_1	I2C (1-byte address), 7-bit address: 0 0 0 1 A2 A1 A0
config_2	I2C (1-byte address), 7-bit address: 0 0 0 1 A2 A1 A0
config_3	I2C (1-byte address), 7-bit address: 0 0 0 1 A2 A1 A0

I2C Address Selection Bits

Config Index	I2C Address Bit A2	I2C Address Bit A1	I2C Address Bit A0
config_0	GPIO4 (PIN 63)	SDO (PIN 7)	nCS (PIN 6)
config_1	GPIO4 (PIN 63)	SDO (PIN 7)	nCS (PIN 6)
config_2	GPIO4 (PIN 63)	SDO (PIN 7)	nCS (PIN 6)
config_3	GPIO4 (PIN 63)	SDO (PIN 7)	nCS (PIN 6)

GPIO Startup Configuration

Pin Number	GPIO	Function Description
62	GPIO0	CONFIG_SEL0
41	GPIO1	CONFIG_SEL1
40	GPIO2	N/A
36	GPIO3	N/A
63	GPIO4	I2C_ADDR2
49	GPIO5	N/A
45	GPIO6	N/A
2	LOCK	N/A

VDD Pins

Property	Value
VDD_VCO	1.8V
VDDXO_DCD	1.8V
VDDD33_SERIAL	3.3V
VDDD33_DIA	1.8V
VDD_CLK	1.8V
VDDO0	1.8V
VDDO1_FOD0	1.8V
VDDO2	1.8V
VDDO3	1.8V
VDDO4	1.8V
VDDO5	1.8V
VDDO6	1.8V
VDDO7	1.8V

VDDO8_FOD1	1.8V
VDDO9	1.8V
VDDO10_FOD2	1.8V
VDDO11	1.8V

config0 (config_0) General Overview

Property	Value
Serial Interface	I2C (1-byte address), 7-bit address: 0 0 0 1 A2 A1 A0
Operation Mode	Synthesizer
External EEPROM Load	Disabled
XIN	625/8
Crystal CL	8.24pF
VCO Frequency	10.625GHz
CLKIN0	DISABLED
CLKIN1	DISABLED
CLKIN2	DISABLED
CLKIN3	DISABLED
APLL Loop BW	~832.0527kHz
Lock BW	~64.6167Hz
Acquire BW	~9.3048kHz

config0 (config_0) GPIO Settings

Pin Number	GPIO	Function Description	Internal PU	Internal PD	Output Drive Strength
62	GPIO0	General purpose input (input)	Enable	Disable	N/A
41	GPIO1	General purpose input (input)	Enable	Disable	N/A
40	GPIO2	General purpose input (input)	Enable	Disable	N/A
36	GPIO3	APLL LF lock (VCTRL-based lock) (output)	Enable	Disable	CMOS Output mode and power supply of 1.8V.
63	GPIO4	General purpose input (input)	Enable	Disable	N/A
49	GPIO5	General purpose input (input)	Disable	Enable	N/A
45	GPIO6	General purpose input (input)	Disable	Enable	N/A
2	GPIO8	General purpose input (input)	Enable	Disable	N/A

config0 (config_0) Output Overview

Output	IOD Mux Selection	Frequency	Status	Output Type	Output Boost
OUT0	VCO/2	-	disabled	DISABLED (Hi-Z/Hi-Z)	-
OUT1	VCO/2	-	disabled	DISABLED (Hi-Z/Hi-Z)	-
OUT2	VCO/2	-	disabled	DISABLED (Hi-Z/Hi-Z)	-
OUT3	VCO/2	-	disabled	DISABLED (Hi-Z/Hi-Z)	-
OUT4	VCO/2	-	disabled	DISABLED (Hi-Z/Hi-Z)	-
OUT5	VCO/2	-	disabled	DISABLED (Hi-Z/Hi-Z)	-

OUT6	VCO/2	-	disabled	DISABLED (Hi-Z/Hi-Z)	-
OUT7	VCO/2	-	disabled	DISABLED (Hi-Z/Hi-Z)	-
OUT8	VCO/2	-	disabled	DISABLED (Hi-Z/Hi-Z)	-
OUT9	Static high (Minimal power)	-	disabled	DISABLED (Hi-Z/Hi-Z)	-
OUT10	FOD2	-	disabled	DISABLED (Hi-Z/Hi-Z)	-
OUT11	FOD2	-	disabled	DISABLED (Hi-Z/Hi-Z)	-

Note: All VDDOs need to ramp before or at the same time as other cores power rails.

config1 (config_1) General Overview

Property	Value
Serial Interface	I2C (1-byte address), 7-bit address: 0 0 0 1 A2 A1 A0
Operation Mode	Synthesizer
External EEPROM Load	Disabled
XIN	625/8
Crystal CL	8.24pF
VCO Frequency	10.625GHz
CLKIN0	DISABLED
CLKIN1	DISABLED
CLKIN2	DISABLED
CLKIN3	DISABLED
APLL Loop BW	~832.0527kHz
Lock BW	~64.6167Hz
Acquire BW	~9.3048kHz

config1 (config_1) GPIO Settings

Pin Number	GPIO	Function Description	Internal PU	Internal PD	Output Drive Strength
62	GPIO0	General purpose input (input)	Enable	Disable	N/A
41	GPIO1	General purpose input (input)	Enable	Disable	N/A
40	GPIO2	General purpose input (input)	Enable	Disable	N/A
36	GPIO3	APLL LF lock (VCTRL-based lock) (output)	Enable	Disable	CMOS Output mode and power supply of 1.8V.
63	GPIO4	General purpose input (input)	Enable	Disable	N/A
49	GPIO5	OE[10] (input)	Disable	Enable	N/A
45	GPIO6	OE[11] (input)	Disable	Enable	N/A
2	GPIO8	General purpose input (input)	Enable	Disable	N/A

config1 (config_1) Output Overview

Output	IOD Mux Selection	Frequency	Status	Output Type	Output Boost
OUT0	VCO/2	312.5MHz	enabled	HCSL (internally terminated) Amplitude: 950mV	disabled
OUT1	VCO/2	312.5MHz	enabled	HCSL (internally terminated) Amplitude: 950mV	disabled
OUT2	VCO/2	312.5MHz	enabled	HCSL (internally terminated) Amplitude: 950mV	disabled

OUT3	VCO/2	312.5MHz	enabled	HCSL (internally terminated) Amplitude: 950mV	disabled
OUT4	VCO/2	312.5MHz	enabled	HCSL (internally terminated) Amplitude: 950mV	disabled
OUT5	VCO/2	312.5MHz	enabled	HCSL (internally terminated) Amplitude: 950mV	disabled
OUT6	VCO/2	312.5MHz	enabled	HCSL (internally terminated) Amplitude: 950mV	disabled
OUT7	VCO/2	312.5MHz	enabled	HCSL (internally terminated) Amplitude: 950mV	disabled
OUT8	VCO/2	156.25MHz	enabled	HCSL (internally terminated) Amplitude: 950mV	disabled
OUT9	VCO/2	-	disabled	DISABLED (Hi-Z/Hi-Z)	-
OUT10	FOD2	50MHz	GPIO Control	HCSL (internally terminated) Amplitude: 950mV	disabled
OUT11	FOD2	50MHz	GPIO Control	HCSL (internally terminated) Amplitude: 950mV	disabled

Note: All VDDOs need to ramp before or at the same time as other cores power rails.

config2 (config_2) General Overview

Property	Value
Serial Interface	I2C (1-byte address), 7-bit address: 0 0 0 1 A2 A1 A0
Operation Mode	Synthesizer
External EEPROM Load	Enabled
XIN	625/8
Crystal CL	8.24pF
VCO Frequency	10.625GHz
CLKIN0	DISABLED
CLKIN1	DISABLED
CLKIN2	DISABLED
CLKIN3	DISABLED
APLL Loop BW	~832.0527kHz
Lock BW	~64.6167Hz
Acquire BW	~9.3048kHz

config2 (config_2) GPIO Settings

Pin Number	GPIO	Function Description	Internal PU	Internal PD	Output Drive Strength
62	GPIO0	General purpose input (input)	Enable	Disable	N/A
41	GPIO1	General purpose input (input)	Enable	Disable	N/A
40	GPIO2	General purpose input (input)	Enable	Disable	N/A
36	GPIO3	Device Ready (startup sequence complete) (output)	Enable	Disable	CMOS Output mode and power supply of 1.8V.
63	GPIO4	General purpose input (input)	Enable	Disable	N/A
49	GPIO5	General purpose input (input)	Disable	Enable	N/A
45	GPIO6	General purpose input (input)	Disable	Enable	N/A
2	GPIO8	General purpose input (input)	Enable	Disable	N/A

config2 (config_2) Output Overview

Output	IOD Mux Selection	Frequency	Status	Output Type	Output Boost
OUT0	VCO/2	-	disabled	DISABLED (Hi-Z/Hi-Z)	-
OUT1	VCO/2	-	disabled	DISABLED (Hi-Z/Hi-Z)	-
OUT2	VCO/2	-	disabled	DISABLED (Hi-Z/Hi-Z)	-
OUT3	VCO/2	-	disabled	DISABLED (Hi-Z/Hi-Z)	-
OUT4	VCO/2	-	disabled	DISABLED (Hi-Z/Hi-Z)	-
OUT5	VCO/2	-	disabled	DISABLED (Hi-Z/Hi-Z)	-

OUT6	VCO/2	-	disabled	DISABLED (Hi-Z/Hi-Z)	-
OUT7	VCO/2	-	disabled	DISABLED (Hi-Z/Hi-Z)	-
OUT8	VCO/2	-	disabled	DISABLED (Hi-Z/Hi-Z)	-
OUT9	VCO/2	-	disabled	DISABLED (Hi-Z/Hi-Z)	-
OUT10	VCO/2	-	disabled	DISABLED (Hi-Z/Hi-Z)	-
OUT11	VCO/2	-	disabled	DISABLED (Hi-Z/Hi-Z)	-

Note: All VDDOs need to ramp before or at the same time as other cores power rails.

config2 (config_2) External EEPROM Settings

Property	Value
Part Number	R1EX24064ASA
Address	0x50
Address Size	2-byte address
I2C Speed	100kHz
Length	8KB

config3 (config_3) General Overview

Property	Value
Serial Interface	I2C (1-byte address), 7-bit address: 0 0 0 1 A2 A1 A0
Operation Mode	Synthesizer
External EEPROM Load	Enabled
XIN	625/8
Crystal CL	8.24pF
VCO Frequency	10.625GHz
CLKIN0	DISABLED
CLKIN1	DISABLED
CLKIN2	DISABLED
CLKIN3	DISABLED
APLL Loop BW	~832.0527kHz
Lock BW	~64.6167Hz
Acquire BW	~9.3048kHz

config3 (config_3) GPIO Settings

Pin Number	GPIO	Function Description	Internal PU	Internal PD	Output Drive Strength
62	GPIO0	General purpose input (input)	Enable	Disable	N/A
41	GPIO1	General purpose input (input)	Enable	Disable	N/A
40	GPIO2	General purpose input (input)	Enable	Disable	N/A
36	GPIO3	Device Ready (startup sequence complete) (output)	Enable	Disable	CMOS Output mode and power supply of 1.8V.
63	GPIO4	General purpose input (input)	Enable	Disable	N/A
49	GPIO5	General purpose input (input)	Disable	Enable	N/A
45	GPIO6	General purpose input (input)	Disable	Enable	N/A
2	GPIO8	General purpose input (input)	Enable	Disable	N/A

config3 (config_3) Output Overview

Output	IOD Mux Selection	Frequency	Status	Output Type	Output Boost
OUT0	VCO/2	-	disabled	DISABLED (Hi-Z/Hi-Z)	-
OUT1	VCO/2	-	disabled	DISABLED (Hi-Z/Hi-Z)	-
OUT2	VCO/2	-	disabled	DISABLED (Hi-Z/Hi-Z)	-
OUT3	VCO/2	-	disabled	DISABLED (Hi-Z/Hi-Z)	-
OUT4	VCO/2	-	disabled	DISABLED (Hi-Z/Hi-Z)	-
OUT5	VCO/2	-	disabled	DISABLED (Hi-Z/Hi-Z)	-

OUT6	VCO/2	-	disabled	DISABLED (Hi-Z/Hi-Z)	-
OUT7	VCO/2	-	disabled	DISABLED (Hi-Z/Hi-Z)	-
OUT8	VCO/2	-	disabled	DISABLED (Hi-Z/Hi-Z)	-
OUT9	VCO/2	-	disabled	DISABLED (Hi-Z/Hi-Z)	-
OUT10	VCO/2	-	disabled	DISABLED (Hi-Z/Hi-Z)	-
OUT11	VCO/2	-	disabled	DISABLED (Hi-Z/Hi-Z)	-

Note: All VDDOs need to ramp before or at the same time as other cores power rails.

config3 (config_3) External EEPROM Settings

Property	Value
Part Number	R1EX24064ASA
Address	0x50
Address Size	2-byte address
I2C Speed	100kHz
Length	8KB

Ordering Info

Part Number	Carrier Type
RC22312A002GN1#BB0	Tray
RC22312A002GN1#KB0	Tape and Reel

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