IDT82V2082 Data Sheet Change Notice

Supplemental Information

This notice describes the differences between the updated version (Version 7, dated November 24, 2009) and its previous version (Version 6, dated December 12, 2005) of the IDT82V2082 data sheet. It helps readers to identify the changes when the data sheet is upgraded.

Revision History

Revision Date	PCN Number (if applicable)	Date Code	Changed Items
November 24, 2009	-	-	14
December 12, 2005	-	-	3-13
July 19, 2004	-	-	2
April 9, 2004	T0404-03	ZByyww	1

Changed Items

November 24, 2009

Item 14: Added FPGA81 pinouts. (Page 10, 11, 12, 13, 14, 15, 16, 17, 18, 64, 65, 88)

December 12, 2005

Item 13: Changed the ATAO bit description. (Page 52)

Item 12: Added pin compatible device names. (Page 1)

Item 11: Added green package options (Page 1, 87)

Item 10: Added MCLK requirement for the $\overline{RST}$ pin. (Page 16)

Item 9: Added how to connect JTAG pins when JTAG is not used. (Page 16)

Item 8: Changed Figure-7 (Page 24)

Item 7: Changed notes for Figure-8 (Page 25)

Item 6: Changed 3.8.1 Analog Loopback (Page 34)

Item 5: Changed description for Reset Operation (Page 43)

Item 4: Added setting for reserved registers (Page 44)

Item 3: Added test conditions for Isc (Page 73, 74)

July 19, 2004

Item 2: The line short circuit current is changed from 100 mApp to 100 mA typical. (Page 34, 66, 67)

April 9, 2004

Item 1: In hardware control mode, the control of the TERMn pin is changed. (Page 14, 22, 24, 56)

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