

Supplemental Information

This notice describes the differences between the updated version (Version 19, dated July 1, 2010) and its previous version (Version 18, dated April 26, 2010) of the IDT82V2048 data sheet. It helps readers to identify the changes when the data sheet is upgraded.

Revision History

Revision Date	PCN Number (if applicable)	Date Code	Changed Items
July 1, 2010	-	-	32
April 26, 2010	-	-	31
January 21, 2010	-	-	30
September 11, 2009	-	-	29
March 18, 2009	-	-	28
July 22, 2005	-	-	27 - 26
April 12, 2005	-	-	25 - 6
September 02, 2004	-	-	5 - 2
December 09, 2003	-	-	1

Changed Items

July 1, 2010

Item 32: Updated Section '2.4.6.3 EXZ AND BPV DETECTION IN B8ZS'. (Page 17)

April 26, 2010

Item 31: Updated Section '2.4.6 Error Detection'. (Page 15, 16, 17, 18)

January 21, 2010

Item 30: Updated the pin description about SDO, changed 'In serial write operation, SDO is always in High impedance' to 'In serial write operation, SDO is in high impedance for the first 8 SCLK clock cycles and driven low for the remaining 8 SCLK clock cycles'. (Page 9)

September 11, 2009

Item 29: Changed 'LEN' column to 'TS[2:0]' column in 'Power Consumption' table. (Page 46)

March 18, 2009

Item 28: Updated Figure-12 'External Transmit/Receive Line Circuitry'. (Page 19)

July 22, 2005

Item 27: Updated MCn pin description in Table-1 'Pin Description'. (Page 10)

Item 26: Updated T1 VDDT supply specification in Table-1 'Pin Description', Table-12 'External Component Values', section 'Transmit Driver Power Supply', 'Recommended Operating Conditions' table and 'Power Consumption' table. (Page 11, 18, 19, 45, 46)

April 12, 2005

- Item 25:** Changed 't10' value in 'Serial Host Interface Timing Characteristics' table and added 't10' in Serial Interface Read Timing figures. (Page 58)
- Item 24:** Changed 'A[7:0]' to 'A[4:0]' in Figure - 28, Figure - 30, Figure - 32 and Figure - 34. (Page 54, 55, 56, 57)
- Item 23:** Changed rise/fall time in 'Transceiver Timing Characteristics' table. (Page 50)
- Item 22:** Changed 'IA' value, 'SIR' value, changed 'Note 2' and removed 'Note 1' in 'Receiver Characteristics' table. (Page 48)
- Item 21:** Changed 'Isc' value and 'Note 3' in 'Transmitter Characteristics' table. (Page 47)
- Item 20:** Removed a note about register DF. (Page 32)
- Item 19:** Added the content in 'Digital Loopback' section and 'Analog Loopback' section. (Page 20)
- Item 18:** Changed the headline 'Reset' into 'Software Reset', changed 'Power Up' section into 'Power On Reset'. (Page 20)
- Item 17:** Added 'Transmit Line Side Short Circuit Failure Detection' section. (Page 19)
- Item 16:** Changed 'Power Driver Failure Monitor' section. (Page 19)
- Item 15:** Added a note about 'Transformer Specifications' table. (Page 19)
- Item 14:** Changed LOS Declare/Clear value in 'LOS Condition in Clock Recovery Mode' table and 'Receiver Characteristics' table, added a note in 'LOS Condition in Clock Recovery Mode' table. (Page 15, 48)
- Item 13:** Changed the description about the CLKE pin. (Page 6, 8, 9, 14)
- Item 12:** Updated the interface of MCLK= high & TDNn = pulse and MCLK= clocked & TDNn = pulse in the 'System Interface Configuration (In Host Mode)' table. (Page 14)
- Item 11:** Updated the interface of MCLK= high & TDNn = pulse in the 'System Interface Configuration (In Hardware Mode)' table. (Page 13)
- Item 10:** Moved description of the IC pins to the end of 'Pin Description' table. (Page 11)
- Item 9:** Updated the description of the TCK and TDO pins. (Page 10, 11)
- Item 8:** Changed the headline into 'Hardware/Host Control Interface'. (Page 7)
- Item 7:** Added a headline 'Transmit and Receive Digital Data Interface'. (Page 5)
- Item 6:** Added the green package options. (Page 1, 61)

September 02, 2004

- Item 5:** Added to VDDT 'For T1 applications, 5 V VDDT is recommended'. (Page 11, 19, 45)
- Item 4:** Added 'Note 1' to 'IA (Input Amplitude) max value' in 'Receiver Characteristics' table: For E1, the max limit is 1.5 Vp. (Page 48)
- Item 3:** Removed the note 'I_{p-p}' of the line short circuit current in table 'Transmitter Characteristics'. (Page 15, 47)
- Item 2:** Changed the characteristics of the ternary receive input amplitude, LOS threshold and LOS hysteresis. (Page 15, 48)

December 09, 2003

- Item 1:** Removed the sentence 'The Inband Loopback Code is compatible with the specifications in T1.403, TA-TSY-000312 and TR-TSY-000303'. (Page 23)

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.