Tsi620 Ballmap -- Top View of Pin Assignment (Document 80D7000_PN003_05)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26
A	No Ball	GPIO[0]	GPIO[1]	GPIO[2]	PCI_AD[0]	PCI_AD[4]	PCI_CBEn[0]	PCI_AD[11]	PCI_AD[15]	PCI_STOPn	PCI_FRAMEn	PCI_AD[18]	PCI_AD[22]	PCI_AD[24]	PCI_AD[28]	PCI_PMEn	PCI_GNTn[1]	PCI_RSTn	PCI_INTBn	PCI_ARBEN	PCI_CLKO[0]	I2C_SLAVE	CLKGEN_PLL_AVSS	CLKGEN_PLL_AVDD	I2C_SA[2]	I2C_SA[5]
B	GPIO[3]	VSS_IO	GPIO[4]	GPIO[5]	VSS_IO	PCI_AD[2]	PCI_AD[6]	VSS_IO	PCI_AD[13]	PCI_PAR	VSS_IO	PCI_AD[16]	PCI_AD[20]	VSS_IO	PCI_AD[26]	PCI_AD[30]	VSS_IO	PCI_CLKO[1]	PCI_INTAn	VSS_IO	PCI_CLK	I2C_SA[6]	VSS_IO	I2C_SA[4]	VSS_IO	PCI_PLL_AVSS
C	GPIO[6]	GPIO[7]	GPIO[8]	GPIO[9]	GPIO[10]	PCI_AD[5]	PCI_AD[7]	PCI_AD[9]	PCI_AD[12]	PCI_AD[14]	PCI_TRDYn	PCI_AD[21]	PCI_AD[23]	PCI_IDSEL	PCI_AD[29]	PCI_REQn[2]	PCI_REQn[1]	PCI_CLKO[2]	PCI_INTCn	PCI_RSTDIR	PCI_HOLD_BOOT	I2C_SA[3]	I2C_SCLK	I2C_SD	I2C_SA[0]	PCI_PLL_AVDD
D	GPIO[11]	VSS_IO	GPIO[12]	GPIO[13]	NC	PCI_AD[1]	PCI_AD[8]	VSS_IO	PCI_CBEn[1]	PCI_DEVSELn	VSS_IO	PCI_IRDYn	PCI_CBEn[3]	VSS_IO	PCI_AD[31]	PCI_REQn[3]	VSS_IO	PCI_GNTn[3]	PCI_CLKO[3]	VSS_IO	PCI_PLL_BYPASS	I2C_SEL	NC	TRST_b	VSS_IO	TDI
E	GPIO[14]	GPIO[15]	GPIO[16]	GPIO[17]	GPIO[18]	PCI_AD[3]	PCI_AD[10]	PCI_M66EN	PCI_SERRn	PCI_PERRn	PCI_CBEn[2]	PCI_AD[17]	PCI_AD[19]	PCI_AD[27]	PCI_AD[25]	PCI_REQn[4]	PCI_GNTn[2]	PCI_GNTn[4]	PCI_CLKO[4]	PCI_INTDn	I2C_DISABLE	I2C_MA	I2C_SA[1]	TMS	TDO	TCK
F	GPIO[19]	GPIO[20]	GPIO[21]	GPIO[22]	GPIO[23]	VSS_IO	VDD_PCI	VSS_IO	VDD_PCI	VSS_IO	VDD_PCI	VSS_IO	VDD_PCI	VSS_IO	VDD_PCI	VSS_IO	VDD_PCI	VSS_IO	VDD_PCI	VSS_IO	VDD_PCI	VSS	NC	VSS	VSS	BCE
G	GPIO[24]	VSS_IO	GPIO[25]	VSS_IO	GPIO[26]	VDD_PCI	VSS_IO	VDD_PCI	VSS_IO	VDD_PCI	VSS_IO	VDD_PCI	VSS_IO	VDD_PCI	VSS_IO	VDD_PCI	VSS_IO	VDD_PCI	VSS_IO	VDD_PCI	VSS_IO	BLK_RST_b	VSS_IO	RST_IRQ_b	NC	CHIP_RST_b
H	GPIO[27]	GPIO[28]	GPIO[29]	GPIO[30]	GPIO[31]	VSS_IO	VDD_PCI	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VSS_IO	VDD_PCI	INT_b	SP_CLK_SEL[0]	SP_CLK_SEL[1]	SP_HOST	SP_MAST_EN
J	SP6_RXD[0]	SP6_RXD[1]	SP6_RXD[2]	SP6_RXD[3]	SP6_RXD[4]	VDD_HSTL	VSS_IO	VDD	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VDD_PCI	VSS_IO	VDD_PCI	SP_TX_SWAP	SP_RX_SWAP	SP_IO_SPEED[1]	SP_IO_SPEED[0]
K	SP6_RXD[5]	VSS_IO	SP6_RXD[6]	VSS_IO	SP6_RXD[7]	VSS_IO	VDD_HSTL	VDD	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDD	VSS_IO	VDD_PCI	SP5_PWRDN	VSS_IO	SP4_PWRDN	VSS_IO	SP3_PWRDN
L	SP6_RXCTL[0]	SP6_RXD[8]	SP6_RXD[9]	SP6_RXD[10]	SP6_RXD[11]	VDD_HSTL	VSS_IO	VDD	VDD	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDD	VDD	VDD_PCI	VSS_IO	SP2_PWRDN	SP1_PWRDN	SP6_PWRDN	SP6_MODE_SEL	SP4_MODE_SEL
M	SP6_RXD[12]	SP6_RXD[13]	SP6_RXD[14]	SP6_RXD[15]	SP6_RXCTL[1]	VSS_IO	VDD_HSTL	VDD	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDD	VSS_IO	VDD_PCI	NC	NC	MCES	SP2_MODE_SEL	SP0_MODE_SEL
N	SP6_RXD[16]	VSS_IO	SP6_VREF	VSS_IO	SP6_RXD[17]	VDD_HSTL	VSS_IO	VDD	VDD	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDD	VDD	VDD_PCI	VSS	VSS	VSS	VSS	VSS	VSS
P	SP6_RXCLK	SP6_RXD[18]	SP6_RXD[19]	SP6_RXD[20]	SP6_RXD[21]	VSS_IO	VDD_HSTL	VDD	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDD	VSS	SP_VDD	SP0_RD_n	SP0_RD_p	SP_VDD	SP0_TD_n	SP0_TD_p
R	SP6_RXD[22]	SP6_RXD[23]	SP6_RXCTL[2]	SP6_RXD[24]	SP6_RXD[25]	VDD_HSTL	VSS_IO	VDD	VDD	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDD	SP_AVDD	VSS	VSS	SP_VDD	VSS	VSS	SP_VDD	VSS
T	SP6_RXD[26]	VSS_IO	SP6_RXD[27]	VSS_IO	SP6_RXD[28]	VSS_IO	VDD_HSTL	VDD	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	SP_AVDD	VSS	SP0_RC_p	SP0_RC_n	SP_VDD	SP0_TC_n	SP0_TC_p
U	SP6_RXD[29]	SP6_RXD[30]	SP6_RXD[31]	SP6_RXCTL[3]	SP6_RX_ERROR	VDD_HSTL	VSS_IO	VDD	VDD	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDD	SP_AVDD	VSS	VSS	SP_VDD	SP0_REXT	VSS	SP_VDD	VSS
V	SP6_TXD[0]	SP6_TXD[1]	SP6_TXD[2]	SP6_TXD[3]	SP6_TXD[4]	VSS_IO	VDD_HSTL	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VSS	SP_AVDD	VSS	SP_VDD	SP0_RB_n	SP0_RB_p	SP_VDD	SP0_TB_p	SP0_TB_n
W	SP6_TXD[5]	VSS_IO	SP6_TXD[6]	VSS_IO	SP6_TXD[7]	VDD_HSTL	NC	VDD	VSS	SP_AVDD	SP_AVDD	SP_AVDD	VSS	SP_AVDD	SP_AVDD	SP_AVDD	VSS	SP_AVDD	SP_AVDD	VSS	VSS	SP_VDD	VSS	VSS	SP_VDD	VSS
Y	SP6_TXCTL[0]	SP6_TXD[8]	SP6_TXD[9]	SP6_TXD[10]	SP6_TXD[11]	NC	NC	VSS	SP_AVDD	VSS	VSS	VSS	SP_AVDD	VSS	VSS	VSS	SP_AVDD	VSS	VSS	VSS	VSS	SP0_RA_p	SP0_RA_n	SP_VDD	SP0_TA_p	SP0_TA_n
AA	SP6_TXD[12]	SP6_TXD[13]	SP6_TXCLK	SP6_TXD[14]	SP6_TXD[15]	NC	SP_VDD	VSS	VSS	VSS	SP_VDD	VSS	VSS	VSS	SP_VDD	VSS	VSS	VSS	SP_VDD	VSS	VSS	VSS	VSS	VSS	VSS	VSS
AB	SP6_TXCTL[1]	VSS_IO	SP6_VREF	VSS_IO	SP6_TXD[16]	NC	SP4_RA_p	SP_VDD	SP4_RB_n	SP_VDD	SP4_RC_p	SP_VDD	SP4_RD_p	SP_VDD	SP2_RA_p	SP_VDD	SP2_RB_p	SP_VDD	SP2_RC_n	SP_VDD	SP2_RD_p	VSS	VSS	VSS	VSS	VSS
AC	SP6_TXD[17]	SP6_TXD[18]	SP6_TXD[19]	SP6_TXD[20]	SP6_TXD[21]	NC	SP4_RA_n	VSS	SP4_RB_p	SP4_REXT	SP4_RC_n	VSS	SP4_RD_n	VSS	SP2_RA_n	VSS	SP2_RB_n	SP2_REXT	SP2_RC_p	VSS	SP2_RD_n	VSS	VSS	SP_VDD	VSS	VSS
AD	SP6_TXD[22]	SP6_TXD[23]	SP6_TXCTL[2]	SP6_TXD[24]	SP6_TXD[25]	VSS	SP_VDD	VSS	SP_VDD	VSS	SP_VDD	VSS	SP_VDD	VSS	SP_VDD	VSS	SP_VDD	VSS	SP_VDD	VSS	SP_VDD	VSS	S_CLK_n	VSS	TCK2_n	VSS
AE	SP6_TXD[26]	VSS_IO	SP6_TXD[27]	VSS_IO	SP6_TXD[28]	VSS	SP4_TA_p	SP_VDD	SP4_TB_n	SP_VDD	SP4_TC_p	SP_VDD	SP4_TD_p	SP_VDD	SP2_TA_p	SP_VDD	SP2_TB_n	SP_VDD	SP2_TC_p	SP_VDD	SP2_TD_p	VSS	S_CLK_p	VSS	TCK2_p	VSS
AF	SP6_TXD[29]	SP6_TXD[30]	SP6_TXD[31]	SP6_TXCTL[3]	SP6_PHY_DISABLE	VSS	SP4_TA_n	VSS	SP4_TB_p	VSS	SP4_TC_n	VSS	SP4_TD_n	VSS	SP2_TA_n	VSS	SP2_TB_p	VSS	SP2_TC_n	VSS	SP2_TD_n	VSS	VSS	SP_VDD	VSS	VSS

Note: NC stands for "no connect." If this device has no connect signals they must be left unconnected.

Revision History

August 2009, 80D7000_PN003_05 -- There have been no technical changes to the ballmap. The formatting has been update for IDT.

September 2008, 80D7000_PN003_04 -- Redefined the following pins as follows:

M22	N/C
M23	N/C
J22	VDD_PCI
F22	VSS
F23	N/C
F24	VSS
F25	VSS

October 2007, 80D7000_PN003_03 -- Removed the NDA status on the document. There were no technical changes made to this version.

September 2007, 80D7000_PN003_02 -- Changed the following pins to no connect: D5, D23, G25, W7, Y6, Y7, AA6, AB6, and AC6.