



RENESAS RZ FAMILY The Next-generation embedded processors enable the smart society that makes people's daily lives more comfortable and affluent.



CONTENTS

| Meeting the Diverse and Evolving Needs of Edge Devices | _ 04 | Development Environment for Linux | _ 45 |
|--|------|---------------------------------------|------|
| RZ Family Target Applications | _ 06 | Development Environment for RTOS | _ 46 |
| RZ/V Series | _ 07 | Winning Combinations | _ 48 |
| RZ/N Series | _ 15 | Motor Control Solution | _ 49 |
| RZ/T Series | _ 19 | Industrial Ethernet Solution | _ 50 |
| RZ/G Series | _ 24 | Functional Safety | _ 51 |
| RZ/A Series | _ 36 | RZ Family Ecosystem Partners | _ 52 |
| Development Environment for the RZ Family | _ 43 | Explanation of Orderable Part Numbers | _ 53 |

In recent years, "intelligence at the edge" has been rapidly advancing across various fields that support our daily lives—such as manufacturing, infrastructure, robotics, home appliances, building management, power grids, and transportation.

This trend is driven by the increasing need for advanced processing directly at the field level, including Al-based image analysis, autonomous control, real-time network communication, and intuitive operation enabled by HMI (Human-Machine Interface).

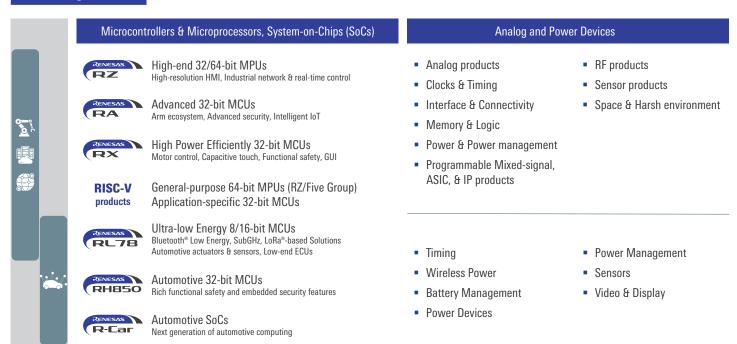
In addition, processing tasks that were traditionally handled by the cloud are now increasingly expected to be performed by edge devices, such as control and terminal equipment.

In order to meet these evolving market needs, Renesas has developed the next-generation RZ family of embedded processors with performance that can meet the advanced processing requirements of edge devices based on reliable peripheral functions and real-time control technologies cultivated through many years of microcontroller development.

The Zenith of the Renesas micro

The ideal choice to meet the requirements of increasingly diverse and sophisticated edge devices — That is the RZ family.

Positioning of the RZ





Meeting the Diverse and Evolving Needs of Edge Devices —— The RZ Family

As application demands become more advanced and varied, the RZ Family delivers a finely tuned blend of processing performance, power efficiency, and peripheral integration, with tailored strengths across each series. This design philosophy enables seamless application across a wide range of edge use cases—Vision AI, industrial networking, real-time control, and human-machine interfaces—providing a best-fit development platform at the edge.

Vision Al



RZ/V Series

Al accelerator Vision processing + Linux

Industrial Network



RZ/N Series

Industrial Ethernet with Redundancy + Linux/ RTOS

Real-time Control



RZ/T Series

Industrial Ethernet Motor drive + Linux/RTOS

IoT Edge & HMI



RZ/G Series

Multimedia / 3D Graphics + Linux

Human Machine Interfaces



RZ/A Series

Large size RAM + RTOS

Vision Al

Renesas own cutting-edge AI technology "DRP-AI" for embedded AI application

Network

TSN and Multi-protocol Industrial network support



Renesas RZ Family

Real-time

High-performance Processing and High Precision Realtime Control

Edge IoT

High-performance CPU and High-speed interfaces for Edge IoT

нмі

High-performance CPU operation and Graphics/Video Processing

Vision AI RZ/V2M RZ/V2H **RZ/V Series** 1.0GHz Dual-core Cortex-A53, 1.8GHz Quad-core Cortex-A55, DRP-AI(576-MAC), 4K-ISP DRP-AI3(4K-MAC), 4K-ISP, 3D-GPU RZ/V2MA RZ/V2N 1.0GHz Dual-core Cortex-A53, DRP-AI(576-MAC), OpenCV Accelerator 1.8GHz Quad-core Cortex-A55, DRP-AI3(2K-MAC), 4K-ISP,3D-GPU RZ/V2L 1.2GHz Dual-core Cortex-A55, DRP-AI(576-MAC), 3D-GPU **Industrial Network** RZ/N2H RZ/N1D RZ/N1S RZ/N2L 1.2GHz Quad-core Cortex-A55 **RZ/N Series** 500MHz Dual-core Cortex-A7, 500MHz Cortex-A7,125MHz Cortex-M3, 400MHz Cortex-R52, 1 OGHz Dual-core Cortex-R52 125MHz Cortex-M3, Industrial Ethernet Industrial Ethernet Industrial Ethernet Industrial Ethernet, 6-axis Motor Control RZ/N1L 125MHz Cortex-M3, Industrial Ethernet **Real-time Control** RZ/T2H **RZ/T2ME** 1.2GHz Quad-core Cortex-A55, 800MHz Dual-core Cortex-R52, **RZ/T Series** 1.0GHz Dual-core Cortex-R52, 2-axis Motor Control, Industrial Ethernet, OTFD 9-axis Motor Control, Industrial Ethernet RZ/T1 RZ/T2M 600MHz Cortex-R4, 150MHz Cortex-M3, 800MHz Dual-core Cortex-R52, 1-axis Motor Control, Industrial Ethernet 2-axis Motor Control, Industrial Ethernet RZ/T2L 800MHz Cortex-R52, 2-axis Motor Control, EtherCAT **IoT Edge RZ/Five** RZ/G3S **RZ/G Series** 1.1GHz Cortex-A55, 250MHz Dual-core Cortex-M33, LPDDR4/DDR4 RISC-V. 1.0GHz AX45MP. DDR4/3L. GbEthernet, CAN-FD HMI RZ/G2H RZ/G3E RZ/A1H RZ/A3M **RZ/G Series** 1.5GHz Quad-core Cortex-A57 + Cortex-A53, 1.8GHz Quad Cortex-A55, 400MHz Cortex-A9, 10MB RAM, 1.0GHz Cortex-A55, LPDDR4, 3DG, H.264/5 LPDDR4/4X, 3DG, NPU LCDC, JPEG, Ethernet, USB Built-in DDR3L 128MB **RZ/A Series** RZ/G2M RZ/G2L RZ/A1M RZ/A2M 400MHz Cortex-A9, 5MB RAM, LCDC, JPEG, Ethernet, USB 528MHz Cortex-A9, 4MB RAM, LCDC, JPEG, MIPI-CSI, Ethernet, USB 1.5GHz Dual-core Cortex-A57 + Cortex-A53, 1.2GHz Dual-core Cortex-A55, LPDDR4, 3DG, H,264/5 DDR4/31 3DG H 264 CAN-FD RZ/G2N RZ/G2LC RZ/A1LU RZ/A3UL 400MHz Cortex-A9, 3MB RAM, LCDC, JPEG, Ethernet, USB 1.0GHz Cortex-A55, DDR4/3L, LCDC, GbEthernet, USB 1.5GHz Dual-core Cortex-A57, LPDDR4, 3DG, H.264/5 1.2GHz Dual-core Cortex-A55, DDR4/3L, 3DG, CAN-FD RZ/G2E RZ/G2UL RZ/A1L 1.2GHz Dual-core Cortex-A53. 400MHz Cortex-A9, 3MB RAM, 1.0GHz Cortex-A55. DDR3L, 3DG, H.264/5 DDR4/3L, CAN-FD, ADC LCDC, Ethernet, USB RZ/G1H RZ/G1N RZ/A1LC 1.4GHz Quad-core Cortex-A15 + Cortex-A7, 1.5GHz Dual-core Cortex-A15, 400MHz Cortex-A9, 2MB RAM, DDR3, 3DG, H.264 DDR3L, 3DG, H.264 LCDC, Ethernet, USB RZ/G1M RZ/G1E 1.5GHz Dual-core Cortex-A15, 1.0GHz Dual-core Cortex-A7, DDR3L, 3DG, H.264 DDR3, 3DG, H.264 Android is a trademark of Google LLC.

RTOS

Linux / Android™ / Multi-OS with RTOS



RZ Family Target Applications

The RZ Family brings new value to customer applications with its high-performance CPU core and various accelerators and peripheral functions.

| | (Main pr | control ocessing, ption) | (Motor/ | ive /inverter trol) | | JI Display ,etc) | (Industria | inication I Network, nmunication) | Proce | raphics essing leo codec) |
|--|----------|--------------------------------|---------|---------------------------|------|---------------------|------------|---|-------|---------------------------------|
| Industrial Automation | RZ/V | RZ/G | RZ/V | RZ/G | RZ/V | RZ/G | RZ/V | RZ/G | RZ/V | RZ/G |
| | RZ/N | RZ/A | RZ/N | RZ/A | RZ/N | RZ/A | RZ/N | RZ/A | RZ/N | RZ/A |
| Inverter, PLC, | RZ/T | | RZ/T | | RZ/T | | RZ/T | | RZ/T | |
| Robot machine tools, etc. | | | | | | | | | | |
| Appliances | RZ/V | RZ/G | RZ/V | RZ/G | RZ/V | RZ/G | RZ/V | RZ/G | RZ/V | RZ/G |
| (a) | RZ/N | RZ/A | RZ/N | RZ/A | RZ/N | RZ/A | RZ/N | RZ/A | RZ/N | RZ/A |
| IH Cooker, Smart Power Tools, Water Pump etc. | RZ/T | | RZ/T | | RZ/T | | RZ/T | | RZ/T | |
| Building Automation | RZ/V | RZ/G | RZ/V | RZ/G | RZ/V | RZ/G | RZ/V | RZ/G | RZ/V | RZ/G |
| | RZ/N | RZ/A | RZ/N | RZ/A | RZ/N | RZ/A | RZ/N | RZ/A | RZ/N | RZ/A |
| HVAC, Elevator, Lighting, | RZ/T | | RZ/T | | RZ/T | | RZ/T | | RZ/T | |
| Fire Alert Unit, etc. Medical & Healthcare | | |] [| 77.0 | | | | | | 77.0 |
| 120 | RZ/V | RZ/G | RZ/V | RZ/G | RZ/V | RZ/G | RZ/V | RZ/G | RZ/V | RZ/G |
| | RZ/N | RZ/A | RZ/N | RZ/A | RZ/N | RZ/A | RZ/N | RZ/A | RZ/N | RZ/A |
| Health Monitor Band, Wearable devices, Blood sugar meter, etc. | RZ/T | | RZ/T | | RZ/T | | RZ/T | | RZ/T | |
| Consumer Electronics | RZ/V | RZ/G | RZ/V | RZ/G | RZ/V | RZ/G | RZ/V | RZ/G | RZ/V | RZ/G |
| | RZ/N | RZ/A | RZ/N | RZ/A | RZ/N | RZ/A | RZ/N | RZ/A | RZ/N | RZ/A |
| Home Entertainment, Power Adapters & Chargers, Wearables, etc. | RZ/T | | RZ/T | | RZ/T | | RZ/T | | RZ/T | |
| Metering & Energy | RZ/V | RZ/G | RZ/V | RZ/G | RZ/V | RZ/G | RZ/V | RZ/G | RZ/V | RZ/G |
| 312 | RZ/N | RZ/A | RZ/N | RZ/A | RZ/N | RZ/A | RZ/N | RZ/A | RZ/N | RZ/A |
| Electricity, Gas, Water, | RZ/T | | RZ/T | | RZ/T | | RZ/T | | RZ/T | |
| Heat Meter Telematics | | | 1 | | | | | | | |
| & Informatics | RZ/V | RZ/G | RZ/V | RZ/G | RZ/V | RZ/G | RZ/V | RZ/G | RZ/V | RZ/G |
| | RZ/N | RZ/A | RZ/N | RZ/A | RZ/N | RZ/A | RZ/N | RZ/A | RZ/N | RZ/A |
| | RZ/T | | RZ/T | | RZ/T | | RZ/T | | RZ/T | |
| Driver monitoring system, etc. Retail, Automation | | |] [| | | | | | | |
| & Payment | RZ/V | RZ/G | RZ/V | RZ/G | RZ/V | RZ/G | RZ/V | RZ/G | RZ/V | RZ/G |
| | RZ/N | RZ/A | RZ/N | RZ/A | RZ/N | RZ/A | RZ/N | RZ/A | RZ/N | RZ/A |
| POS terminals, etc. | RZ/T | | RZ/T | | RZ/T | | RZ/T | | RZ/T | |

RZ/V Series

Features of the RZ/V Series

The RZ/V series is a microprocessor (MPU) that incorporates Renesas' proprietary AI accelerator, Dynamically Reconfigurable Processor (DRP)-AI, which combines high AI inference performance and low power consumption. With a wide range of scalability from 0.5 to 80TOPS, RZ/V provides high added value for your various AI applications.

Furthermore, it is equipped with advanced image processing capabilities, including a 4K-compatible Image Signal Processor (ISP), an OpenCV accelerator (OpenCVA), and a GPU that supports 3D graphics. DRP-AI is the world-class low power AI accelerators achieved up to 10 TOPS/W.

By integrating DRP-AI with image processing functionality, it enables the development of compact products that support real-time AI applications at the endpoint—without the need for cooling fans. This makes them ideal for use in retail, robotics, home appliances, and industrial automation.

Building compact products can handle real-time AI applications without cooling fans for retail, robotics, home appliances and industrial automation.

Vision Al



Al accelerator Vision processing + Linux



Realize high Al performance without Heatsink and FAN *Depending on conditions

RZ/V Development Environment

| Items | Details |
|--------------------------------------|--|
| RZ/V Al Applications (Al Apps) | Al Apps are sets of following software that can be used as is for each-case. Pre-trained Al model objects Pre-build application binary Application source code Users can select the category of applications and access the applications provided on GitHub. |
| RZ/V AI SDK | Binary development environment for AI Applications that is build for specific RZ/V EVK. |
| RZ/V AI SDK Source Code | Source code of RZ/V AI SDK that user can customize Linux environment. |
| RZ/V AI Applications Demo | microSD card image that contains the RZ/V AI Applications. Users can try the AI Applications without having AI SDK environment. |
| RZ/V AI Transfer Learning Tool (TLT) | GUI Tool to re-train the AI models used in RZ/V AI Applications with different datasets. |
| DRP-AI TVM | Machine Learning Compiler plugin for Apache TVM with AI accelerator DRP-AI, which is a tool to compile your own AI models (including BYOM) to get the executable format on RZ/V series. Note: AI SDK also includes DRP-AI TVM. However it is not the latest version. If you would like to use the latest DRP-AI TVM, please follow the guide in DRP-AI TVM Web to construct the environment. |
| Al Navigator (e ² syudio) | A set of plugins for Renesas IDE, e ² studio, that allows users to use following software on GUI environment. RZ/V AI Applications RZ/V AI SDK RZ/V AI TLT DRP-AI TVM |

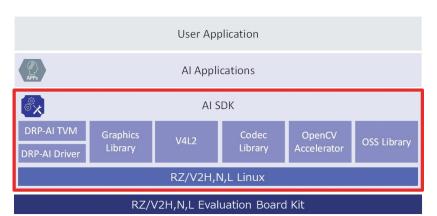


RZ/V AI SDK

AI Applications and AI SDK are quick and easy solutions for starting AI.

It provides various Al applications for free.

- AI SDK is pre-build S/W environment designed for RZ/V Evaluation Board Kits
- AI SDK source code is also available to support the customization requirements for the boards other than RZ/V Evaluation Board Kit and/or Linux environment
- AI SDK supports RZ/V2L, RZ/V2N and RZ/V2H

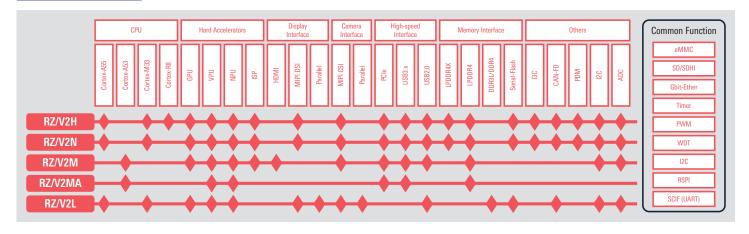


Renesas RZ/V AI Web https://renesas-rz.github.io/rzv_ai_sdk/latest/



Al Applications You can find the Al application you need! Agriculture Healthcare Smart Home Smart City Smart Building Industrial Retail

RZ/V Series Lineup





RZ/V2M Group: Dual Cortex-A53, DRP-AI 1TOPS, 4K HW ISP

The AI hardware IP, <u>DRP-AI</u>, configured with <u>DRP</u> and AI-MAC, combines both a high-speed AI inference and low power consumption and realizes 1TOPS/W class power performance. In addition, the image signal processor (ISP) is highly robust, producing a stable image independent of the environment, allowing for a high AI recognition accuracy. With these features, the RZ/V2M realizes low power consumption, which is a challenge for embedded devices, making heat dissipation measures easier. Since heat sinks and cooling fans are no longer needed, the equipment can be miniaturized and the BOM cost can be reduced. The result is that it is ideal for vision AI applications in a wide range of embedded markets, including surveillance security, retail, office automation (OA), industrial automation, robotics, and healthcare. In addition, the RZ/V2M also features abundant high-speed communication interfaces such as USB 3.1, PCI-Express, Gigabit Ethernet, and many CPU peripheral functions, so it can also be used in a variety of applications.

CPU core

- Arm® Cortex®-A53, Dual-core Max. operating frequency: 1.0GHz Memory interface
- 32bit LPDDR4 memory interface
- eMMC 4.5.1 × 1 channel
- mSDIO × 2 channel
 NPU: DRP-AI: 1TOPS
 ISP (Image signal processor): Up to 4K
 Camera interface: MIPI-CSI2 × 2
 channel

Display interface: HDMI 1.4a

Video codec

- Encoding: H.265 up to 2160p30, H.264 up to 1080p60
- Decoding: H.265 up to 2160p30, H.264 up to 1080p60

2D Graphics Engine: 200MPixels/s High Speed interface

- Gigabit Ethernet × 1 channel
- USB3.1 × 1 channel (Host/Function)
- PCIe Gen2 (2-lane)

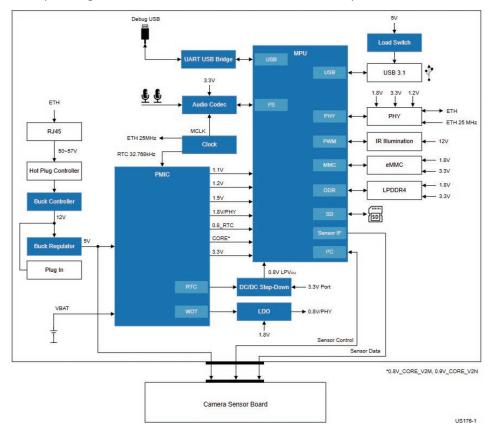
Package

■ FCBGA, 15mm × 15mm, 0.5mm pitch, 841 pins

| System | C | PU | Peripheral I/F |
|----------------------------------|-----------------------------------|---|-------------------------|
| JTAG debugger (CoreSight™) | Arm® Cortex®-A53: 1GHz | Arm® Cortex®-A53: 1GHz | 2 × SD |
| DMAC (16ch) | Neon™ FPU | Neon™ FPU | 1 × PCle Gen2 (2-lane) |
| Power control | L1 I\$: 32KB L1 D\$: 32KB | L1 I\$: 32KB L1 D\$: 32KB | Gbit Ethernet MAC (1ch) |
| | L2\$: ! | 512KB | 1 × USB3.1 Gen1 |
| Timers | | | (Host/Peripheral) |
| 32 × Timer | | nories | 4 × I2C |
| 16 × PWM | RAMA 200KB | RAMB 1MB | 6 × CSI |
| 2 × WDT | Sensing an | 2 × UART | |
| | Al-accelera | tor (DRP-AI) | GPIO |
| Image Sensor I/F MIPI CSI-2 v1.2 | General Processing Accelerator | Multi-target detection (Face, Person's body) | |
| (4-lane, 2ch) | | | External Memory I/F |
| Disculsor I/F | | I Graphics | 1 × LPDDR4-3200 32-bit |
| Display I/F | Camera ISP | 2D Graphics engine | 1 × eMMC |
| 1 × HDMI + PHY | H.264/265 Multi Codec | JPEG Codec | |
| Audio I/F | Sec | Security | |
| 1 × I2S | Trusted | Secure IP | ADC (20ch,12-bit) |

■ High-Performance Monitoring Camera

This AI-enabled surveillance camera features a dynamically reconfigurable processor (DRP) engine, boosting Vision AI performance. It boasts a platform for enhanced features such as password-protected connections, voice alarms, and motion detection with support for Ethernet or USB video streaming. With 4K 30fps image processing and advanced digital noise reduction (2D and optional 3D), the system ensures superior clarity, reducing graininess and enhancing visibility in low-light conditions—critical for AI-based surveillance and analysis.



- High-performance surveillance camera MPU-based design offers AI processing with DRP-AI, enabling high performance with low power consumption and a low-power standby mode.
- Wide dynamic range, custom image settings (saturation, brightness, contrast, sharpness), and black level correction optimize footage for Al detection, ensuring high performance even in challenging lighting conditions.
- Power over Ethernet (PoE) streamlines setup and enables flexible deployment, while Ethernet protocol (100/1000Mbps) ensures high-speed data transmission for reliable and high-resolution streaming.
- Reduced power structure size enables compact camera designs and easy integration into systems without bulky infrastructure.
- Al-based video analytics can monitor crowd movement, congestion patterns, and dwell times for insights.





RZ/V2L Group: Dual Cortex-A55, DRP-AI 0.5TOPS, 5Mp SW ISP

RZ/V2L is equipped with an Arm® Cortex®-A55 (1.2GHz) CPU and built-in Al accelerator "DRP-Al" for vision, which is Renesas' original technology. "DRP-Al" is configured with DRP and Al-MAC. It also has a 16-bit DDR3L/DDR4 interface and a built-in 3D graphics engine with Arm Mali-G31 and video codec (H.264).

DRP-Al's excellent power efficiency eliminates the need for heat dissipation measures such as heat sinks or cooling fans. Al can be implemented cost efficiently not only in consumer electronics and industrial equipment but also in a wide range of applications such as point-of-sale (POS) terminals for retail. Also, the DRP-AI provides both real-time Al inference and image processing functions with the capabilities essential for camera support such as color correction and noise reduction. This enables customers to implement Al-based vision applications without requiring an external image signal processor (ISP).

The RZ/V2L is also package- and pin-compatible with the RZ/G2L. This allows RZ/G2L users to easily upgrade to the RZ/V2L for additional AI functions without

needing to modify the system configuration, keeping migration costs low.

Video codec

CPU core

- Arm® Cortex®-A55, Dual-core/ Single-core
- Max. operating frequency: 1.2GHz Arm® Cortex®-M33, Single-core

Max. operating frequency: 200MHz Memory interface

- 16bit DDR3L/DDR4 memory interface
- eMMC 4.5.1 × 1 channel
- SDIO × 1 channel

NPU: DRP-AI: 0.5TOPS

Camera interface: MIPI CSI2 or Parallel I/ F × 1 channel

Display interface: MIPI DSI or Parallel I/ $F \times 1$ channel

3D Graphics Engine: Arm® Mali™-G31 High Speed interface ■ Gigabit Ethernet × 2 channel ■ USB2.0 × 2 channel (Host only ×1, Host/Function ×1)

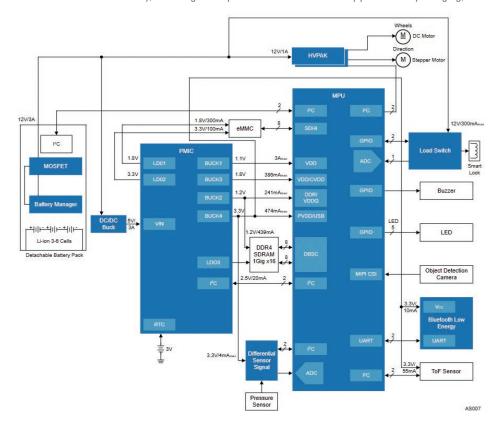
■ Encoding: H.264 up to 1080p30 Decoding: H.264 up to 1080p30

- Package BGA, 15mm × 15mm, 0.5mm pitch, 456 pins
- BGA, 21mm × 21mm, 0.8mm pitch, 551 pins

| System | (| PU | | Interfaces |
|------------------------------------|------------------------------|-------------------------------------|-----------------|---|
| Arm® Debugger (CoreSight™) | | m® Cortex®-A55: 1.2GHz JEON™ VFP | | 1 × DDR3L/DDR4-1600 16-bit (In line ECC) |
| Arm® TrustZone® | L1 I\$: 32KB w/Parity L | 1 I\$: 32KB w/Parity | Arm® | 1 × SPI Multi I/O (8-bit DDR) |
| 16 × DMAC | L1 D\$: 32KB w/ECC L2\$: 0KB | 1 D\$: 32KB w/ECC L2\$: 0KB | Cortex® -M33 | 1 × SDHI(UHS-I)/MMC 1 × SDHI(UHS-I) |
| Interrupt Controller | L3\$: 256KB v | w/ECC | 200MHz | 1 × USB2.0 Host |
| PLL/SSCG | Al Accelerator | Memory | | 1 × USB2.0 Host / Function |
| Standby (Sleep/Software/Module) | DRP-AI | RAM 128KB v | v/ECC | 2 × 100/1000Mbps Ether MAC |
| | | | | |
| Timers | 3D GPU | Camera In | 1 | 4 × I2C |
| 1 × 32-bit MTU3 | Arm Mali™-G31 | (MIPI-CSI2 4-lane, | Parallel) | 2 × SCI 8/9-bit |
| 0 4013 MITHO | H.264 Enc/Dec | Display Ou | t | 5 × SCIF(UART) |
| 8 × 16-bit MTU3 | 1920 × 1080 @ 30fps | (MIPI-DSI 4-lane, | Parallel) | 3 × RSPI |
| 8 × 32-bit PWM | | Image Scaling | Unit | 2 × CAN-FD |
| 3 × WDT | Securit | y (option) | | GPI0 |
| | Secure Boot | Device Uniqu | e ID | Audio |
| Analog | Crypto Engine | JTAG Disab | le | 4 × SSI (I2S) |
| 8 × 12-bit ADC | TRNG | OTP 4K-bi | t | 1 × SRC |

Smart Travel Bag

This smart traveling follow-me bag system is revolutionizing the travel industry by offering hands-free convenience, especially beneficial for elderly travelers, children, and pregnant women. The bag's advanced features include an Al accelerator, object detection, and motion detection, allowing it to autonomously follow its owner. Additionally, the design incorporates a detachable battery pack for easy charging, enhancing practicality and user-friendliness.



- Built-in AI accelerator DRP-AI for vision in the MPU enables intelligent object detection and tracking.
- HVPAK[™] programmable mixed-signal matrix for multi-axis motor drive ensures smooth bag
- Accurate object detection for reliable performance.
- Sensor signal conditioner for precise weight detection using pressure sensing.
- SmartBond TINY™ Bluetooth® Low Energy module for smartphone connectivity.
- Alarm and LED fault indications for low battery, tracking loss, and other critical notifications.



RZ/V2MA Group: Vision AI Accelerator Dual Cortex-A53, DRP-AI 1TOPS

DRP-AI utilizes an AI accelerator consisting of a Dynamically Reconfigurable Processor (DRP) and AI-MAC that accelerates AI inference to achieve both high-speed AI inference and low power consumption, enabling real-time image AI without heat sinks or cooling fans. In addition, the OpenCV accelerator, which takes advantage of DRP technology featuring high flexibility, enables high-speed image processing outside of AI in addition to image preprocessing for AI inference, all on a single chip.

These features enable smaller devices and lower BOM costs for vision Al applications in a wide range of embedded markets, including surveillance security, industrial automation, and healthcare.

CPU core

- Arm® Cortex®-A53, Dual-core Max. operating frequency: 1.0GHz Memory interface
- 32bit LPDDR4 memory interface
- eMMC 4.5.1 × 1 channel
- SDIO × 2 channel NPU: DRP-AI: 1TOPS OpenCV accelerator: DRP

Video codec

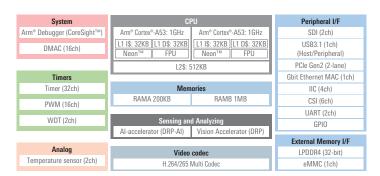
- Encoding: H.265 up to 2160p, H.264 up to 1080p
- Decoding: H.265 up to 2160p, H.264 up to 1080p

High Speed interface

- Gigabit Ethernet × 1 channel
- USB3.1 × 1 channel (Host/Function)
- PCIe Gen2 (2-lane)

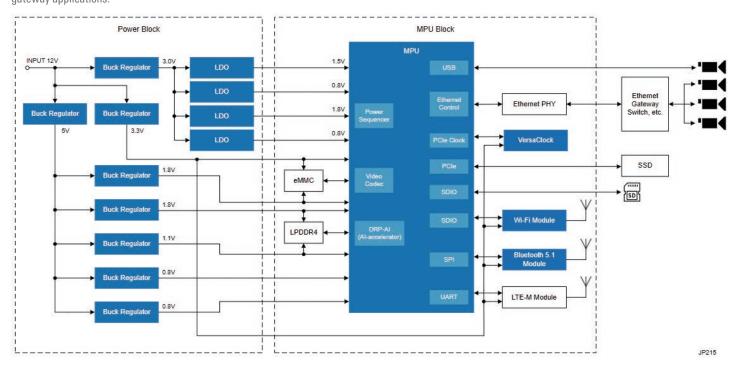
Package

■ FCBGA, 15mm × 15mm, 0.5mm pitch, 841 pins



■ Vision AI Gateway

Renesas' Vision AI Gateway design expertly manages vision data from multiple cameras, performing high-speed AI processing. It features an AI MPU with extensive peripheral functions and an optimized power supply system, achieving high performance and low power consumption and enhancing the value of gateway applications.



- Fast vision Al processing by decoding video streams (H.264 or H.265) and handling multiple Al inferences with minimal switching overhead.
- Supports high-speed vision gateway functionality with Ethernet protocol at 100/1000Mbps and USB 3.1 Gen1 (5Gbps) for fast connections.
- Offers peripheral extension capabilities with PCI Express® 2.0 (Gen2 / 2 Lane).
- The MPU includes a built-in power sequencing control function, simplifying power supply design and enhancing reliability.
- Integrates various communication devices, including a high-performance Wi-Fi module, a compact Bluetooth® Low Energy (LE) module, and an LTE Cat-M1 cellular IoT module.





RZ/V2H Group: Quad Cortex-A55, Dual Cortex-R8, DRP-AI3 80TOPS

The RZ/V2H high-end AI MPU boasts Renesas' proprietary dynamically reconfigurable processor AI accelerator (DRP-AI3), quad Arm® Cortex®-A55 (1.8GHz) Linux processors, and dual Cortex®-R8 (800MHz) real-time processors. Furthermore, the RZ/V2H also includes another dynamically reconfigurable processor (DRP). This processor can accelerate image processing, such as OpenCV, and dynamics calculations required for robotics applications. It also features high-speed interfaces like PCle®, USB 3.2, and Gigabit Ethernet, making it an ideal microprocessor for applications such as autonomous robots and machine vision in factory automation, where advanced AI processing must be implemented with low power consumption.

CPU core

- Arm® Cortex®-A55, Quad-core Max. operating frequency: 1.8GHz
- Arm® Cortex®-R8, Dual-core Max. operating frequency: 800MHz
- Arm® Cortex®-M33, Single-core Max. operating frequency: 200MHz Memory interface
- 32bit × 2 LPDDR4/4X memory interface
- eMMC 4.5.1 × 1 channel
- SDIO × 2 channel NPU: DRP-AI3: 8TOPS/dense, 80TOPS/

sparse
OpenCV accelerator: DRP

ISP (Image signal processor): Up to 4K Camera interface: MIPI CSI-2 × 4

channel

Display interface: MIPI DSI \times 1 channel

Video codec

- Encoding: H.265 up to 2160p30, H.264 up to 1080p60
- Decoding: H.265 up to 2160p30, H.264 up to 1080p60

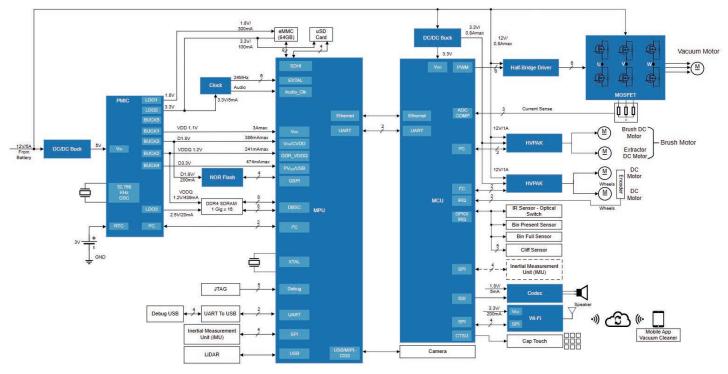
3D Graphics Engine: Arm® Mali™-G31 High Speed interface

- Gigabit Ethernet × 2 channel
- USB3.2 × 2 channel (Host only)
- USB2.0 × 2 channel (Host only ×1, Host/Function ×1)
- PCIe Gen3 (4-lane) × 1 channel Package
- BGA, 19mm × 19mm, 0.5mm pitch, 1368 pins

| System | | CPU | | | Interfaces |
|---------------------------------|--|---|--------------|------------------|--|
| Arm® Debugger | Arm® Cortex®-A55 Ouad 1.8GHz | Arm® Cortex®- Dual 800MH | | ortex®-M33 | LPDDR4/4X w/ECC 32-bit × 2 (12.8GB/s × 2) |
| Arm® Trust Zone® | Quau 1.00112 | | | | xSPI (4, 8-bit DTR) |
| Interrupt Controller PLL / SSCG | L1:(I=32KB+D=32KB)/core L3:1MB | L1:(I=32KB+D=32KB)/ TCM:(I=128KB+D=128KE | | FPU extension | SDIO + eMMC × 1ch SDIO × 2ch |
| Standby | | | | | USB3.2 (Gen2 × 1) - Host × 2ch |
| DMAC 80ch Event Link Controller | Int | ernal Shared N | • | | USB2.0 - Host / Func. × 1ch - Host × 1ch |
| EVOITE EITIK OOTHI OHGI | | | | | Gb Ethernet × 2ch |
| Timers GPT × 16ch | Al Accerelat | or | DRP | | PCIe Gen3 4-lane × 1/2-lane × 2 |
| RTC | DRP-AI3 Dynamically Reconfigurable Processor | | IRQ × 16ch | | |
| GTM (32-bit × 8ch) | | | | | NMI |
| | 1 | /ideo and Grap | hics | | I3C × 1ch |
| CMTW (32-bit × 8ch) | GPU [Mali™ G31] | (option) ISP | [Mali™ C55] | (option) | I2C × 9ch |
| WDT × 4ch | Camera IN: MIPI CSI-2 (1/2/ | 4-lane) x 4ch H | 264/265 End | : /Dec | SCIF × 1ch |
| | Display OUT: MIPI DSI (1/2/ | | mage Scaling | a Unit | RSCI(UART/SPI/I2C host) × 10ch |
| Audio | Display OUT. WIFT DSI (1/2/ | 4-idile) X ICII | maye scann | y Ullit | RSPI × 3ch |
| SSI (I2S) TDM × 10ch | | | | | CAN-FD × 6ch |
| SPDIF × 3ch | | Security IP (op | tion) | | GPIO × 86port |
| SCU / ADMAC | Secure Boo | ot | Device Uniqu | ue ID | Analog |
| ADG | Crypto Engine | | JTAG Disa | ble | 12-bit 2.5Msps ADC × 8ch |
| PDM (input) × 6ch | TRNG | | OTP 32K-I | bit | Temp. Sensor × 2ch |

■ Smart Robot Vacuum Cleaner

This robot vacuum cleaner is a smart cleaning device designed to clean floors and carpets without human intervention. It is equipped with autonomous features like environment mapping, anti-drop, obstacle detection, climbing, and auto-recharge. It implements simultaneous localization and mapping (SLAM) using LiDAR positioned on top of its body. Moreover, its infrared sensor assists in detecting and avoiding obstacles in its path. Additional control can be achieved through a mobile app or voice assistant.



- Powerful Arm® Cortex®-A55 core paired with DRP-Al accelerator builds a virtual map of the room using LiDAR-based SLAM.
- HVPAK reduces BOM count and complexity for brushed motor drive.
- Pre-certified Wi-Fi module enables cloud connectivity with minimal development time and power consumption.



RZ/V2N Group: Quad Cortex-A55, DRP-AI3 15TOPS, 4K HW ISP

The RZ/V2N is a vision AI microprocessor (MPU) with Renesas' proprietary AI accelerator (DRP-AI3) supporting up to 15TOPS AI performance. Its CPUs are quad Arm® Cortex®-A55 (1.8GHz) and Arm Cortex-M33 (200MHz). The RZ/V2N is equipped with an ISP (Image Signal Processor) and dual-channel MIPI® CSI-2® camera interfaces for supporting dual camera signal processing, which is crucial for realizing vision systems. It is also equipped with high-speed interfaces such as PCIe® and USB 3.2, allowing for the expansion of external devices. The RZ/V2N is an ideal microprocessor for applications requiring both low power consumption and advanced AI inference, such as DMS (Driver Monitoring System), monitoring cameras, mobile robots, and more.

CPU core

- Arm® Cortex®-A55, Quad-core Max. operating frequency: 1.8GHz
- Arm® Cortex®-M33, Single-core Max. operating frequency: 200MHz Memory interface
- 32bit LPDDR4/4X memory interface
- eMMC 4.5.1 × 1 channel
- SDIO × 2 channel

NPU: DRP-AI3: 4TOPS/dense, 15TOPS/sparse

ÖpenCV accelerator: DRP-AI3* ISP (Image signal processor): Up to 4K Camera interface: MIPI CSI-2 × 2 channel

Display interface: MIPI DSI \times 1 channel

Video codec

- Encoding: H.265 up to 2160p30, H.264 up to 1080p60
- Decoding: H.265 up to 2160p30, H.264 up to 1080p60

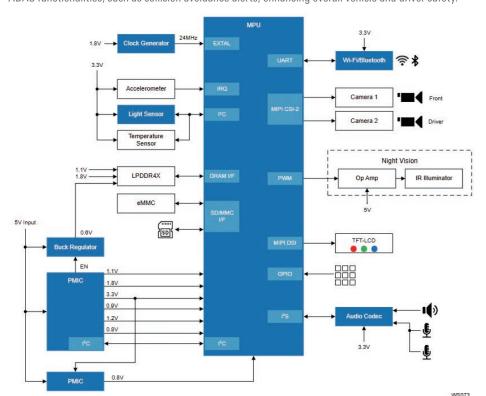
3D Graphics Engine: Arm® Mali™-G31 High Speed interface

- Gigabit Ethernet × 2 channel
- USB3.2 × 1 channel (Host only)
- USB2.0 × 1 channel (Host/Function ×1)
- PCle Gen3 (2Lane) × 1 channel Package
- BGA, 15mm × 15mm, 0.5mm pitch, 840 pins
- * Exclusive operation with AI inference

| System | CPU | | Interfaces |
|---|------------------------------------|--------------------------|--|
| Arm® Debugger | Arm® Cortex®-A55 | Arm® Cortex®-M33 | LPDDR4/4X w/ECC |
| Arm® Trust Zone® | Quad 1.8GHz | 200MHz | 32-bit × 1 (12.8GB/s × 1) xSPI (4, 8-bit DTR) |
| Interrupt Controller | L1:(I=32KB+D=32KB)/core | FPU | SDIO + eMMC × 1ch |
| PLL / SSCG | L3:1MB | DSP extension | SDIO × 2ch |
| Standby | | | - SDIO: V3.0/DHS-1 - eMMC: JEDEC 4.5.1 |
| DMAC 80ch | Men | nory | USB3.2 (Gen2 × 1) - Host × 1ch |
| Event Link Controller | RAM 1.5N | /IB w/ECC | USB2.0 - Host / Func. × 1ch |
| Timers | | | Gb Ethernet × 2ch |
| GPT × 16ch | Al Acce | PCIe Gen3 2-lane × 1 | |
| RTC | DRP | DRP-AI3 | |
| GTM (32-bit × 8ch) | | | NMI |
| . , , , , , , , , , , , , , , , , , , , | Video and | Graphics | I3C × 1ch |
| CMTW (32-bit × 8ch) | GPU [Mali™ G31] (option) | ISP [Mali™ C55] (option) | I2C × 9ch |
| WDT \times 4ch | Camera IN: MIPI CSI-2 4-lane × 2ch | H.264/265 Enc./Dec. | SCIF × 1ch |
| | Display OUT: MIPI DSI 4-lane × 1ch | | RSCI(UART/SPI/I2C host) × 10cl |
| Audio | Display OUT: MIPT DSI 4-lane × Tch | Image Scaling Unit | RSPI × 3ch |
| SSI (I2C) TDM × 10ch | | | CAN-FD × 6ch |
| SPDIF × 3ch | Security I | P (option) | GPIO × 86port |
| ASRC / ADMAC | Secure Boot | Device Unique ID | Analog |
| ADG | Crypto Engine | JTAG Disable | 12-bit 2.5Msps ADC × 24c |
| PDM (input) × 6ch | TRNG | OTP 32K-bit | Temp. Sensor × 2ch |

Al Dash Camera

The demand for consumer and commercial dash cameras is rising globally, driven by increasing mandates for vehicle safety features. Dash cameras serve various applications, including accident recording for liability protection, rideshare and fleet monitoring, and enhanced driver safety. The integration of AI further expands their capabilities, enabling advanced driver assistance systems (ADAS), higher-resolution video processing, and real-time intelligent analytics. This AI-powered dash camera system utilizes a high-performance vision AI MPU with a power-efficient AI accelerator to deliver superior video quality and advanced AI-driven features, such as license plate recognition, facial detection, and long-range object detection. Its high computational efficiency enables ADAS functionalities, such as collision avoidance alerts, enhancing overall vehicle and driver safety.



- Great AI performance with exceptional thermal efficiency and low-power AI processing using DRP-AI for real-time vision inference.
- Dual camera support enables a front-facing ADAS camera and cabin-facing driver monitoring system (DMS) for enhanced situational awareness.
- Low power standby mode extends operational time with a connected accelerometer for instant system wakeup and recording upon detecting impacts or motion, ensuring critical events are captured.
- HMI integration supports touch control, LCD, and voice control, offering an intuitive, versatile, and hands-free user experience.



RZ/V Series Specification

| Items | RZ/V2H | RZ/V2N | RZ/V2L | RZ/V2M | RZ/V2MA |
|---|---|---|--|---|---|
| Main CPU | Cortex-A55 × 4 Cortex-R8 × 2 | Cortex-A55 × 4 | Cortex-A55 × 2 | Cortex-A53 × 2 | Cortex-A53 × 2 |
| Sub CPU | Cortex-M33 | Cortex-M33 | Cortex-M33 | _ | _ |
| Al Accelerator Performance (DRP-AI) | 10 TOPS/W Max. 80 TOPS (Sparse model) Resnet50: 830 Inference/Sec | 10 TOPS/W Max. 15 TOPS (Sparse model) Resnet50: 455 Inference/Sec | 1 TOPS/W Max. 0.5 TOPS Resnet50: 17 Inference/Sec | 1 TOPS/W Max. 1 TOPS Resnet50: 28 Inference/Sec | 1 TOPS/W Max. 1 TOPS Resnet50: 28 Inference/Sec |
| ISP for Camera | 4K ISP (option) (hardware) | 4K ISP (option) (hardware) | Simple ISP (software) | 4K ISP (hardware) | _ |
| MIPI CSI-2 I/F | 4-lane × 4ch | 4-lane × 2ch | 4-lane × 1ch | 4-lane × 2ch | _ |
| Computer Vision Accelerator | OpenCV Accelerator | OpenCV Accelerator | OpenCV Accelerator | _ | OpenCV Accelerator |
| Video Codec | H.265, H.264 | H.265, H.264 | H.264 | H.265, H.264 | H.265, H.264 |
| Graphics | 3D Graphics (option) | 3D Graphics (option) | 3D Graphics | 2D Graphics | _ |
| Package | 1368-pin FCBGA, 19mm × 19mm 0.5mm ball pitch | 840-pin FCBGA, 15mm × 15mm 0.5mm ball pitch | 551-pin PBGA, 21mm × 21mm 0.8mm ball pitch 456-pin PBGA, 15mm × 15mm 0.5mm ball pitch | 841-pin FCBGA, 15mm × 15mm 0.5mm ball pitch | 841-pin FCBGA, 15mm × 15mm 0.5mm ball pitch |

Features of ISP

Supports ISP function to realize Vision System

ISP Comparison Table

| | Item | RZ/V2H | RZ/V2N | RZ/V2L | RZ/V2M |
|---------------|---------------------------|------------------------------|------------------------------|--|---|
| ISP | | H/W ISP Arm Mali™-C55 ISP | H/W ISP Arm Mali™-C55 ISP | S/W ISP Simple ISP by DRP library | H/W ISP 3rd party IP |
| Maximum Resol | ution | Up to 4K | Up to 4K | Up to 5M | Up to 4K |
| Support CMOS | Sensor | User's choice | User's choice | User's choice | Select from IMX415, IMX462, IMX568, AR1335 |
| Camera I/F | | 4× MIPI CSI-2 (4-lane) | 2× MIPI CSI-2 (4-lane) | 1× MIPI CSI-2 (4-lane), 1× Parallel | 2× MIPI CSI-2 (4-lane) |
| | ISP H/W Specifications | ✓ | ✓ | ✓ | _ |
| Dolivorobloo | Driver/API Specifications | ✓ | ✓ | ✓ | ✓ |
| Deliverables | Software | ✓ | √ | ✓ | ✓ |
| | Image Tuning Tool | ✓ | ✓ | ✓ | ✓ |

ISP Function

| Item | RZ/V2H | RZ/V2N | RZ/V2L | RZ/V2M |
|---|--|--|------------------------|--|
| Support Image Size | 3840 × 2160 p × 30 fps × 2 1920 × 1080 p × 60 fps × 2 | 3840 × 2160 p × 30 fps 1920 × 1080 p × 30 fps × 2 | 1920 × 1080 p × 15 fps | 3840 × 2160 p × 30 fps 1920 × 1080 p × 30 fps × 2 |
| AE (Auto Exposure), AWB (Auto White Balance) | ✓ | ✓ | ✓ | ✓ |
| Black Level Correction | √ | √ | ✓ | ✓ |
| Demosaic | √ | ✓ | ✓ | ✓ |
| Flicker Correction | ✓ | ✓ | | ✓ |
| Obtain Focus Analysis Results | √ | ✓ | | ✓ |
| Tone Mapping Settings | ✓ | ✓ | | ✓ |
| Wide Dynamic Range Correction | √ | √ | | ✓ |
| Chromatic Aberration Correction | √ | √ | √ | ✓ |
| Purple Fringing Correction | √ | ✓ | | ✓ |
| Shading Correction | √ | √ | | ✓ |
| Sharpness Correction | √ | ✓ | ✓ | ✓ |
| 2D Noise Reduction | √ | √ | ✓ | ✓ |
| 3D Noise Reduction | √ | ✓ | ✓ | |
| JPEG Conversion | | | | ✓ |
| Resize | ✓ (Downscale only) | ✓ (Downscale only) | ✓ (Downscale only) | ✓ |

RZ/N Series

Features of the RZ/N Series

The Arm®-based RZ/N series MPUs offer scalable and high-performance communication features, supporting multiple industrial Ethernet protocols—including TSN—and redundant networking. With a built-in Gigabit switch and rich peripheral interfaces, they simplify integration into industrial Ethernet systems.

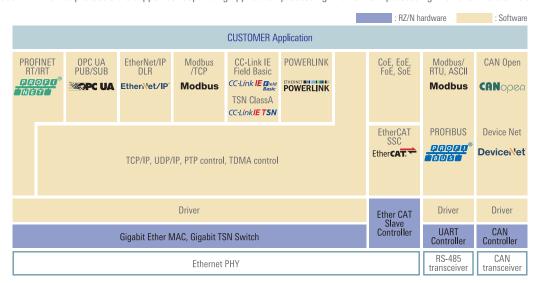
Industrial Network



Industrial Ethernet with Redundancy + Linux/ RTOS

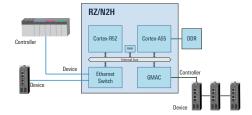
1. Provides optimized microprocessors for a variety of industrial network applications

- The RZ/N2H is optimized for industrial controller equipment such as PLC, DCS, CNC and motion controller. It integrates Quad Arm® CortexR-A55 cores (1.2GHz) for application processing and two Arm Cortex-R52 cores (1.0GHz) for real-time control. The flexible Ethernet functionalities supporting TSN execute both industrial Ethernet controller and device. Also, RZ/N2H can support up to 6-axis motor control, suitable for applications requiring multi-axis.
- The RZ/N2L is optimized for the role of dedicated network companion chip, simplifying the task of adding network functionality to industrial equipment. Since it handles network-related processing independently of the external CPU, Industrial Ethernet support can be implemented without the need to make major changes to the existing application software.
- 2. Integrated Ethernet switch and EtherCAT slave controller alongside support for major Industrial Ethernet protocols and TSN
- A wide range of Industrial Ethernet protocols are supported. Separating application processing and network processing allows for more efficient application control.

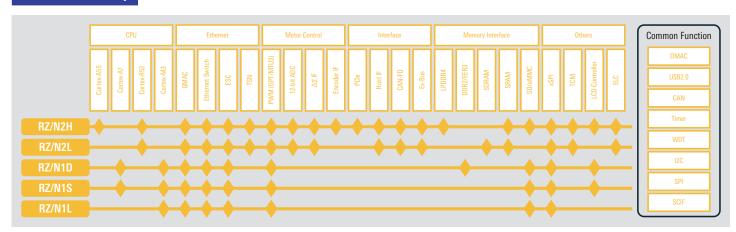


3. Flexible Ethernet Connectivity with RZ/N2H

 RZ/N2H features four Ethernet ports, three GMACs, an Ethernet switch, and an EtherCAT Sub-device Controller (ESC), enabling flexible support not only for industrial Ethernet devices but also for controllers. With a high-performance quad-core Arm Cortex-A55 and LPDDR4 memory, it can run Linux applications, making it an ideal MPU for industrial controller equipment such as PLCs.



RZ/N Series Lineup







Interfaces

LPDDR4-3200 32-bit

2ch SD/eMMC

Industrial Ethernet Switch w/ TSN

4x Ethernet ports

EtherCAT Slave Controller

2ch PCle Gen3

1ch USB2.0

Serial Host II

14ch Encoder IF

3ch I2C

2ch CAN-FD

4ch SPI

RZ/N2H Group: Industrial Ethernet, Linux Application and Real-Time Control in one chip

Renesas RZ/N2H group is high-end MPUs for Industrial Automation that offer high performance computing power for Linux application and high-speed real-time processing power with the capability of Industrial Ethernet and up to 6-axis motor control. The N2H group is suitable for industrial controller equipment such as PLC, DCS, CNC and motion controllers, and multi-axis motor control applications, such as industrial robots.

CPU core

- Arm® Cortex®-A55, Quad/Dual/ Single-core
 Max operating frequency: 1.2GHz
 L1 I/D-cache 32KB per core, L3 cache
 1MB
- Arm® Cortex®-R52, Dual-core Max operating frequency: 1.0GHz L1 I/D-cache 16KB, Tightly Coupled Memory (TCM): 512KB (w/ ECC) + 64KB (w/ ECC) per core

Features

- On-chip system SRAM 2.0MB (w/ ECC)
- LPDDR4-3200 32-bit
- SD/eMMC
- Motor Control Peripherals (Support up to 6-axis)
 - PWM Timer: MTU3 9ch PWM Timer: GPT 56ch $\Delta\Sigma$ interface: 23ch
 - 12-bit ADC: 3units

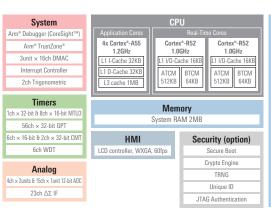
- Encoder IF: 14ch
- Trigonometric function unit
- Industrial Ethernet
- Ethernet Switch w/ TSN
- 3ch Gigabit Ethernet MAC w/ TSN
- 4× Ethernet ports
- EtherCAT Slave Controller (ESC)
- PCI Express Gen3
- Serial host interface
- LCD Controller
- CAN-FD
- USB2.0
- SPI, SCI, I²C
- xSPI

Safety functions

- Register write protection, input clock oscillation stop detection, and CRC
- Isolated peripheral function access via MPU

Package

- 576-pin FCBGA (21mm × 21mm, 0.8mm pitch)
- Tj = -40°C to +125°C

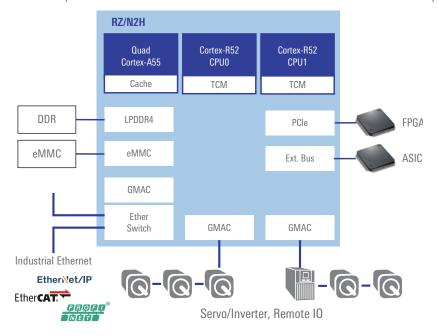


■ PLC (Programable Logic Controller) and Motion Controller

RZ/N2H is suitable for PLC and Motion Controller, which require multi-network support including Industrial Ethernet controller and device, such as EtherCAT®, Ethernet/IP™, PROFINET®.

The Cortex®-A55 Quad core have High Application Processing Power to execute Linux applications such as user-defined sequence processing and Industrial

Dual Cortex-R52 have High Real-time Performance to support Industrial Ethernet device required for standalone PLC and motion controller. High-Speed Connectivity such as PCIe or External Bus to FPGA or custom ASIC which often used for backplane bus or proprietary network.





RZ/N2L Group: Easily Implement Industrial Ethernet and TSN on Industrial Systems

RZ/N2L is an Ethernet communication microprocessor (MPU) that enables customers to easily implement industrial Ethernet and TSN in various IoT and industrial applications like drives, gateways, remote IO and more.

RZ/N2L has functions such as an advanced 3-port Gigabit Ethernet switch with TSN, EtherCAT® slave controller, and supports major industrial Ethernet protocols such as EtherCAT, PROFINET RT/IRT, EtherNet/IPTM, and OPC UA.

RZ/N2L is optimized for network companion chip use-cases. It easily connects to existing systems through its parallel or serial host interface without requirement of major changes.

CPU core

- Arm® Cortex®-R52
 Max operating frequency: 400MHz
 L1 I/D-cache 16KB
 Tightly Coupled Memory (TCM):
 128KB (w/ ECC) + 128KB (w/ ECC)
- Features
- On-chip system SRAM 1.5MB (w/ ECC)
- TSN support
- 3-port Gigabit Ethernet switch
- EtherCAT Slave controller
- Parallel host/serial host interface
- PWM timer
- ∆∑ interface
- ADC

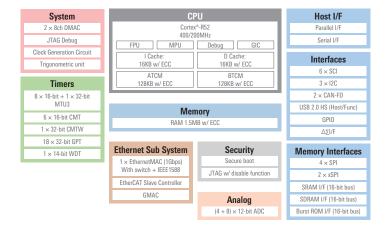
- Trigonometric function unit
- CAN-FD
- USB2.0
- SPI, SCI, I²C
- xSPI

Safety functions

- Register write protection, input clock oscillation stop detection, and CRC
- Isolated peripheral function access via MPII

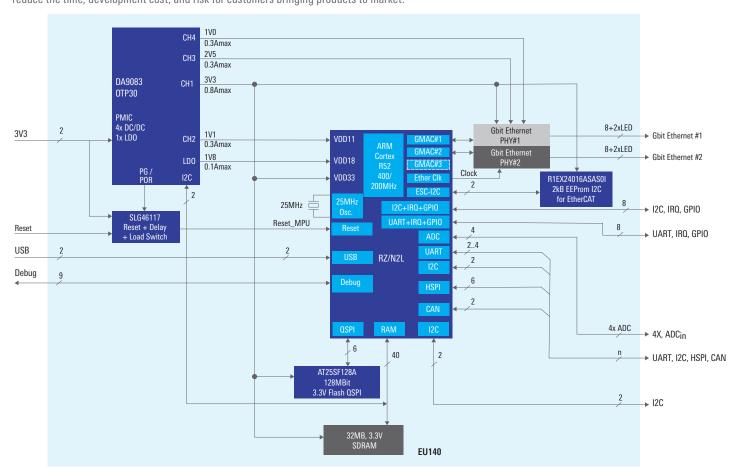
Package

- 225-pin FBGA (13mm × 13mm, 0.8mm nitch)
- 128-pin FBGA (10mm × 10mm, 0.8mm pitch)
- $T_j = -40^{\circ}C \text{ to } +125^{\circ}C$



■ Industrial Gigabit Ethernet System-on-Module

There is increasing demand in the industrial equipment market for MPU-based system on module (SoM) products that offer advanced functionality and compact size, enabling customers to build their own peripheral devices. This solution, which includes an SoM and carrier board, is designed to substantially reduce the time, development cost, and risk for customers bringing products to market.





RZ/N2 Specification

| Item | RZ/N2H | RZ/N2L |
|---------------------|--|--|
| Application Core | Cortex-A55 1.2GHz ×4 | _ |
| Realtime Core | Cortex-R52 1.0GHz ×2 | Cortex-R52 400MHz |
| DDR | LPDDR4-3200 32-bit | - |
| Industrial Ethernet | 4 Ether ports 3 GMAC Ethernet Switch ESC, TSN | 3 Ether ports 1 GMAC Ethernet Switch ESC, TSN |
| Motor Control | Up to 6-axis | - |
| PCle | PCIe (Gen3) ×2 | _ |
| HMI | Parallel RGB | _ |
| Host IF | Serial | Serial / Parallel |
| Package | FCBGA 576-pin (23mm × 23mm) | FBGA 225-pin (23mm × 23mm) FBGA 121-pin (10mm × 10mm) |

RZ/T Series

Features of the RZ/T Series

The Arm®-based RZ/T series MPUs deliver fast real-time control and high-performance application processing with industrial Ethernet communication to build high-performance systems for a wide range of industrial motor control equipment from servos to multi-axis robots. Equipped with encoder interfaces, RZ/T MPUs can support various encoder protocols.

- RZ/T2H is a high-end MPU equipped with a high-performance quad-core Cortex-A55 @1.2GHz for application processing, two high-speed real-time Cortex-R52 cores @1GHz, and peripherals capable of controlling up to 9-axis motors. It also supports both Industrial Ethernet controller and device functions.
- RZ/T2M and RZ/T2ME are equipped with two Cortex-R52 cores @800MHz and support motor control
 of up to 2 axes as well as various Industrial Ethernet devices. RZ/T2ME supports OTFD for security
 enhancement.
- RZ/T2L is equipped with a single Cortex-R52 core @800MHz and supports motor control of up to 2
 axes as well as EtherCAT communication.

■ High-Performance, High-Speed Real-Time Control

- The Real-time core Cortex-R52 equipped with large Tightly Coupled Memory (TCM) minimizes execution time variation by avoiding cache-related fluctuations.
- Motor control peripherals are placed on the LLPP (low latency peripheral port) bus for faster CPU access.
- TFU accelerates trigonometric functions processing.
- Supports multi-protocol absolute encoders such as A-format™, EnDat 2.2, and BiSS-C®, HIPERFACE DSL and FA-Coder, enabling faster and more precise position control.
- Motor control peripheral scalability: RZ/T2H supports up to 9 axes, whereas RZ/T2M, RZ/T2ME, and RZ/T2L support up to 2 axes.

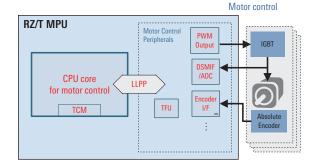
■ High Application-Processing Power and Real-Time Performance

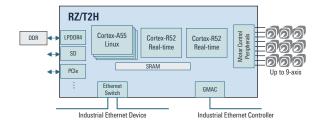
- RZ/T2H is an advanced high-end microprocessor (MPU) equipped with Quad Arm®
 Cortex®-A55 cores (1.2GHz) for application processing and two Arm Cortex-R52 cores (1.0GHz)
 for real-time control.
- LPDDR4-3200 (32-bit) support provides high-speed and large-capacity memory, allowing flexible implementation of Linux, RTOS, or BareMetal software.
- Enables control of up to 9 motor axes while flexibly supporting industrial Ethernet devices and controllers, with compatibility for next-generation TSN.
- Rich Peripheral Set Including PCIe Gen3 (2ch), SD/eMMC, CAN-FD, and LCD Controller.

Real-time Control

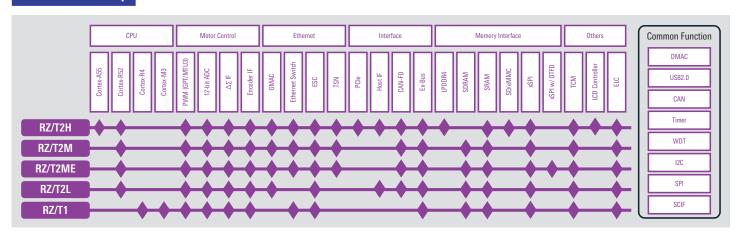


Industrial Ethernet Motor drive + Linux/RTOS





RZ/T Series Lineup







RZ/T2H Group: Up to 9 axes control, Industrial Ethernet and Linux Application in one chip

Renesas RZ/T2H group is high-end MPUs for Industrial Automation that offer high performance computing power for Linux application and high-speed real-time processing power with capability of up-to 9 axes motor control and multiple Industrial Ethernet. The T2H group is suitable for industrial robots with multi-axis control and controller applications such as PLC, DCS, CNC and motion controllers.

CPU core

- Arm® Cortex®-A55, Quad/Dual/ Single-core
 Max operating frequency: 1.2GHz
 L1 I/D-cache 32KB per core, L3 cache
 1MB
- Arm® Cortex®-R52, Dual-core Max operating frequency: 1.0GHz L1 I/D-cache 16KB, Tightly Coupled Memory (TCM): 512KB (w/ ECC) + 64KB (w/ ECC) per core

Features

- On-chip system SRAM 2.0MB (w/ ECC)
- LPDDR4-3200 32-bit
- SD/eMMC
- Motor Control Peripherals (Support up to 9-axis)
 - PWM Timer: MTU3 9ch - PWM Timer: GPT 56ch
 - $-\Delta\Sigma$ interface: 30ch - 12-bit ADC: 3units - Encoder IF: 16ch
 - Trigonometric function unit

- Industrial Ethernet
 - Ethernet Switch w/ TSN
- 3ch Gigabit Ethernet MAC w/ TSN
- 4× Ethernet ports
- EtherCAT Slave Controller (ESC)
- PCI Express Gen3
- Serial host interface
- LCD Controller
- CAN-FDz
- USB2.0
- SPI, SCI, I²C
- xSPI
- Safety functions
- Register write protection, input clock oscillation stop detection, and CRC
- Isolated peripheral function access via MPU

Package

729-pin FCBGA (23mm × 23mm, 0.8mm pitch)

AC 100~200\

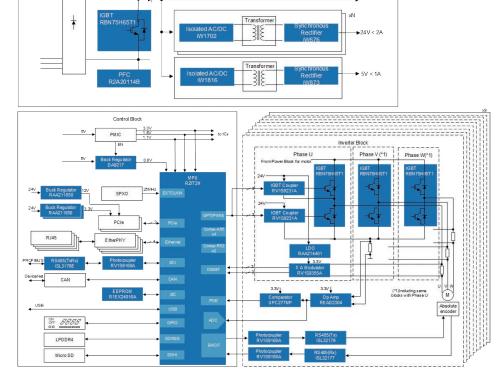
■ Tj = -40°C to +125°C

| System | | Inter | faces | | | |
|---------------------------------------|-----------------------------|-----------------------------------|-----------------------|---------------------------|------------------|--|
| Arm® Debugger (CoreSight™) | Application Cores | Application Cores Real-Time Cores | | | 200 32-bit | |
| Arm® TrustZone® | 4× Cortex®-A55 C | ortex®-R52 1.0GHz | Cortex®-R52 1.0GHz | 2ch | xSPI | |
| 3unit × 16ch DMAC | | D-Cache 16KB | L1 I/D-Cache 16KB | 2ch SD | /eMMC | |
| Interrupt Controller | L1 D-Cache 32KB ATO | CM BTCM | ATCM BTCM | Industrial Ethern | et Switch w/ TSN | |
| 2ch Trigonometric | L3 cache 1MB 512 | KB 64KB | 64KB 512KB 64KB | 3ch GMAC w/ TSN | | |
| Timers | | 4× Ethernet ports | | | | |
| 1ch × 32-bit & 8ch × 16-bit MTU3 | Memory | | | EtherCAT Slave Controller | | |
| 56ch × 32-bit GPT | System | n RAM 2MB | | 2ch PCle Gen3 | | |
| 6ch × 16-bit & 2ch × 32-bit CMT | нмі | | Security | 1ch USB2.0 | | |
| 6ch WDT | LCD controller, WXGA, 60fps | | Secure Boot | 4ch SPI | 3ch I2C | |
| | | 1 | Crypto Engine | 18ch SCI | 2ch CAN-FD | |
| Analog | TRNG | | External Bus | | | |
| 4ch × 2units & 6ch × 1unit 12-bit ADC | | | Unique ID | Serial | Host IF | |
| 30ch ΔΣ IF | | JTA | G Authentication | 16ch En | coder IF | |

To Moto

■ 9-Axis Industrial Motor Control with Ethernet

The system integrates the MPU with peripheral devices, minimizing the need for external components. The MPU's dual Arm® Cortex®-R52 cores enable high-precision motor control and facilitate industrial Ethernet communication. It provides high-precision current sensing through the MPU's delta-sigma ($\Delta\Sigma$) interface and $\Delta\Sigma$ modulator and supports various encoder types with an MPU encoder interface and RS-485 connectivity. The MPU's quad Arm Cortex-A55 cores perform advanced arithmetic processing, including trajectory formation for 9-axis motor control. The system supports major industrial Ethernet protocols, such as EtherCAT®, Ethernet/ IP™, PROFINET®, and OPC Unified Architecture (OPC UA), with a simple configuration requiring minimal external components. A functional safety system can be easily built using the MPU and one MCU for mutual monitoring. Renesas provides reference circuits and a variety of sample programs to assist in implementation.



Power Block





1: RZ/T2ME group further support UDP/IPv4 1step E2E TC

RZ/T2M & RZ/T2ME Group:

High-performance MPU Realizing High-speed High Precision Control for real time control

RZ/T2M&T2ME is an industry-leading high-performance multi-function MPU that realizes high-speed processing, high precision control, and functional safety required for industrial equipment such as AC servos and industrial motors.

Powered by dual Arm® Cortex®-R52 cores with a maximum frequency of 800MHz for real-time control and embedded with a large tightly coupled memory (576KB) directly connected to the CPU to realize high-performance real-time processing, enables low latency access by arranging the peripherals for motor control to the LLPP (Low Latency Peripheral Port) that is directly connected to the CPU.

RZ/T2M&T2ME realizes high speed and highly precise motor control and industrial Ethernet communication such as EtherCAT, PROFINET RT/IRT and EtherNet/IP on a single chip.

CPU core

Arm® Cortex®-R52 x 2
 Max operating frequency: 800MHz
 L1 I/D-cache 16KB
 Tightly Coupled Memory (TCM):
 512KB (w/ ECC) + 64KB (w/ ECC)

Features

- On-chip system SRAM 2MB (w/ ECC)
- Low latency peripheral port (LLPP) bus
- TSN support
- 3-port Gigabit Ethernet switch
- EtherCAT Slave controller
- IEEE1588 UDP/IPv4 1-step E2E TC*
- Encoder interface
- PWM timer
- ∆∑ interface
- ADC
- Trigonometric function unit
- CAN-FD
- USB2.0

- SPI, SCI, I²C
- xSPI (Octa/Quad)
- xSPI (Octa/Quad) w/ On-The-Fly-Decryption (OTFD)*
- Functional safety support up to SIL3 Safety functions
- Register write protection, input clock oscillation stop detection, and CRC
- Isolated peripheral function access via MPII

Package

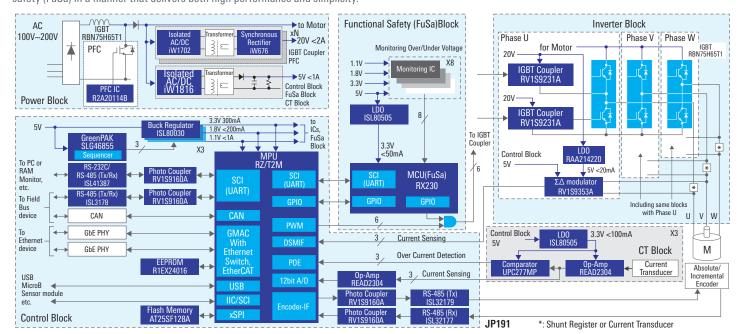
- 320-pin FBGA (17mm × 17mm, 0.8mm pitch)
- 225-pin FBGA (13mm × 13mm, 0.8mm pitch)
- 176-pin LQFP (24mm × 24mm, 0.5mm pitch)
- 128-LQFP (20mm × 14mm, 0.5mm pitch)
- Tj = -40°C to +125°C
- * Supported only by RZ/T2ME

Interfaces System Cortex®-R52 Cortex®-R52 2 × 16ch DMA $6 \times SCI$ 800/400/200MHz 800/400/200MHz JTAG Debug 2 × 12C FPU MPU Debug GIC FPU MPU Debug GIC 2 × CAN-FD Clock Generation Circuit I-cache 16KB w/ ECC 16KB w/ ECC 16KB w/ ECC D-cache 16KB w/ ECC USB 2.0 HS (Host/Func) ATCM BTCM 512KB w/ ECC 64KB w/ ECC GP10 Security ΛΣΙ/Ε Secure boot (option) Memory JTAG w/ disable function **Memory Interfaces** BAM 2MB w/ ECC **Ethernet Sub System Timers** SRAM I/F (32-bit bus) 8 × 16-bit + 1 × 32-bit MTU3 1 × EthernetMAC (1Gbps) With switch + IEEE1588* SDRAM I/F (32-bit bus) 6 × 16-bit CM1 EtherCAT Slave Controlle Burst ROM I/F (32-bit bus) 1 × 32-bit CMTW GMAC Interface 18 × 32-bit GPT 2 × 14-bit WDT

Analog

■ Motor Control System with Industrial Network and Functional Safety

This is a total solution for an industrial motor control system composed of a variety of devices such as MPUs, MCUs for cross monitoring, power ICs, and delta-sigma modulators. Combining these devices makes it possible to implement a variety of functions required for motor control, industrial networks, and functional safety (FuSa) in a manner that delivers both high performance and simplicity.







RZ/T2L Group: High-Performance MPU for Real-Time Control with EtherCAT

RZ/T2L is high-performance MPU that realizes high-speed and high-precision real-time control with EtherCAT. RZ/T2L has Arm® Cortex®-R52 @Max Frequency 800MHz and the large tightly coupled memory size (576 KB) is directly connected to the CPU, reducing the fluctuation in execution time that can occur when cache memory is used, and delivering deterministic and fast-response processing.

RZ/T2L has seamless hardware architecture with RZ/T2M such as CPU core, peripheral functions and LLPP (Low Latency Peripheral Port) bus, and can be proposed for higher performance control systems such as AC servo.

Also, RZ/T2L offers a scalable and compatible software platform with Renesas MPUs and

MCUs. It enables customer utilizing their software assets for new model development.

CPU core

Arm® Cortex®-R52
 Max operating frequency: 800MHz
L1 I/D-cache 16KB
 Tightly Coupled Memory (TCM):
512KB (w/ ECC) + 64KB (w/ ECC)

Features

- On-chip system SRAM 1MB (w/ ECC)
- Low latency peripheral port (LLPP)
- EtherCAT Slave controller
- Gigabit Ether MAC
- Encoder interface
- PWM timer
- Δ∑ interface
- ADC
- Trigonometric function unit

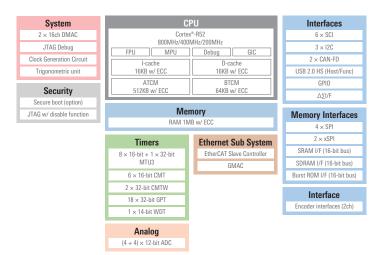
- Serial host interface
- xSPI (Octa/Quad)
- CAN-FD
- USB 2.0
- SPI, SCI, I²C
- Offering functional safety software up to SIL3

Safety functions

- Register write protection, input clock oscillation stop detection, and CRC
- Isolated peripheral function access via MPII

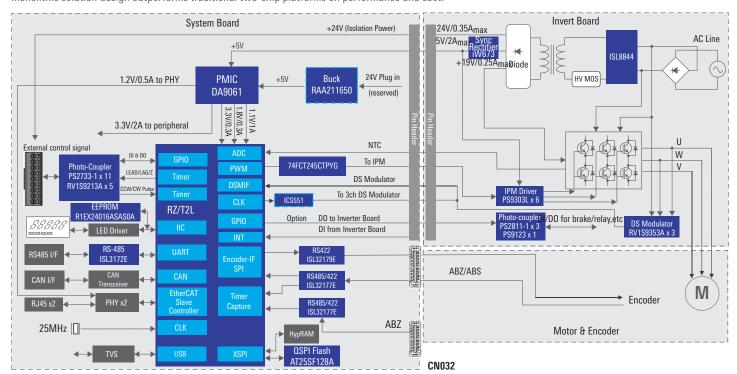
Package

- 196-pin FBGA (12mm × 12mm, 0.8mm nitch)
- $T_i = -40$ °C to +125°C



AC Servo

This Renesas AC servo solution integrates motor control and EtherCAT design to support high-speed and high-precision motor control through synchronizing time-sensitive industrial Ethernet communications. This solution is composed of three blocks: system control, power drive and motor encoder, which are physically isolated while maintaining a high degree of interconnect. By utilizing the high-performance RZ/T2M or RZ/N2L or RZ/T2L microprocessor, this monolithic solution design outperforms traditional two-chip platforms on performance and cost.



RZ/T2 Specification

| | Item RZ/T2H | | RZ/T2ME | RZ/T2M | RZ/T2L | |
|------------------------|--------------------------------|--|--|--|----------------------------|--|
| Application Cor | е | Cortex-A55 1.2GHz ×4 | _ | _ | - | |
| Realtime Core | | Cortex-R52 1.0GHz ×2 | Cortex-R52 800MHz ×2 | Cortex-R52 800MHz ×2 | Cortex-R52 800MHz | |
| DDR | | LPDDR4-3200 32-bit | _ | _ | _ | |
| Industrial Ethernet | | 4 Ether ports 3 GMAC Ethernet Switch ESC, TSN | 3 Ether ports 1 GMAC Ethernet Switch ESC, TSN | 3 Ether ports 1 GMAC Ethernet Switch ESC, TSN | ESC | |
| | GPT/MTU (for motor control) | 56ch/9ch (Up to 9-axis) | 7ch/9ch (2-axis) | 7ch/9ch (2-axis) | 7ch/9ch (2-axis) | |
| Motor Control | Sigma Delta I/F | 30ch | 6ch | 6ch | 6ch | |
| | Absolute Encoder I/F | 16ch | 2ch | 2ch | 2ch | |
| PCIe | | PCIe (Gen3) ×2 | _ | _ | _ | |
| HMI | | Parallel RGB | _ | _ | _ | |
| On-The-Fly-Dec | ryption | _ | Supported | _ | _ | |
| Host IF | | Serial | _ | _ | Serial | |
| Package | | FCBGA 729-pin (23mm × 23mm) | FBGA 320-pin (17mm × 17mm) FBGA 225-pin (13mm × 13mm) | FBGA 320-pin (17mm × 17mm) FBGA 225-pin (13mm × 13mm) LQFP 176-pin (24mm × 24mm) LQFP 126-pin (14mm × 20mm) | FBGA 196-pin (12mm × 12mm) | |



RZ/G Series

Features of the RZ/G Series

The RZ/G series is a scalable MPU platform based on the Arm® Cortex® architecture and RISC-V architecture with advanced graphics, video engine and high-speed interface. The scalable and efficient performance of the RZ/G series is ideal for industrial automation, building automation HMI, industrial cameras, and IoT Edge applications.

IoT Edge & HMI





Multimedia / 3D Graphics + Linux

■ Yocto Based Linux Solution Overview

- Linux BSP Plus Support LTS Kernel: Long Term Support Kernel
 For experts who want to start development with the latest Kernel
- Verified Linux Package (VLP)
 Support SLTS Kernel: Super Long Term Support Kernel
 For users who requires super long-term Linux Kernel maintenance
- Software Development Kit (SDK)
 All-in-one package including application frameworks and VLP
 For Linux beginners who want to start Application software development early

SDK (Software Development Kit) Application framework VLP (Super long-term maintenance) Linux BSP Plus Middleware Linux BSP

RZ/G Series Lineup

| | | | CPU | | | Hard | Acceler | ators | | Display | Interface | 9 | | nera rface | ŀ | igh-spee | ed e | | Memory | Interfac | 9 | | | Others | | | Common Function |
|------------------------------|------------|------------|------------|------------|-----------|----------|----------|----------|----------|----------|-----------|----------|----------|---------------|----------|----------|---------|-----------|--------------|----------|----------|----------|----------|----------|----------|----------|--------------------------------|
| | Cortex-A57 | Cortex-A53 | Cortex-A55 | Cortex-M33 | Cortex-R7 | GPU | VPU | NPU | HDMI | MIPI DSI | SDAT | Parallel | MIPLCSI | Parallel | PCle | SATA | USB3.x | LPDDR4/4X | LPDDR4 | DDR4 | DDR3L | 13C | Ex-Bus | PDM | ASRC | ADC | USB2.0 Gbit-Ether CAN-FD |
| RZ/G2H RZ/G2M | X | + | | | * | * | * | | * | | † | * | † | * | † | + | * | | * | _ | _ | | † | | † | | SD/SDHI Serial-Flash Timer |
| RZG2N RZ/G2E RZ/G3E | | + | + | + | ¥ | X | X | + | | + | X | X | X | X | X | | X | + | | | + | + | ¥ | + | ¥ | _ → | PWM WDT |
| RZ/G2L RZ/G2LC RZ/G2UL | | | X | * | | * | + | | | X | | + | * | + | | | | | | X | X | | | | | * | RSPI SCIF |
| RZ/G3S | | | ¥ | ¥ | | | | | | | | | | | + | | | | + | | | + | | | | → | 128 |



3 × SPDIF

10 × ASRC

RZ/G3E Group: 1.8GHz Quad Cortex-A55, LPDDR4/4X, 3DG, NPU

RZ/G3E is a microprocessor (MPU) integrated with quad CPU and NPU in one chip, improving power efficiency, reliability, and security for human machine interface (HMI) applications. The RZ/G3E offers rich HMI functions including graphics engine (GPU), video codec, multi-screen full HD output, and Neural Processing Unit (NPU) for edge computing functions. In addition to the Cortex-A55 quad core delivering a powerful 1.8GHz to run both HMI and edge computing functions, RZ/G3E also features a Cortex-M33 core to enable low power operation. The combination of two different cores enables users to build products with both high performance and low power consumption.

CPU core

- Arm® Cortex®-A55, Quad-core or dual-core Max. operating frequency: 1.8GHz
- Arm® Cortex®-M33, single-core Max. operating frequency: 200MHz Cache memory (Cortex®-A55)
 - L1 instruction cache: 32KB
 - L1 data cache: 32KB
 - L3 cache: 1MB

External memory

- Ability to connect LPDDR4-SDRAM / LPDDR4X-SDRAM via DDR dedicated
- Data bus width: 32 bits × 1 channel 3D graphics
- Arm Mali[™]-G52 GPU

Video functions

- Video display interface: MIPI DSI × 1 channel or LVDS Dual channel or Digital parallel output × 1 channel
- Video input interface: MIPI CSI-2 × 1 channel
- Video codec module: VCD × 1 channel
- Video Signal processing VSP 1channel Audio functions
- Serial sound interface × 10 channels
- Asynchronous sampling rate converter unit
- SPDIF × 3 channels
- Pulse density modulation x 6 channels

Storage interfaces

- USB 3.2 Gen2 × 1 channel (Host only)
- USB 2.0 × 2 channels (Host only 1 channel/Host-Function 1 channel)
- SD host interface × 1 channel
- SD host interface/Multimedia card interface × 2 channels (Shared with

Other peripheral functions

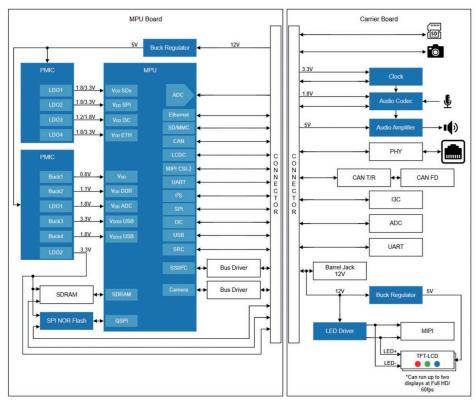
- 32-bit general-purpose timer × 16 channel
- 32-bit CMTW timer × 8 channels
- I3C bus interface × 1 channels
- 12C bus interface × 9 channels
- Serial communication interface with FIFO (SCIF) × 1 channel
- Serial communication interface (RSCI) ×10 channels
- SPI Multi I/O Bus Controllerx 1 channel(8bit Double data rate)
- Serial Peripheral Interface (RSPI) ×3 channels
- Gigabit Ethernet controller × 2 channels
- Controller area network (CAN) interface × 6 channels (support CAN
- 12-bit A/D converter × 8 channels
- Interrupt controller
- Clock generator (CPG): on-chip PLL
- On-chip debug function

CPU Interfaces System LPDDR4/4X (In line ECC) 1 × 32-bit × 3.2GT/s Arm® Debugger Cortex®-M33 Cortex®-A55 Quad Arm® TrustZone xSPI (8-bit/4-bit DTR) FPU 2 × SDHI(UHS-I)/MMC 1 × SDHI(UHS-I) DMAC v/Parity D-L1\$: 32 KB w/EC L2\$: 0KB Interrupt Controlle 1 x PCle Gen3 2-lane 1 × USB3.2 (Gen2 × 1) Host Power management L3\$(Shared): 1MB w/ECC Ethos-U55 2 × USB2.0 lost/Func(OTG) × 1ch, Host × 1ch 1 × Thermal Sensor Unit 2 × GbEther MAC (1000/100, IEEE1588) Memory RAM 512KB w/ FCC 1 × RTC 8 × 32-bit CMTW 10 × RSCI UART/I2C. RS-485 mo Graphics 8 x 32-bit GTM 2 × Dispaly Out MIPI-DSI 4-lane × 1ch / LVDS Dual Channel / Parallel 3D GPU (Mali™-G52) 16 × 32-bit GPTW(PWM) 6 × CAN-FE H.264/265 Enc/Dec Camera In (1 × MIPI CSI-2 4-lane) Analog 8 × 12-bit AD0 Audio Security 10 × SSI (I2S) Device Unique ID Secure Boot 6 × PDM Secure Crypto Engine .ITAG Disable

TRNG

■ High-End Feature-Rich HMI Platform

The demand for sophisticated human machine interfaces (HMIs) continues to grow, necessitating support for multiple display outputs like RGB and MIPI, flexibility in display resolutions, along with peripherals such as microphones, speakers, Ethernet, and CAN FD across various industries. This feature-rich HMI platform integrates multiple peripherals, including microphones, Ethernet, and CAN FD, and is scalable to meet diverse application needs. It offers both an MCU-based system for single displays up to WXGA resolution and an MPU-based system for dual displays up to Full HD, providing flexibility for various end applications.







RZ/G3S Group: 1.1GHz Cortex-A55, Dual Cortex-M33, LPDDR4

The RZ/G3S microprocessor includes an Arm® Cortex®-A55 (1.1GHz) CPU, 16-bit LPDDR4 or DDR4 interface and low-power mode. It also has many interfaces such as PCIe, CAN FD, and 12-bit ADC, making it ideal for applications such as IoT edge applications.

CPU core

- Arm® Cortex®-A55 single-core Max. operating frequency: 1.1GHz
- Arm® Cortex®-M33 core x2
 Max. operating frequency: 250MHz
 Cache memory (Cortex®-A55)
- L1 instruction cache: 32KB
- L1 data cache: 32KB
- L3 cache: 256KB

External memory

- Ability to connect LDDR4-SDRAM / DDR4-SDRAM via DDR dedicated bus
- Data bus width: 16 bits × 1 channel Storage interfaces
- USB 2.0 × 2 channels (Host only 1 channel/Host-Function 1 channel)
- SD host interface × 2 channels
- Multimedia card interface × 1 channel (Shared with SDHI)

Other peripheral functions

- 16-bit timer × 8 channels
- I²C bus interface × 4 channels
- Serial communication interface with FIFO (SCIF) × 6 channels
- SPI Multi I/O Bus Controller × 1 channel (4bit Double data rate)
- Serial Peripheral Interface (RSPI) × 5 channels
- Gigabit Ethernet controller × 2 channels
- Controller area network (CAN) interface× 2 channels (support CAN FD)
- 12-bit A/D converter × 8 channels
- Interrupt controller
- Clock generator (CPG): on-chip PLL
- On-chip debug function

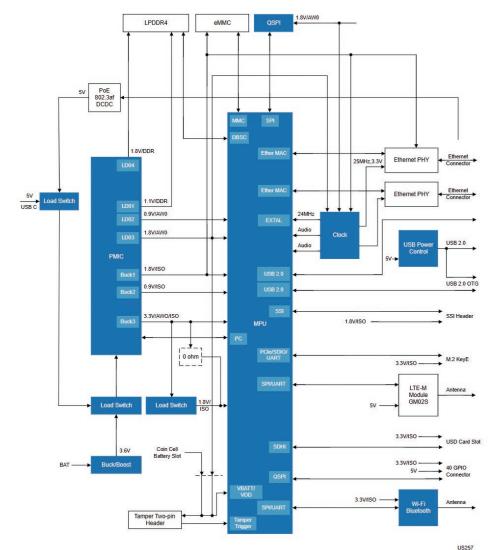
| System | CPL | | Interfaces |
|--|--|-------------------------------|--|
| Arm® Debugger (CoreSight™) | Application Core Domain | System Control Core Domain | 1.6GT/s × 16 LPDDR4/DDR4 (inline ECC) |
| Arm® TrustZone® | Cortex®-A55 | | xSPI |
| DMAC | L1 I-cache : 32 KB (Parity) | | 4 001111111011144440 |
| Interrupt Controller | / D-cache : 32 KB (ECC) L3 cache : 256 Kbytes (ECC) | | 1 × SDHI(UHS-I)/MMC 2 × SDHI(UHS-I) |
| PLL/SSCG | E3 cacile . 230 kbytes (EGG) | | 4 11000.0 |
| MHU (Message Handling Unit) | Cortex®-M33 | Cortex®-M33 | 1 × USB2.0 Host / Function (OTG) |
| Power management | w/ FPU | w/o FPU | 1 × USB2.0 Host |
| (Sleep, Software/Module standby) | are/Module standby) | | |
| VBAT Backup (RTC, Tamper Detection) | Memo | (Root Complex(RC))*Option | |
| 1 × Thermal Sensor Unit | RAM 1MB | 2 × Gbit Ether MAC | |
| 1 × Thermal Sensor Unit | | 4 × I2C | |
| Timers | Audi | - | 1 × I3C |
| 1 × RTC | 4 × SSI (I2S) | 3 × PDM | 6 × SCIF (UART) |
| 8 × 32-bit GTM | RSPDIF | | 5 × RSPI |
| 1 × 32-bit MTU3 | Security (| antian) | 2 × CANFD |
| | Secure Boot | GPI0 | |
| 8 × 16-bit MTU3 | | Secure JTAG | Analog |
| 8 × 32-bit PWM | Secure Crypto Engine | OTP | ŭ |
| 3 × WDT | TRNG | Tamper detection | 8 × 12-bit ADC (1unit) |

■ Single Board Computer Gateway

SBC gateway with Arm Cortex-A55 and Arm Cortex-M33 cores offers efficient processing, flexibility, and connectivity.

With the increasing number of IoT devices in smart buildings and industrial settings, there is a strong need for gateways that can manage and control connected devices. A single board computer (SBC) gateway facilitates communication between different IoT devices and protocols, ensuring smooth data transfer and real-time control across devices, which is essential for automation systems.

This SBC gateway system is assembled with a power-efficient MPU that incorporates an Arm® Cortex®-A55 and two Arm Cortex-M33 cores for real-time processing. A broad set of interfaces provides sensor connectivity and network communication options, making this design suitable for environments where energy efficiency, fast processing, and flexible integration with existing infrastructure are important.





RZ/G2L Group: 1.2GHz Dual Cortex-A55, DDR4/DDR3L, 3DG, Video codec

The RZ/G2L microprocessor includes a Cortex®-A55 (1.2GHz) CPU, 16-bit DDR3L/DDR4 interface, 3D graphics engine with Arm® Mali-G31 and video codec (H.264). It also has many interfaces such as camera input, display output, USB 2.0, and Gbit-Ether, making it ideal for applications such as entry-class industrial humanmachine interfaces (HMIs) and embedded devices with video capabilities.

The RZ/G2L is also package-compatible and pin-compatible with the RZ/V2L embedded with AI accelerator. This allows RZ/G2L users to easily upgrade to the RZ/ V2L for additional AI functions without needing to modify the PCB, keeping migration costs low.

CPU core

- Arm® Cortex®-A55, dual-core or single-core
- Max. operating frequency: 1.2GHz Arm® Cortex®-M33, single-core Max. operating frequency: 200MHz
- Cache memory (Cortex®-A55)
- L1 instruction cache: 32KB ■ L1 data cache: 32KB
- L3 cache: 256KB
- External memory
- Ability to connect DDR4-SDRAM / DDR3L-SDRAM via DDR dedicated
- Data bus width: 16 bits × 1 channel 3D graphics
- Arm Mali[™]-G31 GPU Video functions
- Video display interface: MIPI DSI \times 1 channel or Digital parallel output x 1 channel
- Video input interface: MIPI CSI-2 × 1 channel or Digital parallel input x 1 channel
- Video codec module: VCPL4 \times 1 channel
- Video image processing functions (Resizer and Color Space / Color Format Conversion)

Audio functions

- Serial sound interface × 4 channels Storage interfaces
- USB 2.0 × 2 channels (Host only 1 channel/Host-Function 1 channel)
- SD host interface × 2 channels
- Multimedia card interface × 1 channel (Shared with SDHI)

Other peripheral functions

- 32-bit timer × 1 channel
- 16-bit timer × 8 channels
- PWM timer × 8 channels
- I²C bus interface × 4 channels
- Serial communication interface with FIFO (SCIF) × 5 channels
- Serial communication interface (SCI) × 2 channels
- SPI Multi I/O Bus Controller× 1 channel (8bit Double data rate)
- Serial Peripheral Interface (RSPI) × 3channels
- Gigabit Ethernet controller × 2 channels
- Controller area network (CAN) interface × 2 channels (support CAN
- 12-bit A/D converter × 8 channels
- Interrupt controller
- Clock generator (CPG): on-chip PLL
- On-chip debug function

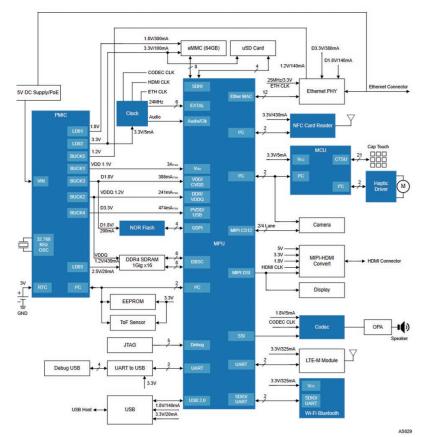
| System | | CI | Interfaces | | |
|-------------------------------|------------------------------------|--------------------|--|----------------------------|---|
| Arm® Debugger (CoreSight™) | Cortex®-A55 1.2GHz Neon™/VFP | 1.2 | ®- A55 (#) GHz | | 1.6/1.3GT/s × 16 DDR4/DDR3L (inline ECC) |
| Arm® TrustZone® | I-L1\$: 32KB (Parity) | D-L1\$: 32KB (ECC) | | | 1 × SPI Multi I/O (8-bit DDR) |
| 16ch DMAC | L2\$: OKB | | | Cortex®-M33 | 1 × SDHI (UHS-I)/MMC |
| Interrupt Controller PLL/SSCG | L3\$(Shared) : | 256KB | (FCC) | @200MHz | 1 × SDHI (UHS-I) |
| FLL/5500 | Low(onarou) . | LOUND | 1 × USB2.0 Host | | |
| Timers 1 × 32-bit MTU3 | R | Mer AM 128 | 1 × USB2.0 | | |
| 8 × 16-bit MTU3 | | 7 1101 120 | 2 × 100/1000Mbps | | |
| 8 × 32-bit PWM | V | 'ideo & | 2 × 100/1000Mbps Ether MAC | | |
| 3 × WDT | 3D GPU Arm® Mali™- | G31 | Camera In (MIPI CSI-2 4-lane, Parallel) | | 2 × I2C, 2 × I2C |
| Austra | | | D | isplay Out | 2 × SCI 8/9-bit |
| Analog 8 × 12-bit ADC | H.264 Enc/D | | (MIPI DS | SI 4-lane, Parallel) | 5 × SCIF (UART) |
| 8 X 1Z-DIL ADG | 1920 × 1080 @ | 3Utps | Image | e Scaling Unit | 3 × RSPI |
| | | · | | | 2 × CAN-FD |
| | Secure Bo | Security | GPI0 | | |
| | Crypto Engi | | | ce Unique ID AG Disable | Audio |
| | TRNG | 1110 | | TP 4Khit | |
| | Inivo | | | JIF 4NUIL | 4 × SSI (I2S) |

Access Control System with NFC, Camera, and Capacitive Touch Authentication The access control system ensures security with

NFC, Wi-Fi, PoE, local storage, and flexible OS support.

With increasing concerns over unauthorized access to buildings and sensitive locations within facilities, there is a growing demand for advanced, multi-layered security solutions in residential, commercial, and industrial settings.

This access control system offers authenticated access and user information storage via NFC card, camera, or manual entry. Capacitive buttons prevent mechanical key failures over extended use, while haptics provide active user feedback. The system supports a proximity sensor to enable auto wake-up functionality to conserve energy, and the option to use either a Linux or Android operating system, offering flexibility in UI experiences.







RZ/G2LC Group: 1.2GHz Dual Cortex-A55, DDR4/DDR3L, 3DG

The RZ/G2LC microprocessor includes a Cortex®-A55 (1.2GHz) CPU, 16-bit DDR3L/DDR4 interface, and 3D graphics engine with Arm® Mali-G31. It also has many interfaces such as camera input, display output, USB 2.0, and Gbit-Ether, making it ideal for applications such as entry-class industrial human-machine interfaces (HMIs) and embedded devices with GUI capabilities.

CPU core

- Arm® Cortex®-A55, dual-core or single-core
 Max. operating frequency: 1.2GHz
- Arm® Cortex®-M33, single-core Max. operating frequency: 200MHz
- Cache memory (Cortex®-A55)

 L1 instruction cache: 32KB
- L1 data cache: 32KB
- L3 cache: 256KB
- External memory
- Ability to connect DDR4-SDRAM / DDR3L-SDRAM via DDR dedicated bus
- Data bus width: 16 bits × 1 channel 3D graphics
- Arm Mali[™]-G31 GPU Video functions
- Video display interface: MIPI DSI × 1 channel
- Video input interface: MIPI CSI-2 × 1 channel
- Video image processing functions (Resizer and Color Space / Color Format Conversion)

Audio functions

■ Serial sound interface × 2 channels

Storage interfaces

- USB 2.0 × 2 channels (Host only 1 channel/Host-Function 1 channel)
- SD host interface × 2 channels
- Multimedia card interface x 1 channel (Shared with SDHI)

Other peripheral functions

- 32-bit timer × 1 channel
- 16-bit timer × 5 channels
- PWM timer × 4 channels
- \blacksquare I²C bus interface \times 4 channels
- Serial communication interface with FIFO (SCIF) × 3 channels
- Serial communication interface (SCI)
 × 2 channels
- SPI Multi I/O Bus Controller× 1 channel (4bit Double data rate)
- Serial Peripheral Interface (RSPI) × 3channels
- Gigabit Ethernet controller × 1 channel
- Controller area network (CAN) interface × 2 channels (support CAN FD)
- Interrupt controller
- Clock generator (CPG): on-chip PLL
- On-chip debug function

| System | П | | CPU | |
|-------------------------------|---|------------------------------------|---------------------------------------|-------|
| Arm® Debugger (CoreSight™) | | Cortex®-A55 1.2GHz Neon™/VFP | Cortex®-A55(#) 1.2GHz Neon™/VFP | |
| Arm® TrustZone® | П | I-L1\$: 32KB (Parity) | | |
| 16ch DMAC | П | D-L1\$: 32KB (ECC) | | Corte |
| Interrupt Controller | П | L2\$: 0KB | L2\$: 0KB | @20 |
| PLL/SSCG | П | L3\$(Shared) : | 256KB (ECC) | 020 |
| | | | | |
| | | | | |

| PLL/SSCG | L3\$(Shared) : 256KB | (ECC) | @ZUUIVII1Z |
|-----------------|--------------------------|----------|---------------------------|
| Timers | Mer | nory | |
| 1 × 32-bit MTU3 | RAM 128 | KB (ECC) | |
| 5 × 16-bit MTU3 | | | |
| 6 × 32-bit PWM | Grap | hics | |
| 3 × WDT | 3D GPU Arm® Mali™-G31 | | amera In CSI-2 4-lane) |

| (MIPI DSI 4-lane) |
|-------------------|
| / (option) |
| Device Unique ID |
| JTAG Disable |
| OTP 4Kbit |
| |

Display Ou

| | Interfaces |
|-------------|---|
| | 1.6/1.3GT/s × 16 DDR4/DDR3L (inline ECC) |
| | 1 × SPI Multi I/O (4-bit DDR) |
| -M33 MHz | 1 × SDHI (UHS-I)/MMC 1 × SDHI (UHS-I) |
| | 1 × USB2.0 Host |
| | 1 × USB2.0 Host / Function |
| | 1 × 100/1000Mbps Ether MAC |
| | 2 × I2C, 2 × I2C |
| ine) | 2 × SCI 8/9-bit |
| t ne) | 4 × SCIF (UART) |
| ie) | 3 × RSPI |
| | 2 × CAN-FD |
| e ID | GPI0 |
| le | Audio |

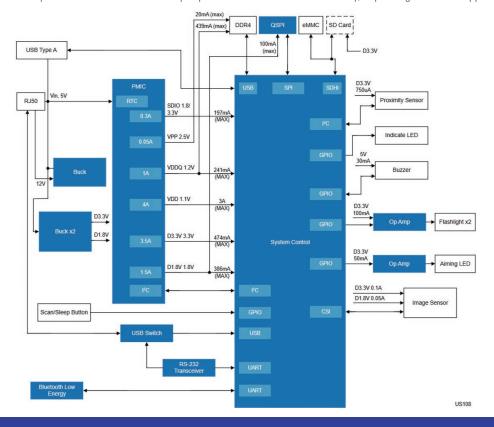
3 × SSI (12S)

■ Barcode Scanner System

Dual-core Cortex-A55-based barcode scanner with object detection, safe operation, and flexible connectivity.

This barcode scanner system can read 1D and 2D barcodes via an integrated image-based scanner with optional object detection using a fast image processor based on a dual Arm® Cortex®-A55 core. The barcode information can be shared through RS-232, USB, or wireless communication.

The system can be based on a variety of processors from the RZ MPU family, depending on the end application.





RZ/G2UL Group: 1.0GHz Cortex-A55, DDR4/DDR3L

The RZ/G2UL microprocessor includes a Cortex®-A55 (1.0GHz) CPU, a 16-bit DDR3L/DDR4 interface, and a simple LCD controller. It also has many interfaces such as camera input, display output, USB 2.0, and Gbit-Ether, making it ideal for applications such as entry-level industrial gateway control and embedded devices with simple GUI capabilities.

CPU core

- Arm® Cortex®-A55, single-core Max. operating frequency: 1.0GHz
- Arm® Cortex®-M33, single-core Max. operating frequency: 200MHz Cache memory (Cortex®-A55)
- L1 instruction cache: 32KB
- L1 data cache: 32KB
- L3 cache: 256KB

External memory

- Ability to connect DDR4-SDRAM / DDR3L-SDRAM via DDR dedicated
- Data bus width: 16 bits × 1 channel Video functions
- Video display interface:
 Digital parallel output x 1 channel
- Digital parallel output × 1 channel

 Video input interface:
- MIPI CSI-2 × 1 channel

 Video image processing functions
 (Resizer and Color Space / Color
 Format Conversion)

Audio functions

Serial sound interface × 4 channels

Storage interfaces

- USB 2.0 × 2 channels (Host only 1 channel/Host-Function 1 channel)
- SD host interface × 2 channels
- Multimedia card interface x 1 channel (Shared with SDHI)

Other peripheral functions

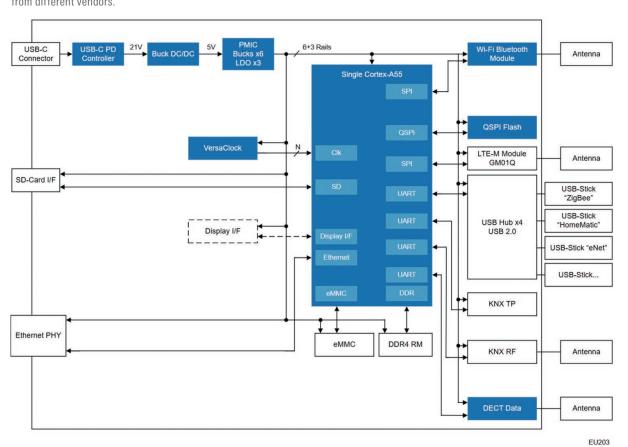
- 16-bit timer × 8 channels
- I²C bus interface × 4 channels
- Serial communication interface with FIFO (SCIF) × 5 channels
- Serial communication interface (SCI)
 × 2 channels
- SPI Multi I/O Bus Controller× 1 channel (4bit Double data rate)
- Serial Peripheral Interface (RSPI) × 3channels
- Gigabit Ethernet controller × 2 channels
- Controller area network (CAN) interface × 2 channels (support CAN FD)
- 12-bit A/D converter × 2 channels
- Interrupt controller
- Clock generator (CPG): on-chip PLL
- On-chip debug function

| System | CP | U | | Interfaces |
|-------------------------------|--|-------------------------------|------------------------|---|
| Arm® Debugger (CoreSight™) | Cortex®-A55 1.0GHz | | | 1.6/1.3GT/s × 16 DDR4/DDR3L (inline ECC) |
| Arm® TrustZone® | Neon™/VFP I-L1\$: 32KB (Parity) D-L1\$: 32KB (ECC) | | | 1 × SPI Multi I/0 (4-bit DDR) |
| Interrupt Controller PLL/SSCG | L2\$: 0KB L3\$ (Shared): 256KB (| ECC) | Cortex®-M33 @200MHz | 1 × SDHI (UHS-I)/MMC 1 × SDHI (UHS-I) |
| | | | | 1 × USB2.0 Host |
| Timers 8 × 16-bit MTU3 (#) | Men RAM 128 | 1 × USB2.0 Host / Function | | |
| 2 × WDT | Grap | 2 × 100/1000Mbps Ether MAC | | |
| Analog | Image Sca | aling Ur | nit | 2 × I2C, 2 × I2C |
| 2 × 12-bit ADC | Display Out | (Paralle | el-IF) | 2 × SCI 8/9-bit |
| | Camera In (MIF | ו רכו-2 | A-lana) | 5 × SCIF (UART) |
| | Camera III (IVIII | 1 001-2 | 4-lalic) | 3 × RSPI |
| | Security | (option | 1) | 2 × CAN-FD |
| | Secure Boot | | ce Unique ID | GPI0 |
| | Crypto Engine | JT | 'AG Disable | Audio |
| | TRNG | - | OTP 1Kbit | 4 × SSI (I2S) |

■ Smart Home Controller with Multiple PHY

All-in-one smart home gateway with multi-standard support, USB-C power, and upgradeable design.

Smart home systems have multiple standards. This design combines all of them in one, allowing for control and visualization of all of your smart home devices from different vendors.







RZ/G2H Group: 1.5GHz Quad Cortex-A57, Quad Cortex-A53, LPDDR4, 3DG

Ultra-high processing performance with quad-core Arm® Cortex®-A57 (1.5GHz) and quad-core Arm Cortex-A53 (1.2GHz) CPUs, with 3D graphics and 4K video encoder/decoder.

CPU core

- Arm® Cortex®-A57, quad-core Max. operating frequency: 1.5GHz
- Arm® Cortex®-A53, quad-core Max. operating frequency: 1.2GHz
- Arm® Cortex®-R7, single-core Max. operating frequency: 800MHz Cache memory (Cortex®-A57)
- L1 instruction cache: 48KB
- L1 data cache: 32KB
- L2 cache: 2MB

Cache memory (Cortex®-A53)

- L1 instruction cache: 32KB
- L1 data cache: 32KB
- L2 cache: 512KB
- Cache memory (Cortex®-R7)
- L1 instruction cache: 32KB
- L1 data cache: 32KB
- I-TCM: 32KB
- D-TCM: 32KB
- External memory
- Ability to connect LPDDR4-SDRAM via DDR dedicated bus
- Data bus width: 32 bits × 2 channels External expansion
- Ability to connect flash ROM or SRAM directly
- Data bus width: 8/16 bits
- PCI Express 2.0 : 1 Lane × 2 channels (one of PHY is shared with Serial ATA) 3D graphics
- PowerVR[™] GX6650

Video functions

- Video display interface × 3 channels (1 channel: HDMI(option), 1 channel: LVDS, 1 channel: RGB888)
- Video input interface × 4 channels (2 channels: MIPI CSI-2, 2 channels: Digital(RGB/YCbCr))

- Video codec module: VCP4 × 1 channel
- IP converter module
- Video image processing functions (color conversion, image enlargement/reduction, filtering)

Audio functions

- Sampling rate converter × 10 channels
- Serial sound interface × 10 channels Storage interfaces
- USB 3.0 DRD × 1 channel
- USB 2.0 × 2 channels (Host only 1 channel/Host-Function 1 channel)
- SD host interface × 4 channels
- Multimedia card interface x 2 channels
- Serial ATA interface × 1 channel Other peripheral functions
- 32-bit timer × 15 channels
- PWM timer × 7 channels
- I²C bus interface × 7 channels
- Serial communication interface (SCIF) × 6 channels
- Quad serial peripheral interface (QSPI) × 2 channels (boot support)
- Clock-synchronous serial interface (MSIOF) × 4 channels (SPI/IIS support)
- Ethernet controller with AVB support (support for IEEE 802.1BA, IEEE 802.1AS, IEEE 802.1Qav, and IEEE 1722)
- Controller area network (CAN) interface × 2 channels
- Interrupt controller (INTC)
- Clock generator (CPG): on-chip PLL
- On-chip debug function

System System controller × Cortex®-A57 1.5GHz | 4 × Cortex®-A53 1.2GHz | 1 × Cortex®-R7 800 System RAM: 384KB L1 I\$ 48KB L1 I\$ 32KB L1 D\$ 32KB L1 D\$ 32KB L1 D\$ 32k Thermal Sensor VFPv3-D1 JTAG Debug 2 cache: 512KB with ECC I-TCM 32KB, D-TCM (CoreSight™ 2 cache: 2MR with FCC **Timers** 26 × 32-bit Timer 15 × 32-bit Interval WDT

| 3D Graphics | |
|---|--|
| PowerVR GX6650 2D/3D tile based 600MHz | |
| | |
| Video Codeo | |

| 7 × PWM out | Up to 4K resolution | | | | | | |
|------------------------|---|--|--|--|--|--|--|
| Audio IPs | (2 channels) | | | | | | |
| dio router w/10 ASRC, | Video IP | | | | | | |
| xer, 10 I2S (6ch TDM), | 3 × Display out 4 × Video Signal Proces | | | | | | |
| 90ch Audio DMA | 1 × Digital out, 1 × LVDS | | | | | | |

| Secure IP |
|-----------------------------|
| Crypto engine |
| (AES, DES, Hash, RSA, TRNG) |

Audio

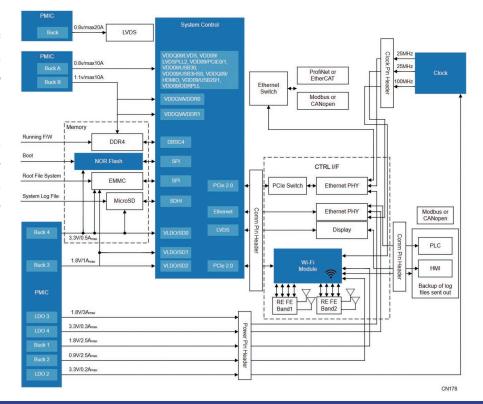
| Video Codec | | | |
|---|----------------------------|--|--|
| Up to 4K resolution (2 channels) | | | |
| Video IP | | | |
| 3 × Display out | 4 × Video Signal Processor | | |
| × Digital out, 1 × LVDS 1 × HDMI | 2 × Fine Display Processor | | |
| 8 × Video in 2 × MIPI CSI-2 (1 × 4L, 1 × 2L) 2 × Digital | | | |

FC-BGA: 29 × 29mm² 1022-pins, 0.8mm pitch

| | Connectivity |
|------|--|
| MHz | 2 × PCle2.0 (1-lane) |
| В | SATA (Rev.3.2) (shared) |
| В | USB3.0/2.0 (DRD) |
| 6 | 4 × USB2.0 (2H, 2H/F/OTG) |
| 32KB | Ethernet AVB (1Gbps) |
| | 2 × CAN2.0B / 2 × CAN-FD |
| П | 6 × UART, 5 × H-UART 4 × SPI |
| | 7 × I2C: 1 × DVFS ctrl |
| | 7 × 120, 1 × DVI 3 CIII |
| | Memory I/F |
| | |
| SSOT | Memory I/F 32-bit × 2ch LPDDR4-3200 |
| ssor | Memory I/F 32-bit × 2ch LPDDR4-3200 access cache |
| | Memory I/F 32-bit × 2ch LPDDR4-3200 access cache 16-bit ExtBus/SRAM 1 × OSPI (4/8-bit selectable) |

Industrial Gateway with Wi-Fi 6

This solution shows the capability and features of an ultra-high performance MPU with quad-core Arm® Cortex®-A57 and quad-core Arm® Cortex®-A53 CPUs, rich peripheral supports LVDS, PCle, and memory I/F like Gigabit Ethernet, DDR, USB 3.0. SD. etc. Power and clock design is simple and saves on PCB size. High-performance, highly integrated Wi-Fi 6 (802.11ax) R2 single PCle chip delivers the best Wi-Fi network with flexibility and reliability.





Connectivity

2 × PCle2.0 (1-lane)

USB3 0/2 0 (DBD)

2 × USB2.0 (1H, 1H/F/0TG)

Ethernet AVB (1Gbps)

2 × CAN2.0B / 2 × CAN-FD

6 × UART, 5 × H-UART

7 × I2C; 1 × DVFS ctrl

Memory I/F

32-bit × 2ch LPDDR4-3200

Raw NAND

(8/16-bit, ONFI 1.x,

ECC 1-8-bits)

16-bit ExtBus/SRAM

1 × QSPI (4/8-bit selectable)

or $1 \times Hyperflash$

4 × SDIO (SDR104)

2 × eMMC (5.0 HS400)

RZ/G2M Group: 1.5GHz Dual Cortex-A57,Quad Cortex-A53, LPDDR4, 3DG

Get a higher specification of processing performance with dual-core Arm® Cortex®-A57 (1.5GHz) and quad-core Arm Cortex-A53 (1.2GHz) CPUs, with 3D graphics and 4K video encoder/decoder.

CPU core

- Arm® Cortex®-A57, dual-core Max. operating frequency: 1.5GHz
- Arm® Cortex®-A53, quad-core
 Max. operating frequency: 1.2GHz
- Arm® Cortex®-R7, single-core
 Max. operating frequency: 800MHz
- Cache memory (Cortex®-A57)
- L1 instruction cache: 48KB
- L1 data cache: 32KB
- L2 cache: 2MB

Cache memory (Cortex®-A53)

- L1 instruction cache: 32KB
- L1 data cache: 32KB
- L2 cache: 512KB

Cache memory (Cortex®-R7)

- L1 instruction cache: 32KB
- L1 data cache: 32KB
- Li data cache: 3
- I-TCM: 32KB
- D-TCM: 32KB
- External memory
- Ability to connect LPDDR4-SDRAM via DDR dedicated bus
- Data bus width: 32 bits × 2 channels External expansion
- Ability to connect flash ROM or SRAM directly
- Data hus width: 8/16 hits
- PCI Express 2.0 : 1 Lane × 2 channels (one of PHY is shared with Serial ATA)
 3D graphics
- PowerVR[™] GX6250

Video functions

- Video display interface × 3 channels (1 channel: HDMI(option), 1 channel: LVDS, 1 channel: RGB888)
- Video input interface × 4 channels (2 channels: MIPI CSI-2, 2 channels: Digital(RGB/YCbCr))
- Video codec module: VCP4 × 1 channel

- IP converter module
- Video image processing functions (color conversion, image enlargement/reduction, filtering)

Audio functions

- Sampling rate converter × 10 channels
- Serial sound interface × 10 channels
 Storage interfaces
- USB 3.0 DRD × 1 channel
- USB 2.0 × 2 channels (Host only 1 channel/Host-Function 1 channel)
- SD host interface × 4 channels
- Multimedia card interface × 2 channels

Other peripheral functions

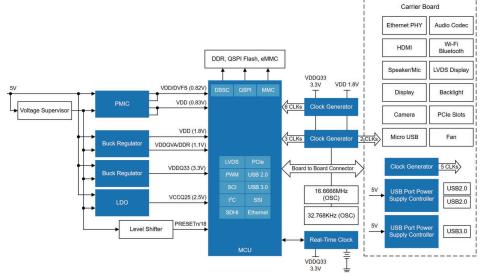
- 32-bit timer × 15 channels
- PWM timer × 7 channels
- I²C bus interface × 7 channels
- Serial communication interface (SCIF) × 6 channels
- Quad serial peripheral interface (QSPI)
 × 2 channels (boot support)
- Clock-synchronous serial interface (MSIOF) × 4 channels (SPI/IIS support)
- Ethernet controller with AVB support (support for IEEE 802.1BA, IEEE 802.1AS, IEEE 802.1Qav, and IEEE 1722, GMII/MII interface, PHY device connection support)
- Ethernet controller with AVB support (support for IEEE 802.1BA, IEEE 802.1AS, IEEE 802.1Qav, and IEEE 1722)
- Controller area network (CAN) interface × 2 channels
- Interrupt controller (INTC)
- Clock generator (CPG): on-chip PLL
- Clock generator (CPG): ofOn-chip debug function

System System controller Cortex®-A57 1.5GHz | 4 × Cortex®-A53 1.2GHz | 1 × Cortex®-R7 800MHz System RAM: 384KB L1 I\$ 48KB L1 I\$ 32KB L1 I\$ 32KB L1 D\$ 32KB L1 D\$ 32KB L1 D\$ 32KB Thermal Sensor JTAG Debug L2 cache: 512KB with ECC 1-TCM 32KB, D-TCM 32 (CoreSight™ 2 cache: 2MR with ECC 3D Graphics Timers PowerVR GX6250 2D/3D tile based 600MHz 26 × 32-bit Timer 15 × 32-bit Interval WDT Video Codec 7 × PWM out Up to 4K resolution (2 channels) Audio IPs Audio router w/10 ASRC, mixer, 10 I2S (6ch TDM), Video IP $\begin{array}{c} \text{3 \times Display UUT} \\ \times \text{Digital out, 1} \times \text{LVDS} \\ 1 \times \text{HDMI} \end{array} \begin{array}{c} 4 \times \text{Video Signal Processo} \\ 2 \times \text{Fine Display Processo} \end{array}$ 3 × Display Out 4 × Video Signal Processor 90ch Audio DMA 8 × Video in 2 × MIPI CSI-2 Crypto engine (1 × 4L, 1 × 2L) 2 × Digital (AES, DES, Hash, RSA, TRNG) FC-BGA: 29 × 29mm² 1022-pins, 0.8mm pitch

■ Multi-Display HMI SoM

SOM with optimized power and timing supports multi-display embedded applications.

System-on-modules (SoMs) are compact, ready-to-use processor modules that help customers accelerate time to market and shorten project schedules for embedded products. This SoM provides an optimized power and timing tree for the MPU, supporting three displays: HDMI, LVDS, and RGB. It helps SoM system designers avoid risk by leveraging a proven, reliable design.



US057





RZ/G2N Group: 1.5GHz Dual Cortex-A57, LPDDR4, 3DG

Higher specification of processing performance with dual-core Arm® Cortex®-A57 (1.5GHz) and with 3D graphics and 4K video encoder/decoder.

CPU core

- Arm® Cortex®-A57, quad-core Max. operating frequency: 1.5GHz
- Arm® Cortex®-R7, single-core Max. operating frequency: 800MHz
- Cache memory (Cortex®-A57)

 L1 instruction cache: 48KB
- L1 data cache: 32KB
- L2 cache: 2MB
- Cache memory (Cortex®-R7)
- L1 instruction cache: 32KB
- L1 data cache: 32KB
- I-TCM: 32KB
- D-TCM: 32KB
- External memory
- Ability to connect LPDDR4-SDRAM via DDR dedicated bus
- Data bus width: 32 bits × 1 channel External expansion
- Ability to connect flash ROM or SRAM directly
- Data bus width: 8/16 bits
- PCI Express 2.0 : 1 Lane × 2 channels (one of PHY is shared with Serial ATA)
 3D graphics
- PowerVR[™] GE7800
- Video functions
- Video display interface x 3 channels (1 channel: HDMI(option), 1 channel: LVDS, 1 channel: RGB888)
- Video input interface × 4 channels (2 channels: MIPI CSI-2, 2 channels: Digital(RGB/YCbCr))
- Video codec module: VCP4 x 1 channel
- IP converter module

- Video image processing functions (color conversion, image enlargement/reduction, filtering)
- Audio functions
 Sampling rate converter × 10
- channels
 Serial sound interface × 10 channels
 Storage interfaces
- USB 3.0 DRD × 1 channel
- USB 2.0 × 2 channels (Host only 1 channel/Host-Function 1 channel)
- SD host interface × 4 channels
- Multimedia card interface × 2 channels
- Serial ATA interface × 1 channel Other peripheral functions
- 32-bit timer × 15 channels
- PWM timer × 7 channels
- I²C bus interface × 7 channels
- Serial communication interface (SCIF)
 × 6 channels
- Quad serial peripheral interface (QSPI)
 × 2 channels (boot support)
- Clock-synchronous serial interface (MSIOF) × 4 channels (SPI/IIS support)
- Ethernet controller with AVB support (support for IEEE 802.1BA, IEEE 802.1AS, IEEE 802.10av, and IEEE 1722)
- Controller area network (CAN) interface × 2 channels
- Interrupt controller (INTC)
- Clock generator (CPG): on-chip PLL
- On-chip debug function

| System | CPU | |
|-------------------|------------------------|---------------------------------|
| System controller | 2 × Cortex®-A57 1.5GHz | 1 × Cortex®-R7 800MHz |
| System RAM: 384KB | L1 I\$ 48KB | L1 I\$ 32KB |
| Thermal Sensor | L1 D\$ 32KB | L1 D\$ 32KB |
| JTAG Debug | Neon™/VFPv4 | VFPv3-D16 |
| (CoreSight™) | L2 cache: 1MB with ECC | I-TCM 32KB, D-TCM 32KB with ECC |
| Timers | 3D Granhics | |

| Timers | 3D Graphics |
|-------------------------|-------------------------|
| 26 × 32-bit Timer | PowerVR GE7800 |
| 15 × 32-bit Interval | 2D/3D tile based 600MHz |
| WDT | Video Codec |
| 7 × PWM out | Up to 4K resolution |
| Audio IPs | (2 channels) |
| Addio II o | |
| Audio router w/10 ASRC, | Video IP |

3 × Display out × Digital out, 1 × LVDS 1 × HDMI

FC-BGA: $29 \times 29 \text{mm}^2$ 1022-pins, 0.8 mm pitch

× Video Signal Processo

1 × Fine Display Processo

| Secure IP | 2 × MIPI CSI-2 |
|--|---|
| Crypto engine , DES, Hash, RSA, TRNG) | 2 × MIPI CSI-2 (1 × 4L, 1 × 2L) 2 × Digital |

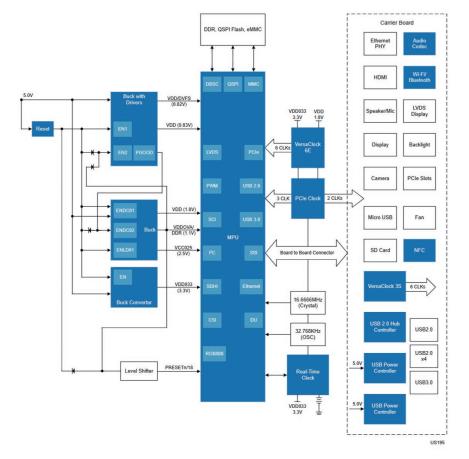
mixer, 10 I2S (6ch TDM), 90ch Audio DMA

| | Connectivity |
|---|-----------------------------------|
| ı | 2 × PCle2.0 (1-lane) |
| | SATA (Rev.3.2) (shared) |
| | USB3.0/2.0 (DRD) |
| 1 | 2 × USB2.0 (1H, 1H/F/0TG) |
| | Ethernet AVB (1Gbps) |
| | 2 × CAN2.0B / 2 × CAN-FD |
| 1 | 6 × UART, 5 × H-UART 4 × SPI |
| ł | 4 × 5PI 7 × I2C; 1 × DVFS ctrl |

| | Memory I/F |
|---|--|
| | 32-bit × 1ch LPDDR4-3200 access cache |
| | Raw NAND (8/16-bit, ONFI 1.x, ECC 1-8-bits) |
| | 16-bit ExtBus/SRAM |
| | $1 \times QSPI$ (4/8-bit selectable) or $1 \times Hyperflash$ |
| | 4 × SDIO (SDR104) |
| Г | 2 × eMMC (5.0, HS400) |

■ High-Performance Human Machine Interface (HMI) System

This solution features a system-on-module (SoM) design to reduce overall complexity and cost. The integrated and tested SoM features a high-performance RZ MPU that enables the creation of graphical human machine interfaces (HMI), capable of driving multiple displays at up to 4K resolutions. Wireless connectivity is provided via Wi-Fi, Bluetooth® Low Energy or near-field communication (NFC).



RZ/G2E Group: 1.2GHz Dual Cortex-A53, DDR3L, 3DG

High processing performance with dual-core Arm® Cortex®-A53 (1.2GHz) CPUs, with 3D graphics and video codec engine.

CPU core

- Arm® Cortex®-A53, quad-core Max. operating frequency: 1.2GHz
- Arm® Cortex®-R7, single-core Max. operating frequency: 800MHz Cache memory (Cortex®-A53)
- L1 instruction cache: 32KB
- L1 data cache: 32KB
- L2 cache: 256KB
- Cache memory (Cortex®-R7)
- L1 instruction cache: 32KB
- L1 data cache: 32KB
- I-TCM: 32KB
- D-TCM: 32KB
- External memory
- Ability to connect DDR3L-SDRAM via DDR dedicated bus
- Data bus width: 32 bits × 1 channel External expansion
- Ability to connect flash ROM or SRAM directly
- Data bus width: 8/16 bits
- PCI Express 2.0 : 1 Lane × 1 channel 3D graphics
- PowerVR[™] GE8300 Video functions
- Video display interface × 2 channels (2 channels: LVDS, 1 channel: RGB888)
- Video input interface × 3 channels (1 channels: MIPI CSI-2, 2 channels: Digital(RGB/YCbCr))
- Video codec module: VCP4 \times 1 channel
- IP converter module

- Video image processing functions (color conversion, image enlargement/reduction, filtering)
- Audio functions ■ Sampling rate converter × 10 channels
- Serial sound interface × 10 channels Storage interfaces
- USB 3.0 DRD × 1 channel
- USB 2.0 × 1 channel (Host-Function 1 channel)
- SD host interface × 3 channels
- Multimedia card interface × 1 channel

Other peripheral functions

- 32-bit timer × 15 channels
- PWM timer × 7 channels
- I²C bus interface × 8 channels
- Serial communication interface (SCIF) × 6 channels
- Quad serial peripheral interface (QSPI) × 2 channels (boot support)
- Clock-synchronous serial interface (MSIOF) × 4 channels (SPI/IIS support)
- Ethernet controller with AVB support (support for IEEE 802.1BA, IEEE 802.1AS, IEEE 802.1Qav, and IEEE 1722)
- Controller area network (CAN) interface × 2 channels
- Interrupt controller (INTC)
- Clock generator (CPG): on-chip PLL
- On-chip debug function

| System | CF | טי |
|-------------------|--------------------------|---------------------------------|
| System controller | 2 × Cortex®-A53 1.2GHz | 1 × Cortex®-R7 800MHz |
| System RAM: 128KB | L1 I\$ 32KB | L1 I\$ 32KB |
| Thermal Sensor | L1 D\$ 32KB | L1 D\$ 32KB |
| JTAG Debug | Neon™/VFPv4 | VFPv3-D16 |
| (CoreSight™) | L2 cache: 256KB with ECC | I-TCM 32KB, D-TCM 32KB with ECC |
| Timers | 3D Gra | anhies |

| HIIIGIS | an diahiiica |
|----------------------|------------------------|
| 26 × 32-bit Timer | PowerVR GE8300 |
| 15 × 32-bit Interval | 2D/3D tile based 600MI |
| WDT | Video Codec |
| 7 × PWM out | Lin to FLID recolution |

Audio IPs Audio router w/10 ASRC, mixer, 10 I2S (6ch TDM), 45ch Audio DMA

| | S | ecure | IP | |
|-------|------|--------|------|-----|
| | Cry | pto en | gine | |
| (AES, | DES, | Hash, | RSA, | TRN |

| Neon™/VFPv4 | VFPv3-D16 | | |
|--|--|--|--|
| L2 cache: 256KB with ECC | I-TCM 32KB, D-TCM 32KB with ECC | | |
| 3D Graphics | | | |
| PowerVR GE8300 2D/3D tile based 600MHz | | | |
| Video Codec | | | |
| Up to FHD resolution | | | |
| Video IP | | | |
| 2 × Display out: (2 × LVDS or 1 × LVDS + 1 × DRGB) | 2 × Video Signal Processor | | |
| | $1 \times \text{Fine Display Processor}$ | | |
| | | | |

| 2 × Video in 1 × MIPI CSI-2 (1 × 2L) 1 × Digital | |
|--|-----------------------|
| FC-BGA: 21 × 21mm ² | 552-pins, 0.8mm pitch |

| Connectivity | | | |
|---|--|--|--|
| 1 × PCle2.0 (1-lane) | | | |
| | | | |
| USB3.0/2.0 (DRD) | | | |
| USB2.0 (1H/F) | | | |
| Ethernet AVB (1Gbps) | | | |
| 2 × CAN2.0B / 2 × CAN-FD | | | |
| $6 \times \text{UART}$, $5 \times \text{H-UART}$ $4 \times \text{SPI}$ $8 \times \text{I2C}$; $1 \times \text{DVFS ctrl}$ | | | |

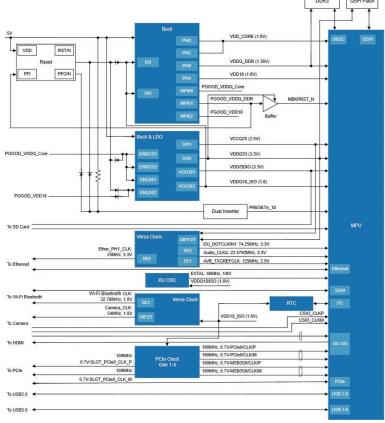
| Memory I/F | | | |
|--|--|--|--|
| 32-bit DDR3L-1856 access cache | | | |
| Raw NAND (8-bit, ONFI 1.x, ECC 1-8-bits) | | | |
| 16-bit ExtBus/SRAM | | | |
| 1 × QSPI (4/8-bit selectable) or 1 × Hyperflash | | | |
| 3 × SDIO (SDR104) | | | |
| eMMC (5.0, HS400) | | | |

■ Power & Timing SoM for RZ/G2E

Power and timing SoM ensures precise timing and efficient power distribution.

In many applications, power and timing are crucial. Applications involving multiple sensors and systems, such as real-time data processing, require precise timing synchronization to ensure all components work in unison, reducing latency and improving performance. Additionally, power distribution is essential for system peripherals to maintain stable performance and energy efficiency.

System-on-Modules (SoMs) are compact, readyto-use processor modules that help engineers and developers accelerate time to market for embedded products and shorten overall project schedules. This SoM offers an optimized power and timing tree for the RZ/G2E MPU, ensuring precise timing and power distribution for various system peripherals.







RZ/Five [RISC-V] Group: 1.0GHz RISC-V CPU, DDR4/DDR3L

The RZ/Five microprocessor includes a RISC-V CPU Core (AX45MP Single) 1.0 GHz, 16-bit DDR3L/DDR4 interface. And it also has many interfaces such as Gbit-Ether, CAN, and USB 2.0, making it ideal for applications such as entry-class social infrastructure gateway control and industrial gateway control.

CPU core

- 64bit RISC-V CPU Core AndesCoreTM AX45MP Single core 1.0GHz
- Cache memory
- L1 instruction Cache: 32KB
- L1 data cache: 32KB
- L2 cache: 256KB

External memory

- Ability to connect DDR4-SDRAM / DDR3L-SDRAM via DDR dedicated bus
- Data bus width: 16 bits × 1 channel Audio functions
- Serial sound interface × 4 channels Storage interfaces
- USB 2.0 × 2 channels (Host only 1 channel/Host-Function 1 channel)
- SD host interface × 2 channels
- Multimedia card interface × 1 channel (Shared with SDHI)

Other peripheral functions

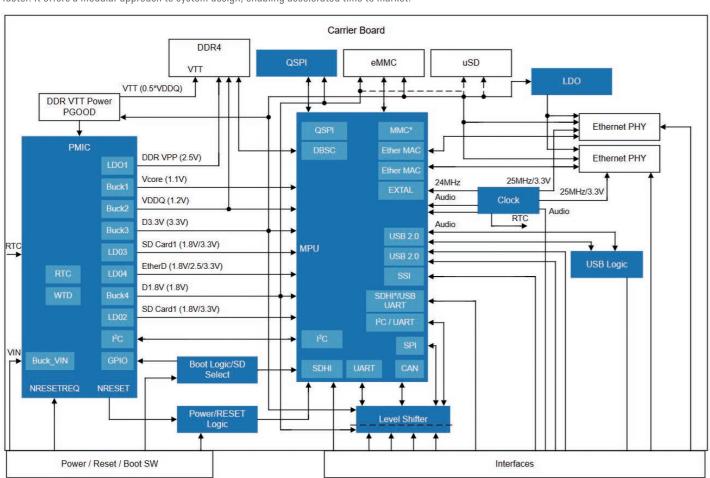
- 16-bit timer × 8 channels
- I^2C bus interface \times 4 channels
- Serial communication interface with FIFO (SCIF) × 5 channels
- Serial communication interface (SCI)
 × 2 channels
- SPI Multi I/O Bus Controller × 1 channel (4bit Double data rate)
- Serial Peripheral Interface (RSPI) × 3 channels
- Gigabit Ethernet controller × 2 channels
- Controller area network (CAN) interface × 2 channels (support CAN
- 12-bit A/D converter × 2 channels
- Interrupt controller
- Clock generator (CPG): on-chip PLL
- On-chip debug function

| System | СРИ | Interfaces |
|-----------------------------|---|-------------------------------|
| Debugger | Application Core Domain | 1.6/1.3GT/s × 16 |
| 16ch DMAC | AX45MP Single (1GHz) With SIMD / FPU | DDR4/DDR3L (inline ECC) |
| Interrupt Controller | I-L1\$: 32KB (Parity), D-L1\$: 32KB (ECC) | 1 × SPI Multi I/O (4-bit DDR) |
| PLL/SSCG | TCM (ILM/DLM): Total 128KB (ECC) | 2 × SDHI(UHS-I)/MMC |
| 1 22 0000 | L2\$: 128KB (ECC) | 1 × USB2.0 Host |
| Timers | ΕΖΨ. 120ΚΒ (ΕΟΟ) | 1 × USB2.0 Host / Function |
| 1 × 32-bit MTU3 | Internal Memory | 2 × 100/1000 |
| 8 × 16-bit MTU3 | SRAM: 128KB (ECC) | Ether MAC |
| 1 × WDT | 511111111111111111111111111111111111111 | 4 × I2C |
| | Security | 2 × SCI 8/9-bit (incl. IrDA) |
| Analog | Secure Boot | 5 × SCIF (UART) |
| 2 input 12-bit ADC (1 unit) | Crypto Engine | 3 × RSPI |
| Thermal Sensor | Secure JTAG | 4 × SSIF2 |
| | TRNG | 2 × CAN-FD |
| | OTP 1Kbit | GPI0 |

■ Scalable SMARC 2.1 Gateway SoM with RISC-V MPU

The scalable SMARC 2.1 SoM design for IIoT gateways with low power consumption, strong connectivity, and flexibility.

As Industrial Internet of Things (IIoT) systems expand, there's a growing demand for compact, modular gateway designs that support high-performance processing while maintaining low power consumption. The Smart Mobility Architecture (SMARC) 2.1 standard is increasingly preferred for IoT gateway designs due to its flexibility and ability to integrate key features like communication interfaces, display support, and optimized power management into a small form factor. It offers a modular approach to system design, enabling accelerated time to market.



RZ/G3 Specification

| Items | RZ/G3E | RZ/G3S |
|-------------------------|--|--|
| CPU (Arm® Cortex®-A) | 2x or 4x Cortex®-A55@1.8GHz L1, L3 Parity/ECC | 1x Cortex®-A55@1.1GHz L1, L3 Parity/ECC |
| CPU (Arm® Cortex®-M) | 1× Cortex®-M33@200MHz | 1× or 2× Cortex®-M33@250MHz |
| NPU | 1 × Ethos™-U55 | _ |
| DRAM I/F | 32-bit × 1ch LPDDR4/4X-3200 w/ECC | 16-bit × 1ch LPDDR4/DDR4-1600 w/ECC |
| Video in | 1 × MIPI CSI-2 | _ |
| Video Codec | Support up to 4K @30fps resolutions | _ |
| 3D GFX | Arm Mali™-G52 GPU | _ |
| Display out | 1 × MIPI DSI or 1 × Digital Parallel output | _ |
| USB | USB3.2 (Gen2) Host × 1ch USB2.0 × 2ch (1Host, 1Host/Function/OTG) | USB2.0 × 2ch (1Host, 1Host/Function/OTG) |
| Gbit Ether | 2ch | 2ch |
| CAN | 6ch (support CAN-FD) | 2ch (support CAN-FD) |
| 12-bit ADC | 8ch | 8ch |
| Package | 625-pin FCBGA, 21mm × 21mm, 0.8mm ball pitch 529-pin FCBGA, 15mm × 15mm, 0.5mm ball pitch | 359-pin LFBGA, 14mm × 14mm, 0.5mm ball pitch 361-pin LFBGA, 13mm × 13mm, 0.5mm ball pitch |

RZ/G2 Specification 1

| Items | RZ/G2L | RZ/G2LC | RZ/G2UL |
|-------------------------|--|--|--|
| CPU (Arm® Cortex®-A) | 1× or 2× Cortex®-A55@1.2GHz L1, L3 Parity/ECC | 1× or 2× Cortex®-A55@1.2GHz L1, L3 Parity/ECC | 1× Cortex®-A55@1.0GHz L1, L3 Parity/ECC |
| CPU (Arm® Cortex®-M) | 1× Cortex®-M33@200MHz | 1× Cortex®-M33@200MHz | 1× Cortex®-M33@200MHz |
| DRAM I/F | 16-bit ×1ch DDR4-1600/DDR3L-1333 w/ECC | 16-bit ×1ch DDR4-1600/DDR3L-1333 w/ECC | 16-bit ×1ch DDR4-1600/DDR3L-1333 w/ECC |
| Video in | 1×MIPI CSI-2 or 1×Digital Parallel input | 1×MIPI CSI-2 | 1×MIPI CSI-2 |
| Video Codec | Support up to Full HD @30fps resolutions Encoding and Decoding: H.264 | _ | - |
| 3D GFX | Arm Mali-G31 GPU @500MHz | Arm Mali-G31 GPU @500MHz | _ |
| Display out | 1×MIPI DSI or 1×Digital Parallel output | 1×MIPI DSI | 1×Digital Parallel output |
| USB | USB2.0×2ch (1Host, 1Host/Function/OTG) | USB2.0×2ch (1Host, 1Host/Function/OTG) | USB2.0×2ch (1Host, 1Host/Function/OTG) |
| Gbit Ether | 2ch | 1ch | 2ch |
| CAN | 2ch (support CAN-FD) | 2ch (support CAN-FD) | 2ch (support CAN-FD) |
| 12-bit ADC | 8ch | _ | 2ch |
| Package | 551-pin LFBGA, 21mm×21mm, 0.8mm ball pitch 456-pin LFBGA, 15mm×15mm, 0.5mm ball pitch | 361-pin LFBGA, 13mm×13mm, 0.5mm ball pitch | 361-pin LFBGA, 13mm×13mm, 0.5mm ball pitch |

RZ/G2 Specification 2

| Items | RZ/G2H | RZ/G2M | RZ/G2N | RZ/G2E |
|-------------------------|---|---|---|---|
| CPU (Arm® Cortex®-A) | 4× Cortex®-A57@1.5GHz 4× Cortex®-A53@1.2GHz L1, L2 Parity/ECC | 2× Cortex®-A57@1.5GHz 4× Cortex®-A53@1.2GHz L1, L2 Parity/ECC | 2× Cortex®-A57@1.5GHz L1, L2 Parity/ECC | 2× Cortex®-A53@1.2GHz L1, L2 Parity/ECC |
| CPU (Arm® Cortex®-R) | 1× Cortex®-R7@800MHz L1, TCM w/ECC | 1× Cortex®-R7@800MHz L1, TCM w/ECC | 1× Cortex®-R7@800MHz L1,TCM w/ECC | 1× Cortex®-R7@800MHz L1,TCM w/ECC |
| DRAM I/F | 32-bit ×2ch LPDDR4(3200) | 32-bit ×2ch LPDDR4(3200) | 32-bit ×1ch LPDDR4(3200) | 32-bit ×1ch DDR3L(1856) |
| Video in | 2×MIPI CSI-2, 2×Digital (RGB/YCbCr) up to 8 input image can be captured | 2×MIPI CSI-2, 2×Digital (RGB/YCbCr) up to 8 input image can be captured | 2×MIPI CSI-2, 2×Digital (RGB/YCbCr) up to 8 input image can be captured | 1×MIPI CSI-2, 1×Digital(RGB/YCbCr) up to 2 input image can be captured |
| Video Codec | Support up to 4k resolutions Decoding: H.265, Encoding and Decoding: H.264 | Support up to 4k resolutions Decoding: H.265, Encoding and Decoding: H.264 | Support up to 4k resolutions Decoding: H.265, Encoding and Decoding: H.264 | Support up to FHD resolutions Decoding: H.265, Encoding and Decoding: H.264 |
| 3D GFX | PowerVR GX6650@600MHz | PowerVR GX6250@600MHz | PowerVR GE7800@600MHz | PowerVR GE8300@600MHz |
| Display out | 1×HDMI, 1×LVDS, 1×Digital RGB | 1×HDMI, 1×LVDS, 1×Digital RGB | 1×HDMI, 1×LVDS, 1×Digital RGB | 2×LVDS or 1×LVDS, 1×Digital RGB |
| USB | USB2.0×2ch (1H, 1H/F/OTG) USB3.0/2.0×1ch (DRD) | USB2.0×2ch (1H, 1H/F/OTG) USB3.0/2.0×1ch (DRD) | USB2.0×2ch (1H, 1H/F/OTG) USB3.0/2.0×1ch (DRD) | USB2.0×1ch (H/F) USB3.0/2.0×1ch (DRD) |
| Gbit Ether | 1ch | 1ch | 1ch | 1ch |
| CAN | 2ch (support CAN-FD) | 2ch (support CAN-FD) | 2ch (support CAN-FD) | 2ch (support CAN-FD) |
| PCle | 2ch (Rev2.0 1Lane) one of the 2ch is shared with SATA | 2ch (Rev2.0 1Lane) | 2ch (Rev2.0 1Lane) one of the 2ch is shared with SATA | 1ch (Rev2.0 1Lane) |
| SATA | 1ch (Pin Shared) | No | 1ch (Pin Shared) | No |
| Package | 1022-pin FCBGA, 29mm×29mm 0.8mm ball pitch | 1022-pin FCBGA, 29mm×29mm 0.8mm ball pitch | 1022-pin FCBGA, 29mm×29mm 0.8mm ball pitch | 552-pin FCBGA, 21mm×21mm 0.8mm ball pitch |



RZ/A Series

Features of the RZ/A Series

The RZ/A series is an RTOS-based microprocessor (MPU) combining excellent real-time performance and fast boot time based on Renesas' proprietary technology and Arm® ecosystem, and is as user-friendly as Renesas MCUs with integrated large size RAM. RZ/A series are specialized devices with a feature set optimized to address diverse HMI, Consumer, Smart Home and Building Automation, Healthcare, Industrial Applications, and Office Automation market segments.

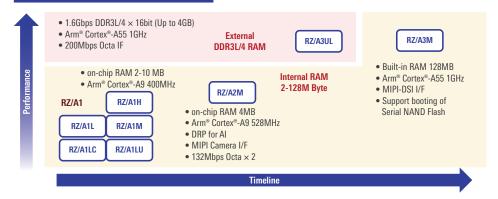


Human Machine Interfaces

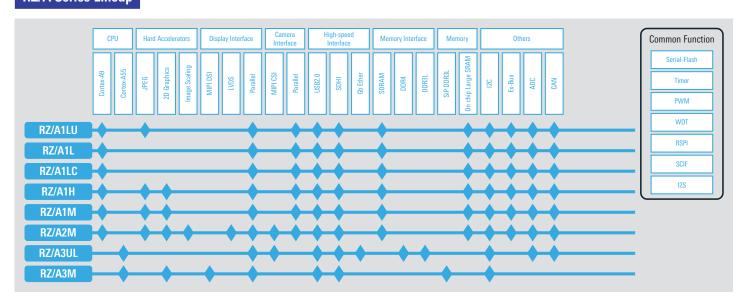


Large size RAM + RTOS

RZ/A Series Product Positioning



RZ/A Series Lineup





RZ/A3M Group: RTOS MPU with built-in DDR3L SDRAM

RZ/A3M microprocessor includes a Cortex®-A55 core with NEON™ extension and built-in large capacity 128MB DDR3L memory. It integrates features such as high-resolution Graphics LCD controller with parallel RGB and 4-lane MIPI-DSI interfaces to display panels, 2D graphics drawing engine, support QSPI NOR/NAND Flash and 244 pin LFBGA package which is ideal for 2-layers board design.

CPU core

 Arm® Cortex®-A55, single-core Max. operating frequency: 1.0GHz Neon™ extension

Cache memory (Cortex®-A55)

- L1 instruction cache: 32KB
- L1 data cache: 32KB
- L3 data cache: 256KB

Memory

- Internal 128KB SRAM
- SiP 128MB DDR3L SDRAM
 2D Graphics
- 2D Graphics Drawing Engine Video functions
- Video display interface MIPI-DSI 4-lane × 1 channel Parallel interface × 1 channel

Audio functions

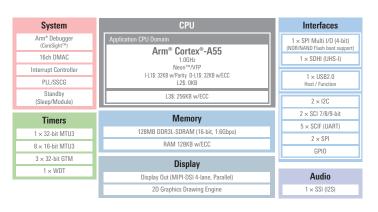
- Serial sound interface × 1 channel Storage interfaces
- USB2.0 × 1 channel (Host-Function)
- SD host interface × 1channel

Other peripheral functions

- 16-bit Multi-function Timer × 8 channels
- 32-bit Multi-function Timer × 1 channel
- 32-bit General Timer × 3 channels
- I²C bus interface × 2 channels
- Serial communication interface with FIFO (SCIF) × 5 channels
- Serial communication interface (SCI)
 × 2 channels
- SPI Multi I/O Bus controller with NOR/NAND support x 1 channel (4bit Double data rate)
- Serial Peripheral Interface (RSPI) × 2 channels
- Interrupt controller
- Clock generator (CPG): on-chip PLL
- On-chip debug function

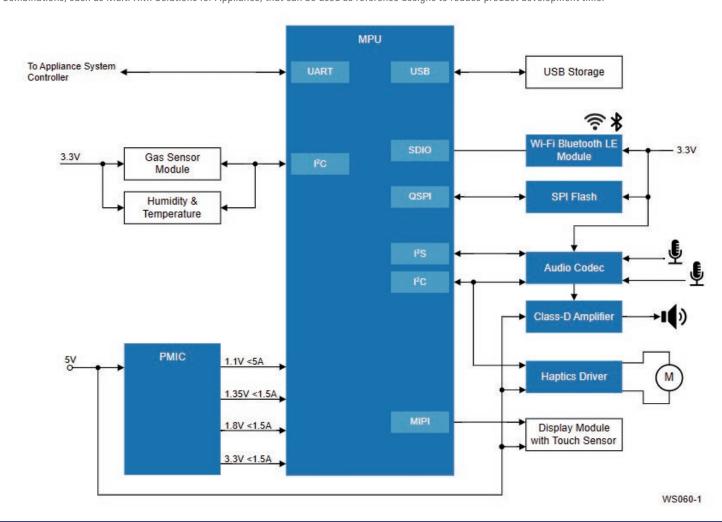
Package

244-LFBGA (17mm × 17mm, 0.8mm pitch)



■ Human Machine Interface (HMI) for Appliances

Renesas will provide a reference system solution for the RZ/A3M with DA9080-62 power management IC. These devices work together seamlessly in Winning Combinations, such as Multi HMI Solutions for Appliance, that can be used as reference designs to reduce product development time.







RZ/A3UL Group: RTOS MPU for High-Definition HMI

RZ/A3UL microprocessor includes a Cortex®-A55 core with NEON™ extension, the ability to connect to high-speed DDR3L/DDR4 RAM and an Octal-SPI memory interface that facilitates simpler and more compact board designs. Using an RTOS allows systems to start up instantly, in less than a second after boot-up. RZ/A3UL provides a cost-effective solution for HMI, IoT Gateway, and audio equipment.

CPU core

 Arm® Cortex®-A55, single-core Max. operating frequency: 1.0GHz Neon™ extension

Cache memory (Cortex®-A55)

- L1 instruction cache: 32KB
- L1 data cache: 32KB
- L3 data cache: 256KB

Memory

- Internal 128KB SRAM
- DDR4/3L SDRAM 16-bit interface Video functions
- Video display interface Parallel interface × 1 channel
- Video input interface MIPI CSP-2 × 1 channel
- Video image processing functions (Resize and Color Space/Color format Conversion)

Audio functions

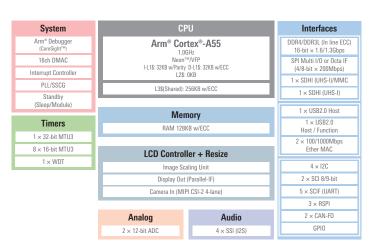
- Serial sound interface × 4 channel Storage interfaces
- USB2.0 × 2 channels (Host 1channel, Host-Function 1 channel)
- SD host interface × 2 channels
- Multimedia card interface x 1 channel (Shared with SDHI)

Analog functions

- 12-bit ADC ×2 input channels Other peripheral functions
- 16-bit Multi-function Timer × 8 channels
- 32-bit Multi-function Timer × 1 channel
- I²C bus interface × 4 channels
- Serial communication interface with FIFO (SCIF) × 5 channels
- Serial communication interface (SCI)
 × 2 channels
- SPI Multi I/O Bus controller x 1 channel (4/8-bit Double data rate)
- Serial Peripheral Interface (RSPI) x 3 channels
- Gigabit Ethernet controller × 2 channel
- Controller area network (CAN) interface × 2 channels (support CAN-FD)
- Interrupt controller
- Clock generator (CPG): on-chip PLL
- On-chip debug function

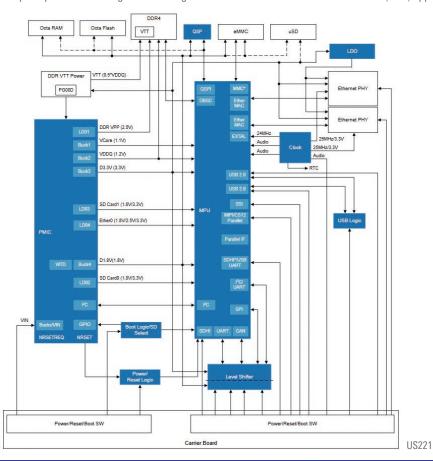
Package

361-LFBGA (13mm × 13mm, 0.5mm pitch)



■ RTOS-Based RZ/A3UL HMI SMARC SoM

This compact SMARC 2.1 system-on-module (SoM) incorporates a Renesas RZ/A3UL MPU for RTOS applications. This system design architecture provides a complete power and timing tree. It is targeted for real-time human machine interface (HMI) applications, such as smart homes/buildings or industrial terminals.



System Benefits:

- RTOS operating system
- Single Arm® Cortex®-A55 configurations for low power consumption
- Support for multiple memories: Octal Flash and RAM, DDR, QSPI, eMMC
- Single programmable clock generator
- Multiple communication interface support: USB, Ethernet, CAN, Wi-Fi/Bluetooth® Low Energy (LE)



RZ/A2M Group: RTOS MPU with DRP and 4MB of On-chip RAM

RZ/A2M supports the MIPI camera interface, widely used in mobile devices, and is equipped with a DRP for high-speed image processing. Renesas has also boosted network functionality with the addition of two-channel Ethernet support. These features enable network connectivity, making the new RZ/A2M best suited for a wide range of systems employing image recognition, from home appliances to industrial machinery.

CPU (Arm® Cortex®-A9)

- Operating frequency: 528MHz
- Single-precision/double-precision FPU
- Arm® Neon™

On-chip memory

■ 4MB

Main graphics and camera input functions

- Video display controller (VDC6): 1 channel LCD output: Max. WXGA Screen superimposition: 3 layers Video input: Max. XGA
- CMOS camera input (CEU): 1 channel
- MIPI CSI-2 interface: 1 channel
- Distortion compensation unit (IMR): 1 channel
- 2D graphics engine: 1 channel
- Sprite engine: 1 channel
- JPEG coding engine: 1 channel Main memory interface functions
- NOR flash, SDRAM, NAND flash
- Serial flash: 1-bit/4-bit/8-bit: 1 channel, 8-bit: 1 channel (ability to run stored programs directly)

- SD/MMC host interface: 2 channels Main communication functions
- USB 2.0 High Speed: 2 channels (Host/Function switchable)
- 10M/100M EtherMAC: 2 channels
- SCIF: 5 channels
- I²C: 4 channels
- SSI: 4 channels
- RSPI: 3 channels
- CAN-FD: 2 channels
- Optional functions
- DRP (Dynamically Reconfigurable Processor)

Package

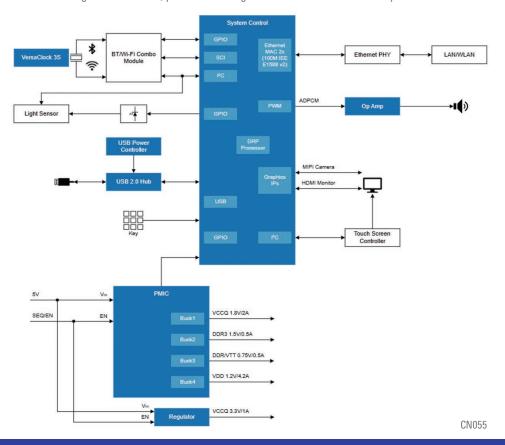
- 176-LFBGA (13mm × 13mm, 0.8mm pitch)
- 256-LFBGA (11mm × 11mm, 0.5mm pitch)
- 272-FBGA (17mm × 17mm, 0.8mm pitch)
- 324-FBGA (19mm × 19mm, 0.8mm pitch)

| System | C | Interfaces | |
|--------------------------------------|--------------------------------------|---|---|
| 16ch DMAC | Arm® Co | 4 × I2C | |
| Interrupt Controller | 528 | MHz | 2 × SCI |
| PLL/SSCG | Neon™ | FPU | 5 × SCIF (UART) |
| On-chip Debug | | | 3 × RSPI |
| (JTAG/SWD) Standby | Mei | mory | 2 × CAN-FD |
| (Sleep/Software/Deep/Module) | SRAN | 1: 4MB | 2 × Ethernet MAC |
| | I Cache: 32KB | D Cache: 32KB | (100M: IEEE1588 v2) |
| Timers | L2 Cach | e: 128KB | 1 × IrDA |
| 3 × 32-bit 0STM | | 1 × SPDIF | |
| 1 × 32-bit MTU3 | Grap | 4 × SSI (I2S) | |
| 8 × 16-bit MTU3 | 4 1/000 (1.000) | 1 × LVDS | 1 × BSC (Ext. Bus I/F) |
| 8 × 32-bit PWM | 1 × VDC6 (LCDC) Timing Controller | 1 × IMR-LS2 | 1 × HyperFlash™ / HyperRAM™ |
| 1 × WDT | Digital Inpuit | 1 × Sprite Engine | 1 × OctaFlash™ / OctaRAM™ |
| 1 × RTC | 1 × CMOS Camera I/F | 1 × 2D Graphics Engine | 1 × SPI Multi I/O (DDR) (1,4 or 8-bit width) |
| DRP (option) | 1 × MIPI Camera I/F | 1 × JPEG Codec Engine | 1 × NAND Flash I/F |
| | | | (ONFI1.0, ECC) |
| lynamically Reconfigurable Processor | Security | 2 × USB2.0 HighSpeed (Host/Peripheral/OTG) | |
| | Secur | 2 × SDHI(UHS-I)/MMC | |
| | Crypto | GPIO | |
| | TR | | |
| | Device U | Jnique ID | Analog |
| | JTAG | 8 × 12-bit ADC | |

■ Industrial Barcode Scanner

Barcode scanners are widely used in industrial applications such as automatic tracking and quality control. Barcode scanners have advantages over other tracking methods, as they offer faster input speed, higher reliability, and the ability to scan a large amount of information while being flexible.

Renesas has a range of MCU/MPUs, power and analog devices that can be used for any barcode scanner solution, optimizing the solution to the specific need.









RZ/A1H & RZ/A1M Group: RTOS MPU with 10MB/5MB of On-chip RAM

RZ/A1H can display WXGA (1280 x 800) and RZ/A1M can display XGA (1024 x 768) without requiring external memory. In addition, with two LCD outputs, up to two LCD displays are possible. It enables very compact embedded designs without the need to worry about memory procurement and memory EOL. You can design your embedded system like an MCU and get the performance of a 400MHz Arm® Cortex®-A9 MPU.

CPU (Arm® Cortex®-A9)

- Operating frequency: 400MHz
- Single-precision/double-precision FPU
- Arm® Neon™

On-chip memory

- RZ/A1H: 10MB
- RZ/A1M: 5MB

Main graphics and camera input functions

- Video display controller (VDC5): 2 channels LCD output: Max. WXGA Screen superimposition: 4 layers Video input: Max. XGA (CVBS analog input supported)
- CMOS camera input (CEU): 1 channel
- PAL/NTSC decoder (DVDEC): 2 channels
- Distortion compensation unit (IMR): 1 channel
- Open VG accelerator: 1 channel
- JPEG coding engine: 1 channel

Main memory interface functions

- NOR flash, SDRAM, NAND flash
- QSPI serial flash: 2 channels (ability to run stored programs directly)
- SD host interface: 2 channels
- MMC host interface: 1 channel
- Main communication functions
- USB 2.0 High Speed: 2 channels (Host/Function switchable)
- 10M/100M EtherMAC: 1channel
- SCIF: 8 channels
- I²C: 4 channels
- SSI: 6 channels
- RSPI: 5 channels
- Ethernet AVB: 1 channel
- CAN: 5 channels

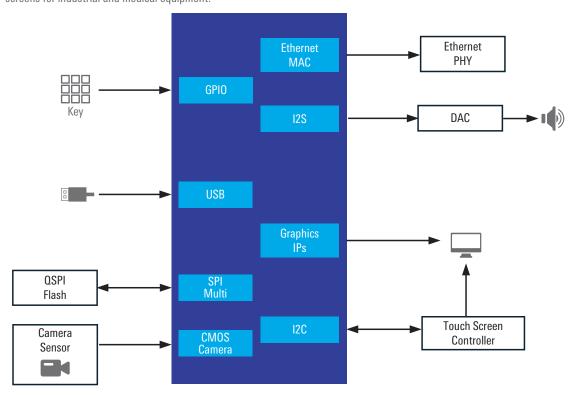
ackane

- 256-LFBGA (11mm × 11mm, 0.5mm pitch)
- 256-LFQFP (28mm × 28mm, 0.4mm pitch)
- 324-FBGA (19mm × 19mm,0.8mm pitch)

| System | СРІ | Interfaces | |
|----------------------|-----------------------------------|-------------------|--|
| 16ch DMAC | Arm® Cort | 8 × SCIF (UART) | |
| Interrupt Controller | 400M | 2 × LIN (Master) | |
| Standby | Neon™ | FPU | 4 × I2C |
| On-Chip Debug | | | 5 × CAN |
| PLL/SSCG | Mem | | 1 × IEBus |
| JTAG/SWD | SRAN RZ/A1H: 10MB / I | | MLB (MOST50) |
| Timers | I Cache: 32KB | D Cache: 32KB | Ethernet MAC (100Mbps) |
| 5 × 16-bit MTU2 | L2 Cache: | Ethernet AVB | |
| 2 × 32-bit Interval | Graph | 6 × SSI (I2S) | |
| 16 × PWM | Video Display | 1 × SPDIF | |
| 1 × WDT | 2ch | 5 × RSPI | |
| 1 × RTC | OpenVG | 2 × SPI Multi I/O | |
| Audio | Enhanced eng. PAL/NTSC dec. 2ch | | 2 × SCIc ISO7816-3 (Smart Card I/F) |
| SCUX 4ch ASRC | CMOS Can | *** | BSC (Ext. Bus I/F) |
| CDROM DEC | 1ch | | 2 × USB2.0 HS |
| Sound Generator | Fish Eye Correction 2ch | | (Host/Func) 2 × SDHI |
| Analog | JPEG Engine | | NAND Flash I/F |
| 8 × 12-bit ADC | | | MMC |
| O A 12 SITABO | | | GPI0 |
| | | | 1 × IrDA |

■ Industrial HMI Systems

With the advancement of industrial HMI systems, there is a growing need for embedded platforms that compactly integrate high-performance graphical interfaces and a variety of peripheral functions.RZ/A1H,RZ/A1M are equipped with a Cortex-A9 processor and large-capacity internal memory, integrating smooth display performance and a variety of interfaces. It utilizes Ethernet, USB, and other technologies to powerfully support the construction of operation screens for industrial and medical equipment.





RZ/A1LU Group: RTOS MPU with JPEG codec and 3MB of On-chip RAM

RZ/A1LU is capable of displaying WVGA (800x480) images without external SDRAM thanks to its 3MB internal SRAM. In addition, the built-in JPEG codec unit improves image processing capabilities. Using the RZ/A1LU, you can design embedded systems like MCUs and obtain the performance of a 400MHz Arm® Cortex®-A9 MPU.

CPU (Arm® Cortex®-A9)

- Operating frequency: 400MHz
- Single-precision/double-precision
 FPU
- Arm® Neon™
- On-chip memory
- 3MB

Main graphics and camera input functions

- LCD controller (VDC5): 1 channel LCD output: Max. WXGA Screen superimposition: 3 layers Video input: Max. XGA
- CMOS camera input (CEU): 1 channel
- JPEG coding engine: 1 channel Main memory interface functions
- NOR flash, SDRAM
- QSPI serial flash: 1 channel (ability to run stored programs directly)

- SD host interface: 2 channels
- MMC host interface: 1 channel Main communication functions
- USB 2.0 High Speed: 2 channels
- (Host/Function switchable)

 10M/100M EtherMAC: 1channel
- SCIF: 5 channels
- I²C: 4 channels
- SSI: 4 channels
- RSPI: 3 channels
- Ethernet AVB: 1 channel
- CAN: 2 channels

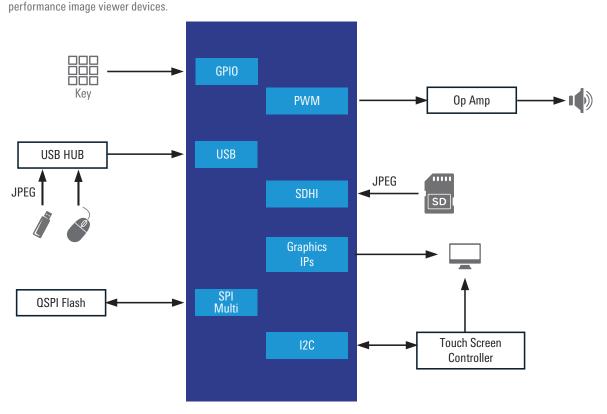
Package

- 176-LFBGA (8mm × 8mm,0.5mm pitch)
- 176-LFQFP (24mm × 24mm,0.5mm pitch)
- 208-LFQFP (28mm × 28mm,0.5mm pitch)

| System | Cl | PU | Interfaces | |
|------------------------|---------------|-----------------------------|--|--|
| 16ch DMAC | Arm® Co | rtex®-A9 | 5 × SCIF (UART) | |
| Interrupt Controller | 400 | MHz | 1 × LIN (Master) | |
| Standby | Neon™ | FPU | 4 × I2C | |
| On-Chip Debug | | | 2 × CAN | |
| PLL/SSCG | | nory | 1 × IEBus | |
| JTAG/SWD | SRAN | 1: 3MB | MLB (MOST50) | |
| Timers | I Cache: 32KB | I Cache: 32KB D Cache: 32KB | | |
| 5 × 16-bit MTU2 | EE Odon | 0. 12010 | Ethernet AVB | |
| 2 × 32-bit Interval | Grap | 4 × SSI (I2S) | | |
| 1 × WDT | Video Displi | 1 × SPDIF | | |
| 1 × RTC | CMOS C | 3 × RSPI | | |
| | | ch | 1 × SPI Multi I/0 | |
| Audio SCUX 4ch ASRC | | Engine ch | 2 × SCIc ISO7816-3 (Smart Card I/F) | |
| CDROM DEC | | | BSC (Ext. Bus I/F) | |
| | | | 2 × USB2.0 HS (Host/Func) | |
| Analog | | | 2 × SDHI | |
| 8 × 12-bit ADC | | | MMC | |
| | | | GPI0 | |
| | | | 1 v IrDA | |

■ Digital photo frame

JPEG files stored on a microSD card or USB memory stick are loaded and processed by the built-in JPEG codec unit, and it smoothly displayed on the LCD. Images are scaled according to the LCD resolution to ensure optimal display quality. It also supports intuitive user operations via touch panels and USB mouse, making it easy to implement interactive UI features such as page turning and image enlargement/reduction. The large capacity of 3MB of built-in RAM eliminates the need for external memory, simplifying board design and reducing costs, while providing powerful support for the development of compact, high-









RZ/A1L & RZ/A1LC Group: RTOS MPU with 3MB/2MB of On-chip RAM

RZ/A1L can display WVGA (800x480) images without external SDRAM thanks to its built-in 3MB SRAM, while the RZ/A1LC can display VGA (640x480) images. It also has an SDRAM interface that can expand external memory up to 128 MB.

CPU (Arm® Cortex®-A9)

- Operating frequency: 400MHz
- Single-precision/double-precision FPU
- Arm® NEON™
- On-chip memory
- RZ/A1L: 3MB
- RZ/A1LC: 2MB

Main graphics and camera input functions

- LCD controller (VDC5): 1 channel LCD output: Max. WXGA Screen superimposition: 3 layers Video input: Max. XGA
- CMOS camera input (CEU): 1 channel Main memory interface functions
- NOR flash, SDRAM, NAND flash
- QSPI serial flash: 1 channel (ability to run stored programs directly)

- SD host interface: 2 channels
- MMC host interface: 1 channel

Main communication functions

- USB 2.0 High Speed: 2 channels (Host/Function switchable)
- 10M/100M EtherMAC: 1 channel
- SCIF: 5 channels
- I²C: 4 channels
- SSI: 4 channels
- RSPI: 3 channels
- CAN: 2 channels

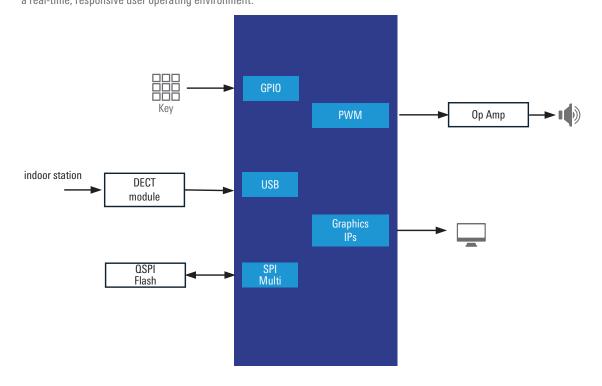
Package

- 176-LFBGA (8mm × 8mm,0.5mm pitch)
- 176-LFQFP (24mm × 24mm,0.5mm nitch)
- 208-LFQFP (28mm × 28mm,0.5mm pitch)
- 233-FBGA (15mm × 15mm, 0.8mm pitch)

| System | CPU | | Interfaces |
|-------------------------------|------------------------------|---------------|--|
| 16ch DMAC | Arm® Cort | ex®-A9 | 5 × SCIF (UART) |
| Interrupt Controller | 400MF | lz | 1 × LIN (Master)* |
| Standby | Neon™ | FPU | 4 × I2C |
| On-Chip Debug | | | 2 × CAN |
| PLL/SSCG | Memo | • | 1 × IEBus* |
| JTAG/SWD | SRAN RZ/A1L: 3MB / RZ | | MLB (MOST50)* |
| Timers | I Cache: 32KB D Cache: 32KB | | Ethernet MAC (100Mbps) |
| 5 × 16-bit MTU2 | L2 Cache: 1 | 4 × SSI (I2S) | |
| 2 × 32-bit Interval | Graphics | | 1 × SPDIF |
| 1 × WDT | Video Display Controller | | 3 × RSPI |
| 1 × RTC | 1ch | | 1 × SPI Multi I/0 |
| Audio | Video In (VDC5) (digital) | | 2 × SCIc ISO7816-3 (Smart Card I/F) |
| SCUX 4ch ASBC | CMOS Cam 1ch | era I/F | BSC (Ext. Bus I/F) |
| CDROM DEC* | TCII | | 2 × USB2.0 HS (Host/Func) |
| Analog | | | 2 × SDHI |
| 8 × 12-bit ADC | | | MMC |
| | | | GPIO |
| A1L Group specification only. | | | 1 × IrDA |

■ Indoor Unit System for Video Door Phone

This system receives and processes image and audio data transmitted via DECT signals from the indoor master unit, displaying video on the LCD while outputting audio in real time. It is equipped with a built-in LCD controller, serial audio IF, and a wide range of communication interfaces (SCI, SPI, I2C, etc.), enabling a compact design with a minimum of external components. The built-in RAM can store RTOS, lightweight frame buffers, audio buffers, etc., providing a real-time, responsive user operating environment.



Development Environment for the RZ Family

The RZ Family is a lineup of high-performance processors designed to support a wide range of applications, offering a variety of product groups. These products are structured to meet diverse needs—ranging from those optimized for graphics and Al processing to those specialized for real-time control and industrial networks. A key feature of the RZ Family is that each product group is supported by a development environment optimized for its specific use case. The development environment for the RZ Family can be broadly categorized into the following two styles.

Linux-based development

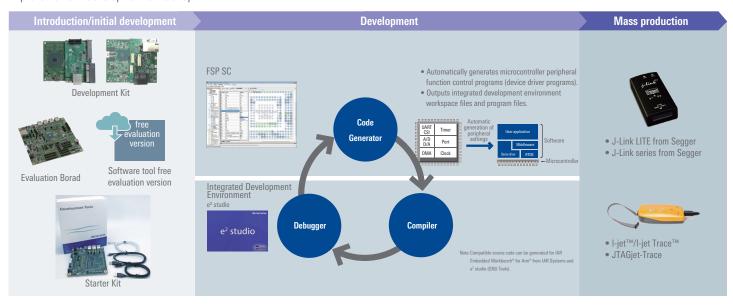
The RZ/V, RZ/N, RZ/T, and RZ/G series support development based on the Linux operating system. These series are optimized for applications requiring high computational performance and flexible software configurations, such as Al inference processing, multimedia handling, and GUI rendering.



Smart Configurator Current Measurement Program
*For Cortex-M cores, please refer to the IDE-based development.

IDE based development

The RZ/V, RZ/N, RZ/T, RZ/G, and RZ/A series offer support for real-time OS-based development environments. Through the use of integrated development environments, real-time operating systems, compilers, and debuggers provided by Renesas Electronics and its partners, customers can achieve substantial improvements in development efficiency.





Evaluation Board

The Renesas RZ Family of 32-bit and 64-bit Arm microprocessors (MPUs) enables the solutions required for the smart societies of the future. Through high-performance CPU cores and a variety of accelerators and peripheral functions, engineers can easily implement high-resolution human machine interfaces (HMI), embedded vision, embedded artificial intelligence (e-AI), and real-time control and industrial ethernet connectivity

Evaluation Board is used to evaluate our RZ Family MPUs. Renesas provide environment where customers can evaluate functionalities of the MPUs using the software environment and various technical documents provided by us.

■ Vision AI (RZ/V series)

The evaluation board kits are used to evaluate our RZ/V vision AI MPUs. We provide the Verified Linux Package and DRP-AI Support Package for these kits. It allows users to boot Linux and run the AI application easily and quickly.

Industrial Network (RZ/N Series)

The evaluation board kits are used to evaluate our RZ/N Industrial Network MPUs. With an on-board emulator, allowing users to start development simply by connecting the included cable to a PC. Industrial Ethernet communication can be easily evaluated using the provided solution.

■ Real-time Control (RZ/T Series)

The evaluation board kits are used to evaluate our RZ/T Real-time Control MPUs. With an on-board emulator, allowing users to start development simply by connecting the included cable to a PC. With the RZ/T2H-EVKIT, motor control of up to 9 axes can be evaluated by connecting to the RZ/T Series Inverter Board and Bus Board.

■ IoT Edge (RZ/G Series)

The evaluation board kits MPUs are used to evaluate our RZ/G IoT Edge MPUs (RZ/G3S and RZ/Five). We provide the Verified Linux Package for these kits. It allows users to boot Linux and reduce the burden of software development in embedded system development.

■ HMI (RZ/G and RZ/A series)

The evaluation board kits are used to evaluate our RZ/G HMI MPUs and RZ/A MPUs. For the RZ/G Evaluation Board kits, we provide the Linux BSP Plus, Verified Linux Package (VLP), and RZ/G HMI Software Development Kit (HMI SDK). It allows users to boot Linux and run HMI demos easily and quickly. For RZ/A Evaluation Board Kits, we provide RZ/A Flexible Software Package (FSP) to help users quickly develop embedded systems.

Board Lineup

| | Vision Al RZ/V Series | Industrial Network RZ/N Series | Real-time Control RZ/T Series | IoT Edge RZ/G Series | HMI RZ/G Series RZ/A Series |
|---|---|-----------------------------------|---|--------------------------------|--|
| Linux / Android™ / Multi-OS with RTOS | RZ/V2H-EVK RZ/V2N-EVK RZ/V2L-EVKIT RZ/V2M-EVKIT RZ/V2MA-EVKIT | RZ/N2H-EVKIT | RZ/T2H-EVKIT | BZ/G3S-EVKIT RZ/Five-EVKIT | RZ/G3E-EVKIT RZ/G2L-EVKIT RZ/G2LC-EVKIT RZ/G2UL-EVKIT RZ/A3UL-EVKIT RZ/G2H-HiHOPE RZ/G2M-HiHOPE RZ/G2N-HiHOPE EK874 (RZ/G2E) |
| RTOS | | RZ/N2L-RSK | RZ/T2ME-RSK RZ/T2M-RSK RZ/T2L-RSK | | EK-RZ/A3M RZ/A3UL-EVKIT RZ/A2M-EVKIT |



RZ/N2H-EVKIT

RZ/T2H-EVKIT

RZ/T2ME-RSK

RZ/G3S-EVKIT

RZ/G3E-EVKIT

EK-RZ/A3M















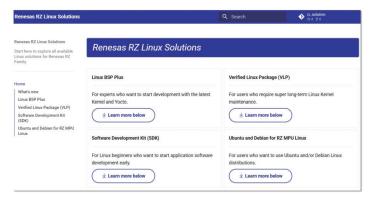
Examples of Boards and Kits for RZ MPUs family

Development Environment for Linux

A development environment is available through a Yocto Project-based Linux BSP, which can be customized to meet specific system requirements. Various development environments are available to accommodate different development needs, enabling flexible development of Linux device drivers and applications.

Please visit the following website for further information.

https://renesas-rz.github.io/rz_solution/





Furthermore, user-friendly development tools, including "Smart Configurator" and "Current Measurement Program", are available to support efficient design.

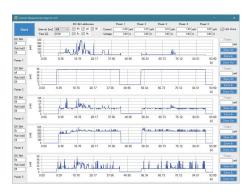
Smart Configurator for RZ

The Smart Configurator is a GUI tool that helps you easily assign shared pins to their specific functions. This tool can generate a device tree file (.dtsi) for Linux. By using this device tree file, users can apply new pin settings.



Current Measurement Program

The Current Measurement Program is a GUI tool that measures current on the EVK of RZ/G3S and RZ/G3E. This tool provides real-time plotting and automatically saves the data as a CSV file. Customers can develop software while checking in real time how much current the EVK is consuming.





Development Environment for RTOS

The RZ family development environment offers flexibility in terms of different supported on-chip debuggers, IDEs, and compilers. Customers can use the Renesas e² studio, IAR Embedded Workbench*. All tools can use the RZ configurators for FSP driver and middleware selection and configuration, in addition to pin mapping and clock tree configuration.

* Supported only on some RZ product series.

Overview

| | Renesas e² studio | IAR Systems Embedded Workbench for Arm | Arm Development Studio |
|--|--|--|--|
| Integrated Development Environment | This development environment based on Eclipse provides a large number of functions. | This is the C/C++ integrated development environment most broadly used internationally. | Embedded C/C++ software development toolchain specifically for Arm-based SoCs. |
| Compilers | GNU Arm Embedded Toolchain | ■ IAR Arm Compiler* | Arm Compiler |
| Debugger probes | J-Link LITE from SeggerJ-Link series from Segger* | ■ I-jet TM /I-jet Trace TM for Arm® Cortex®-A/R/M ■ JTAGjet-Trace | ■ DSTREAM™ ■ ULINKpro™ ■ ULINKproD™ ■ ULINK2™ |
| Supported products | RZ/N2H, N2LRZ/T SeriesRZ/A1 Group, RZ/A2M, RZ/A3UL | RZ/N2H, N2LRZ/T SeriesRZ/A1 Group, RZ/A2M | ■ RZ/A2M |

^{*} Compiler must be purchased and licensed directly from 3rd-party.

Integrated Development Environment

Renesas have prepared an integrated development environment that strongly supports the entire embedded system development. You can choose from an open source-based environment with various expansion functions, an original Renesas development environment, or a partner-made environment according to your usage scenario.







The eclipse-based e² studio along with a GCC compiler and SEGGER J-Link debugger is the primary development solution for RZ MPUs and Flexible Software Package (FSP). e² studio offers a complete development flow from initial project generators, graphical FSP configuration and comprehensive debugger options.



IAR Embedded Workbench® for Arm®

This is the C/C++ integrated development environment most broadly used internationally as a high-performance and highly reliable commercial tool for embedded software development. All functions are integrated seamlessly to maximize development efficiency. The static response analysis and dynamic response analysis add-ons provide a low-cost way for developers to dramatically increase the quality of their code.



Arm Development Studio

Arm Development Studio is an embedded C/C++ development toolchain designed specifically for Arm-based SoCs, from tiny microcontrollers to custom multicore processors. Designed alongside Arm processor IP, it accelerates system design and software development for Cortex-M, Cortex-R and Cortex-A, Cortex-X and Neoverse processors. Only the RZ/A2M model is supported among RZ products.



Compiler

Renesas is preparing a range of compilers to maximize the performance of RZ, fromits own compilers to open source compilers from its partners.



Renesas C/C++ Compiler Package for RZ Family (node locked and floating license versions)

Provides powerful optimized features that help you realize the full performance potential of Renesas' proprietary RZ CPU cores and boost development efficiency. A selection of compiler license formats are available.



Original compilers from IAR Systems generate code that leads the industry in speed and compactness.

Arm Development Studio is an embedded C/C++ development toolchain designed specifically for Arm-based SoCs, from tiny microcontrollers to custom multicore processors.

Debuggers, ICEs

Debugger/ICE is a tool that supports the development and debugging of embedded systems. It emulates the operation of the CPU and memory on the target board, providing features such as setting breakpoints, stepping through p-rogram execution, accessing registers and memory, and real-time tracing.

| | Kyoto Microcomputer Co., Ltd. | DTS INSIGHT Our insight, your value | LAUTERBACH DEVELOPMENT TOOLS | Computex* | SEGGER |
|---------------------|---|--|--|--|---|
| Debuggers | ■ PARTNER-Jet2 | microVIEW-Xross | ■ TRACE32 PowerView | CSIDE version 7 | Ozone e² studio |
| ICEs | | adviceXross | ■ TRACE32 PowerDebug & PowerTrace | ■ PALMiCE4 | J-Link Series |
| Supported compilers | exeGCC from Kyoto Microcomputer GNU tool*1 Arm CC*2 IAR C/C++ compiler,*3 etc. | ■ Arm CC*2 ■ GNU tool,*1 etc. | Arm CC*2 GNU tool*1 IAR C/C++ compiler*3 etc. | ■ Arm CC*² ■ IAR C/C++ compiler*³ ■ GNU tool,*1 etc. | GNU Arm Embedded Toolchain Arm compiler IAR C/C++ compiler, etc. |
| Supported products | RZ/T2H, RZ/T2ME, RZ/ T2M, RZ/T1 RZ/N2H, RZ/N2L RZ/A1 Group, RZ/A2M, RZ/A3UL | ■ RZ/T2H, RZ/T2ME, RZ/ T2M, RZ/T1 ■ RZ/N2H, RZ/N2L | RZ/T2H, RZ/T2ME, RZ/T2M, RZ/T2L RZ/T1 RZ/N2H, RZ/N2L RZ/A1 Group, RZ/A2M, RZ/A3UL | ■ RZ/T1 | RZ/A1 Group, RZ/A2M, RZ/A3UL |

Real-time operating systems (RTOS)

Main RTOS supported by the RZ family are FreeRTOS and Zephyr RTOS. Other RTOSs (such as AzureRTOS) are supported by the Renesas RZ ecosystem, which consists of a wide range of partners.



FreeRTOS is supporting a small memory footprint, fast execution times, and cutting-edge RTOS features and libraries including Symmetric Multiprocessing (SMP), a thread-safe TCP stack with IPv6 support, and seamless integration with cloud services. It's open-source and actively supported and maintained.



The Zephyr Project is a Linux Foundation hosted Collaboration Project. It's an open-source collaborative effort uniting developers and users in building a best-in-class small, scalable, RTOS optimized for resource-constrained devices, across multiple architectures.



Winning Combinations

Speeding Up Application Design for Customers

■ More Than 400 Winning Combinations for a Variety of Applications

Renesas offers comprehensive full-system solutions, featuring Winning Combinations of devices across our embedded processing, power, analog, and connectivity portfolios, to meet your application needs. With these engineering-vetted designs, you can take advantage of an elevated platform for your design ideas, accelerate your product development cycle, and lower overall risk to bring your designs to market.

Renesas continues to make available new Winning Combinations, including many featuring RZ Family MPUs, one after another.

Key Technologies



Artificial Intelligence (AI)
Functional Safety
Gallium Nitride (GaN) Power
Human Machine Interface (HMI)

Motor Control Security Tracking & Locationing USB

Industrial



Appliances
Building Automation
Industrial Automation
Medical & Healthcare

Metering Motor Drives & Robotics Renewable Energy & Grid Retail, Automation & Payment

Consumer Electronics



Cameras
Computing
Home Entertainment

Power Adapters & Chargers Wearables

Communications Infrastructure

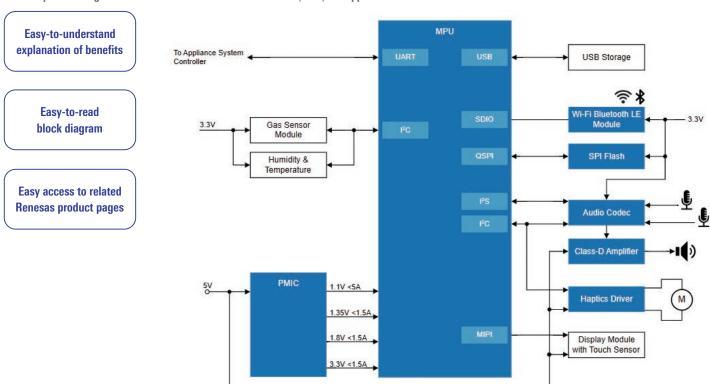


Cloud & Enterprise Memory

Networking & Fixed Access Wireless Infrastructure

WS060-1

■ Example Winning Combinations: Human Machine Interface (HMI) for Appliances



Motor Control Solution

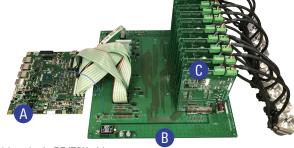
Renesas provides kits and motor control sample code for different types of motors and MPUs.

| Motor Type | Kit Name | RZ/T2H | RZ/T2M | RZ/T2L | RZ/N2L |
|----------------------|---|--------|----------|----------|----------|
| BLDC Motor | RZ/T2H 9-Axis Motor Control Reference Design | ✓ | _ | _ | _ |
| | RZ/T Series Inverter Board | ✓ | _ | _ | _ |
| | RZ/T Series Inverter Board Kit | ✓ | _ | _ | - |
| | Bus Board for RZ/T2H | ✓ | _ | _ | _ |
| | RZ/T2M Motor Solution Kit | _ | ✓ | _ | _ |
| AC Synchronous Motor | RZ/T2M, RZ/T2L, and RZ/N2L Motor Solution Kit (AC 220V Version) | _ | √ | √ | √ |

RZ/T2H 9-Axis Motor Control Reference Design

The <u>RZ/T2H 9-Axis Motor Control Reference Design</u> enables 9-axis motor control using the RZ/T2H advanced high-end microprocessor (MPU). This design consists of the following three boards.

- A) Evaluation board kit for RZ/T2H (P/N:RTK9RZT2H0S00000BJ)
- B) Bus board for RZ/T2H (P/N:RTK0EM0000Z03000BJ)
- C) RZ/T series inverter board kit (P/N:RTK0EM0000S05010BJ) x 9



By connecting these boards, it is possible to evaluate the control of a BLDC motor for 9 axes with a single RZ/T2H chip.

RZ/T2M Motor Solution Kit

The <u>RZ/T2M Motor Solution Kit</u> is a development kit that enables easy initial evaluation and advanced development of a customer's motor control system development using the RZ/T2M MPU with a low voltage 24V BLDC motor.



RZ/T2M, RZ/T2L, and RZ/N2L Motor Solution Kit (AC 220V Version)

This motor solution kit is a reference kit that enables easy initial evaluation and advanced development of motor control systems using an RZ/T2M (or RZ/T2L or RZ/N2L) MPU with a high voltage 220V AC servo motor.

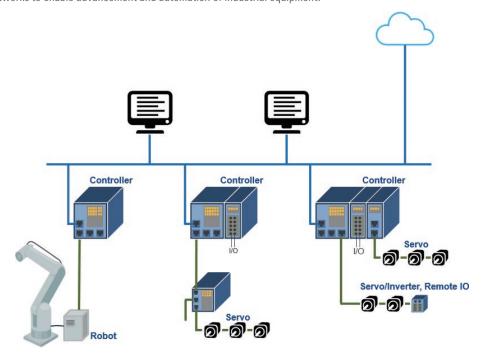
- RZ/T2M version (P/N: CN032-ACSERVOT2MPOCZ)
- RZ/T2L version (P/N: CN032-ACSERV0T2LP0CZ)
- RZ/N2L version (Loaned products)





Industrial Ethernet Solution

Seamless real-time communication is indispensable to Industry 4.0 and Industrial Internet of Things (IIoT) implementations. Renesas offers a variety of solutions for industrial networks to enable advancement and automation of industrial equipment.



Lineup

There are various protocols for industrial network and there are made the best use of various features. However, coexist of various protocols is the challenge for realizing smart society that require interoperability. Renesas has various product/solution and overcomes challenges with customer.

| | RZ/ | T2H | RZ/ | N2H | | T2M F2ME | RZ/T2L | RZ/ | 'N2L |
|------------|----------------|--|--|---|---------------------|----------------|---------------------|---------------------|--------------|
| | Arm® Cortex®-F | | Arm® Cortex®-F | | Arm® Cortex®-F | R52 ×2 | Arm® Cortex®-R52 ×1 | Arm® Cortex®-F | R52 ×1 |
| Controller | 3€OPC UA | PROFO ** | ¾©PC UA | 999 99 3 06 05 * | | | | | |
| | Ether CAT. * | EtherNet/IP | Ether CAT. * | EtherNet/IP | Ether CAT. * | | _ | Ether CAT. * | |
| Device | MOPC UA | 9999 9 3 09 0 * | ************************************** | 999 99 3 0600 * | MOPC UA | epopp dnedd | | MOPC UA | PROFO |
| | Ether CAT. | EtherNet/IP | Ether CAT. | EtherNet/IP | Ether CAT. | EtherNet/IP | Ether CAT: | Ether CAT. | EtheriNet/IP |
| | Modbus TCP | | Modbus TCP | | Modbus TCP | | | Modbus TCP | |

^{*:} Partner solution. Please contact your sales representative for details.

Reliable Development

Conformance tested on major protocols.







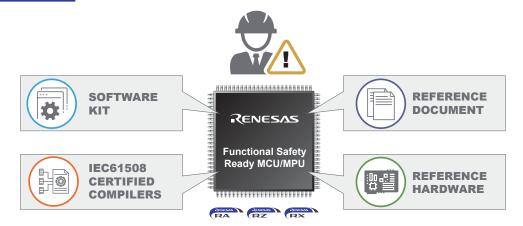
Functional Safety

The Renesas Functional Safety solution provides core technology needed for IEC61508 SIL* certification. The certified software kits and related reference board and documents help to construct a certified functional safety system.

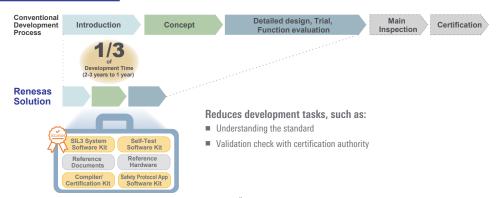
This solution significantly reduces development time and contributes to the implementation of a safe working environment in factories with the ability to handle hazards—even when the system functions fail.

* SIL: Safety Integrity Level which is defined in the functional safety standard

Renesas Solution Overview



Fast, Easy, and Reliable Development



Note: The software kits in yellow boxes are certified by $T\ddot{U}V$ Rheinland

RZ/T2L Safety Network Reference Kit

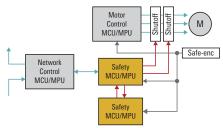
Hardware and software package for realizing safety network function.

- Easily conduct evaluation and development of safety network function on a board equipped with two RZ/T2L chips
- Reference software is available for three types of safety protocols (FSoE, PROFIsafe, and CIPSafety™)

What is inside:

- RZ/T2L functional safety reference board
- RZ/T2L safety network reference software (scan QR code inside the kit)
 - RZ/T2L FSoE reference software
 - RZ/T2L PROFIsafe reference software
 - RZ/T2L CIP Safety[™] reference software

For more detail, please visit RZ/T2L Safety Network Reference Kit.











RZ Family Ecosystem Partners

Renesas is enabling a comprehensive partner ecosystem to deliver an array of software and hardware building blocks that will work out-of-the-box with Renesas RZ Family MPUs. The Renesas RZ ecosystem will help accelerate the development of IoT applications, including core technologies such as security, safety, connectivity, and HMI among others.



Expansive Third Party Solutions Portfolio

- 200+ partners, 300+ solutions and growing
- Coverage across all key IoT technologies
- Robust GTM and strong digital drumbeat



Commercial Grade Building Block Solutions

- Commercial grade software
- Work out-of-box with Renesas products
- Bundling options for select solutions



Problem Solving at Heart

- Address specific design problems
- Address specific skill-set gaps
- Customer-centric approach

Partner Overview

The partner overview shown might not be complete since the partner network is extending almost daily. For best reference and latest data, we recommend checking our webpage at: RZ Partner Ecosystem Solutions



RZ/V Series

| (1) | Option | Quality Grade | Package | Qualification level |
|------------|--------|---------------|---------|---------------------|
| R9AxxGxxxx | XX | G | BG | #xxn |

| (1) | | |
|------------|---------------|--|
| R9A09G057H | RZ/V2H Group | |
| R9A09G011 | RZ/V2M Group | |
| R9A09G055M | RZ/V2MA Group | |
| R9A09G056N | RZ/V2N Group | |
| R9A07G054L | RZ/V2L Group | |

| | Option (RZ/V2H Group) | | |
|----|--------------------------|--|--|
| | Quad Core + Realtime CPU | | |
| 41 | No ISP/GPU, non-Secure | | |
| 42 | GPU only, non-Secure | | |
| 44 | ISP and GPU, non-Secure | | |
| 45 | No ISP/GPU, Secure | | |
| 46 | GPU only, Secure | | |
| 48 | ISP and GPU, Secure | | |

| Option (RZ/V2N Group) | | |
|-----------------------|--------------------------|--|
| | Quad Core + Realtime CPU | |
| 41 | No ISP/GPU, non-Secure | |
| 42 | Non-Secure, GPU | |
| 43 | Non-Secure, ISP | |
| 44 | Non-Secure, ISP, GPU | |
| 45 | Secure | |
| 46 | Secure, GPU | |
| 47 | Secure, ISP | |
| 48 | Secure, ISP, GPU | |
| · | | |

| Quality Grade | |
|---------------|----------|
| G | Standard |

| Package | | |
|---------|-----|--|
| BG | BGA | |

| Qualification level | | |
|---------------------|--------------------|--|
| #ACn | Bulk (Tray) | |
| #BCn | Full Carton (Tray) | |

| Option (RZ/V2M Group) |
|-----------------------|
| _ |

| | Option (RZ/V2MAv Group) |
|--------------------------|-------------------------|
| Quad Core + Realtime CPU | |
| A3 | Full-spec, non-Secure |

| Option (RZ/V2N Group) | | |
|-----------------------|--------------------------|--|
| | Dual Core + sub-CPU | |
| 13 | Reduced-pin, non-Secure | |
| 14 | Full-pin pkg, non-Secure | |
| 17 | Reduced-pin, Secure | |
| 18 | Full-pin pkg, Secure | |
| 23 | Reduced-pin, non-Secure | |
| 24 | Full-pin pkg, non-Secure | |
| 27 | Reduced-pin, Secure | |
| 28 | Full-pin pkg, Secure | |



RZ/N Series

Note: For the RZ/N1 group, please refer to the <u>RZ Family Product Part Number Guide</u>.

| (1) | Option | Quality Grade | Package | Qualification level |
|------------|--------|---------------|---------|---------------------|
| R9AxxGxxxx | XX | G | BG | #xxn |

| (1) | | |
|------------|--------------|--|
| R9A07G084M | RZ/N2L Group | |
| R9A09G087M | RZ/N2H Group | |

| | Option (RZ/N2H Group) |
|----|------------------------------------|
| 04 | Cortex-A55 Single-core, non-Secure |
| 08 | Cortex-A55 Single-core, Secure |
| 24 | Cortex-A55 Dual-core, non-Secure |
| 28 | Cortex-A55 Dual-core, Secure |
| 44 | Cortex-A55 Quad-core, non-Secure |
| 48 | Cortex-A55 Quad-core, Secure |

| Option (RZ/N2L Group) | | |
|-----------------------|------------|--|
| 04 | Non-Secure | |
| 08 | Secure | |

| Quality Grade | |
|---------------|----------|
| G | Standard |

| Package (RZ/N2L Group) | | |
|------------------------|------------|--|
| BG | 225pin BGA | |
| BA | 121pin BGA | |

| Package (RZ/N2H Group) | |
|-------------------------|------------|
| BG | 576pin BGA |

| Qualification level | | |
|---------------------|--------------------|--|
| #ACn | Bulk (Tray) | |
| #BCn | Full Carton (Tray) | |

RZ/T Series

Note: For the RZ/T1 group, please refer to the $\underline{\text{RZ Family Product Part Number Guide}}.$

| (1) | Option | Quality Grade | Package | Qualification level |
|------------|--------|---------------|---------|---------------------|
| R9A0xG07xM | XX | G | XX | #xxn |

| (1) | | |
|-------------------------|-------------------------|--|
| R9A07G074M | RZ/T2L Group | |
| R9A07G075M | RZ/T2M, RZ/T2ME Group * | |
| R9A09G077M RZ/T2H Group | | |

^{*:} If the option (RZ/T2M, RZ/T2ME group) is 29, the group name will be RZ/T2ME.

Otherwise, it will be RZ/T2M.

| Option (RZ/T2H Group) | | |
|-----------------------|---------------------------------------|--|
| 04 | 04 Cortex-A55 Single-core, non-Secure | |
| 08 | Cortex-A55 Single-core, Secure | |
| 24 | Cortex-A55 Dual-core, non-Secure | |
| 28 | Cortex-A55 Dual-core, Secure | |
| 44 | Cortex-A55 Quad-core, non-Secure | |
| 48 | Cortex-A55 Quad-core, Secure | |

| Option (RZ/T2L Group) | | |
|-----------------------|---|--|
| 01 | Classical CAN, non-EtherCAT, non-Secure | |
| 04 | CAN-FD, EtherCAT, non-Secure | |
| 05 | Classical CAN, non-EtherCAT, Secure | |
| 08 | CAN-FD, EtherCAT, Secure | |

| Quality Grade | |
|---------------|----------|
| G | Standard |

| Package (RZ/T2H Group) | |
|------------------------|------------|
| BG | 729pin BGA |

| Package (RZ/T2L Group) | | |
|------------------------|------------|--|
| BG | 196pin BGA | |

| Package (RZ/T2M, RZ/T2ME Group) | | |
|---------------------------------|------------|--|
| BA | 225pin BGA | |
| BG | 320pin BGA | |
| FA | 128pin QFP | |
| FP | 176pin QFP | |

| Qualification level | | |
|---------------------|--------------------|--|
| #ACn | Bulk (Tray) | |
| #BCn | Full Carton (Tray) | |

| Option (RZ/T2M,RZ/T2ME Group) | | | | |
|-------------------------------|--------------------------------------|-----------|--------------------------------------|--|
| Single Core | | Dual Core | | |
| 01 | Classical CAN, non-Ether, non-Secure | 21 | Classical CAN, non-Ether, non-Secure | |
| 02 | Classical CAN, non-Secure | 22 | Classical CAN, non-Secure | |
| 04 | CAN-FD, non-Secure | 24 | CAN-FD, non-Secure | |
| 05 | Classical CAN, non-Ether, Secure | 26 | Classical CAN, Secure | |
| 06 | Classical CAN, Secure | 27 | CAN-FD, non-Ether, Secure | |
| 08 | CAN-FD, Secure | 28 | CAN-FD, Secure | |
| _ | _ | 29 | CAN-FD, Secure, OTFD | |



RZ/G Series

| (1) | HDMI Support | Quality Grade | Option | Package | Qualification level |
|---------|--------------|---------------|--------|---------|---------------------|
| R8A774x | X | НА | XX | Вх | #xxn |
| | | | | | |

| (2) | Option | Quality Grade | Package | Qualification level |
|------------|--------|---------------|---------|---------------------|
| R9A0xG04xx | XX | G | BG | #xxn |

| (1) | | | |
|---------|--------------|--|--|
| R8A774A | RZ/G2M Group | | |
| R8A774B | RZ/G2N Group | | |
| R8A774C | RZ/G2E Group | | |
| R8A774E | RZ/G2H Group | | |

| HDMI Support | | |
|--------------|----------|--|
| 0 | HDMI OFF | |
| 1 | HDMI ON | |
| 2 | HDMI OFF | |
| 3 | HDMI ON | |

| Quality Grade | | |
|---------------|----------|--|
| G,HA | Standard | |

| (2) | | | |
|------------|---------------|--|--|
| R9A07G044L | RZ/G2L Group | | |
| R9A07G044C | RZ/G2LC Group | | |
| R9A07G044U | RZ/G2UL Group | | |
| R9A08G045S | RZ/G3S Group | | |
| R9A09G047E | RZ/G3E Group | | |
| R9A07G043F | RZ/Five Group | | |

| Qualification level | | |
|---------------------|--------------------|--|
| #ACn | Bulk (Tray) | |
| #BCn | Full Carton (Tray) | |

| | Option (RZ/G2H, RZ/G2M, RZ/G2N, RZ/G2E Group) |
|----|---|
| 01 | Standard |

| | Package |
|----|---------|
| BG | BGA |

| Option (RZ/Five Group) | | |
|------------------------|---------------------|--|
| 00 Non-Secure, 266pins | | |
| 01 | Non-Secure, 361pins | |
| 04 Secure, 266pins | | |
| 05 Secure, 361pins | | |

| Option (RZ/G2L, RZ/G2LC, RZ/G2UL Group) | | | | |
|---|-------------------------|-------------------|--------------------------|--|
| | Single Core | Dual Core +subCPU | | |
| 01 | Smaller pkg, non-Secure | 22 | Small pkg, non-Secure | |
| 05 | Smaller pkg, Secure | 23 | Reduced-pin, non-Secure | |
| Single Core +subCPU | | 24 | Full-pin pkg, non-Secure | |
| 11 | Smaller pkg, non-Secure | 26 | Small pkg, Secure | |
| 15 | Smaller pkg, Secure | 27 | Reduced-pin, Secure | |
| _ | _ | 28 | Full-pin pkg, Secure | |

| Option (RZ/G3E Group) | | | | | |
|-------------------------------------|--|----------------------------|------------------------------|--|--|
| Dual Core +subCPU Quad Core +subCPU | | | | | |
| 27 | 15×15mm package, Secure | 47 15×15mm package, Secure | | | |
| 28 | 21×21mm package, Secure | 48 21×21mm package, Secure | | | |
| 37 | 15×15mm package, NPU, Secure | 57 | 15×15mm package, NPU, Secure | | |
| 38 | 21×21mm package, NPU, Secure 58 21×21mm package, | | 21×21mm package, NPU, Secure | | |

| | Option (RZ/G3S Group) | | | | | |
|-------------------------------------|---|--|------------------------------------|--|--|--|
| Dual Core +subCPU Quad Core +subCPU | | | | | | |
| 11 | Non-Secure,1× Cortex-M33,13mm BGA | 31 Non-Secure,1× Cortex-M33,13mm BGA | | | | |
| 13 | Non-Secure, PCle,1× Cortex-M33,14mm BGA | 33 Non-Secure, PCIe, 1× Cortex-M33, 14mm BGA | | | | |
| 15 | Secure,1× Cortex-M33,13mm BGA | 35 | Secure,1× Cortex-M33,13mm BGA | | | |
| 17 | Secure, PCle,1× Cortex-M33,14mm BGA | 37 | Secure,PCle,1× Cortex-M33,14mm BGA | | | |

RZ/A Series

| (1) | Pin count | Temperature | Quality G | rade | Package | Qualification level |
|----------|-------------------|-------------|-----------|------|---------|---------------------|
| R7S7210x | X | V | х | | XX | #xxn |
| (2) | Pin count, Secure | Temperature | Quality G | rade | Package | Qualification level |
| R7S9210x | Х | V | х | | BG | #xxn |
| (3) | Option | Qualit | y Grade | | Package | Qualification level |

| (3) | Option | Quality Grade | Package | Qualification level |
|------------|--------|---------------|---------|---------------------|
| R9A07G06xx | XX | G | BG | #xxn |

| (1) | | | | |
|----------|---|--|--|--|
| R7S72100 | RZ/A1H Group (10MB) | | | |
| R7S72101 | RZ/A1M Group (5MB) | | | |
| R7S72102 | RZ/A1L Group (3MB) | | | |
| R7S72103 | RZ/A1LU Group (3MB), RZ/A1LC Group (2MB) | | | |

| Temperature | | | | |
|-----------------|--|--|--|--|
| V -40°C to 85°C | | | | |

Qualification level (RZ/A2M, RZ/A3M,RZ/A3UL Group)

Quality Grade

High quality Standard Standard

Bulk (Tray)

Full Carton (Tray)

| (2) | | | | |
|----------|----------------------------------|--|--|--|
| R7S92104 | RZ/A2M Group: (4MB), without DRP | | | |
| R7S92105 | RZ/A2M Group: (4MB), with DRP | | | |

| (3) | | | |
|------------|---------------|--|--|
| R9A07G063U | RZ/A3UL Group | | |
| R9407G066M | R7/Δ3M Group | | |

| | Option (RZ/A3M Group) |
|-----|-----------------------|
| 0.4 | Ruilt-in DDR 128MB |

| | , , | |
|-----------------------|------|-------------|
| Option (RZ/A3M Group) | #Aan | Bulk (Tray) |
| uilt-in DDR 128MB | #ACn | Bulk (Tray) |
| | | |

#ACn

#BCn

| Option (RZ/A3UL Group) | | | | |
|------------------------|---------|--|--|--|
| 02 | DDR I/F | | | |

| Package, Pin count, Pin pitch (RZ/A2M Group) | | | | | | |
|--|-----|--------|-------|--|--|--|
| BG | BGA | 176pin | 0.8mm | | | |
| BG | BGA | 256pin | 0.5mm | | | |
| BG | BGA | 272pin | 0.8mm | | | |
| BG | BGA | 324pin | 0.8mm | | | |

| Package, Pin count, Pin pitch (RZ/A1M,RZ/A1H Group) | | | | |
|---|-----|--------|-------|--|
| FP | QFP | 256pin | 0.4mm | |
| BG | BGA | 324pin | 0.8mm | |
| BG | BGA | 256pin | 0.5mm | |

| (RZ/A1H, RZ/A1M, RZ/A1L, RZ/A1LU, RZ/A1LC Group) | | | |
|--|-------------|-----------------|--|
| #Aan | Bulk (Tray) | Sn (Tin) only | |
| #ACn | Bulk (Tray) | SnCu and others | |

| Package (RZ/A3M,RZ/Z3UL Group) | | |
|--------------------------------|-----|--|
| BG | BGA | |

| Package, Pin count, Pin pitch (RZ/A1LU RZ/A1LC Group) | | | | |
|---|-----|--------|-------|--|
| FP | QFP | 176pin | 0.5mm | |
| FP | QFP | 208pin | 0.5mm | |
| BG | BGA | 176pin | 0.5mm | |
| BG | BGA | 233pin | 0.8mm | |

| Package, Pin count, Pin pitch (RZ/A1L Group) | | | | |
|--|-----|--------|-------|--|
| FP | QFP | 176pin | 0.5mm | |
| FP | QFP | 208pin | 0.5mm | |
| BG | BGA | 176pin | 0.5mm | |



Renesas Electronics Corporation TOYOSU FORESIA, 3-2-24 Toyosu, Koto-ku, Tokyo 135-0061, Japan

Notice

- Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation or any other use of the circuits, software, and information in the
- design of your product or system. Renesas Electronics disclaims any and all liability for any losses and damages incurred by you or third parties arising from the use of these circuits, software, or information.

 Renesas Electronics hereby expressly disclaims any warranties against and liability for infringement or any other claims involving patents, copyrights, or other intellectual property rights of third parties, by or arising from the use of Renesas Electronics products or technical information described in this document, including but not limited to, the product data, drawings, charts, programs, algorithms, and application examples.

- No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Penesas Electronics or others.

 You shall be responsible for determining what licenses are required from any third parties, and obtaining such licenses for the lawful import, export, manufacture, sales, utilization, distribution or other disposal of any products incorporating Renesas Electronics products, if required.

 You shall not alter, modify, copy, or reverse engineer any Renesas Electronics product, whether in whole or in part. Renesas Electronics disclaims any and all liability for any losses or damages incurred by you or third parties arising from such alteration, modification, copying or reverse
- Renesas Electronics products are classified according to the following two quality grades: "Standard" and "High Quality". The intended applications for each Renesas Electronics product depends on the product's quality grade, as indicated below "Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; industrial robots; etc.
 - "High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control (traffic lights); large-scale communication equipment; key financial terminal systems; safety control equipment; etc.
 - Unless expressly designated as a high reliability product or a product for harsh environments in a Reneasa Electronics document, Reneasa Electronics document, Reneasa Electronics document, Reneasa Electronics products are not intended or authorized for use in products or systems that may pose a direct threat to human life or bodily injury (artificial life support devices or systems; surgical implantations; etc.), or may cause serious property damage (space system; undersea repeaters; nuclear power control systems; aircraft control systems; key plant systems; military equipment; etc.). Renesas Electronics disclaims any and all liability for any damages or losses incurred by you or any third parties arising from the use of any Reneasa Electronics product that is inconsistent with any Reneasa Electronics data sheet, user's manual or other Reneasa Electronics document.
- No semiconductor product is absolutely secure. Notwithstanding any security measures or features that may be implemented in Reneasa Electronics hardware or software products, Reneasa Electronics shall have absolutely no liability arising out or any vulnerability or security breach, including but not limited to any unauthorized access to or use of a Reneasa Electronics product or a system that uses a Reneasa Electronics product. RENESAS ELECTRONICS DOES NOT WARRANT OR GUARANTEE THAT RENESAS ELECTRONICS PRODUCTS, OR ANY SYSTEMS CREATED USING RENESAS ELECTRONICS PRODUCTS WILL BE INVULNERABLE OR FREE FROM CORRUPTION, ATTACK, VIRUSES, INTERFERENCE, HACKING, DATA LOSS OR THEFT, OR OTHER SECURITY INTRUSION ("Vulnerability Issues"). RENESAS ELECTRONICS DISCLAIMS ANY AND ALL RESPONSIBILITY OR LIABILITY ARISING FROM OR RELATED TO ANY VULNERABILITY ISSUES. FURTHERMORE, TO THE EXTENT PERMITTED BY APPLICABLE LAW, RENSAS ELECTRONICS DISCLAIMS ANY AND ALL WARRANTIES, EXPRESS OR IMPLIED, WITH RESPECT TO THIS DOCUMENT AND ANY RELATED OR ACCOMPANYING SOFTWARE OR HARDWARE, INCLUDING BUT NOT LIMITED TO THE IMPLIED WARRANTIES OF MERCHANTABILITY, OR FITNESS FOR A PARTICULAR PURPOSE.

 When using Renesas Electronics products, refer to the latest product information (data sheets, user's manuals, application notes, "General Notes for Handling and Using Semiconductor Devices" in the reliability handbook, etc.), and ensure that usage conditions are within the ranges specified
- by Renesas Electronics with respect to maximum ratings, operating power supply voltage range, heat dissipation characteristics, installation, etc. Renesas Electronics disclaims any and all liability for any malfunctions, failure or accident arising out of the use of Renesas Electronics products Although Renesas Electronics endeavors to improve the quality and reliability of Renesas Electronics products, semiconductor products, semiconductor products, such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Unless designated as a high
- reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not subject to radiation resistance design. You are responsible for implementing safety measures to guard against the possibility of bodily injury, injury or damage caused by fire, and/or danger to the public in the event of a failure or malfunction of Renesas Electronics products, such as safety design for hardware and software, including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult and impractical, you are responsible for evaluating the safety of the final products or systems manufactured by you.
- Please contract a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. You are responsible for carefully and sufficiently investigating applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive, and using Renesas Electronics products in compliance with all these applicable laws and regulations. Renesas Electronics disclaims any and all liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
- Renesas Electronics products and technologies shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations. You shall comply with any applicable export control laws and regulations promulgated and administered by the governments of any countries asserting jurisdiction over the parties or transactions.

 It is the responsibility of the buyer or distributor of Renesas Electronics products, or any other party who distributes, disposes of, or otherwise sells or transfers the product to a third party, to notify such third party in advance of the contents and conditions set forth in this document.
- This document shall not be reprinted, reproduced or duplicated in any form, in whole or in part, without prior written consent of Renesas Electronics.
- Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products to 1) "Renesas Electronics" as used in this document means Renesas Electronics Corporation and also includes its directly or indirectly controlled subsidiaries.

"Renesas Electronics product(s)" means any product developed or manufactured by or for Renesas Electronics.

(Rev.5.0-1 2020.10)

■Contact Us https://www.renesas.com/contact-us



Renesas Electronics Corporation

www.renesas.com