# ASIC
## Technology Handbook


Renesas Electronics
www.renesas.eu

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# Contents

# 1 Technology

## 1.1 Description

Renesas Electronics supports two types of technologies:

Gate Array ASICs:
- Renesas is number 1 provider worldwide
- Very low unit cost
- Lowest NRE cost – ideally suited for cost-saving FPGA replacements
- Easy and fast design flow
- Copy protection of sensitive customer IP

Cell-based IC (Standard Cell ASICs):
- Optimum design flexibility
- Highest performance
- Extremely low power for highest complexity designs
- Optimum silicon efficiency
- Rich IP portfolio

## 1.2 Overview

| Technology Node | Product | Type |
|---|---|---|
| 0.5µm | CMOS-N5 | Gate Array |
| 0.35µm | CMOS-9HD | Gate Array |
| | EA-9HD | Embedded Array |
| | System-on-Chip Lite | Gate Array + ARM7TDMI |
| 0.25µm | System-on-Chip Lite+ | Gate Array + ARM7TDMI-S |
| 150nm | CB-12 | Cell-based |
| | CMOS-12M | Structured Array |
| | PfESiP-EP1 | Customizable MCU |
| 130nm | CB-130 | Cell-based |
| 90nm | CB-90 | Cell-based |
| | PfESiP-EP3 | Customizable MCU |
| 55nm | CB-55 | Cell-based |
| 40nm | CB-40 | Cell-based |

## 1.3 Gate Array Technology Details

| FAMILY | CMOS-N5 (0.5 µm) | CMOS-9HD (0.35 µm) |
|---|---|---|
| RAW GATE COUNT | 1.5 – 123 Kgates | 11k – 1.6 Mgates (3ML)<br>585k – 2.5 Mgates (4ML) |
| # OF METAL LAYERS | 2 | 3 or 4 |
| CORE VOLTAGE | 3.3 V or 5 V | 3.3 V |
| I/O VOLTAGES | 3.3 V/5 V | 3.3 V/5 V tolerant |
| POWER CONSUMPTION [µW/MHz/gate] | 0.405 @ 5 V<br>0.177 @ 3.3 V | 0.048 |
| PROPAGATION DELAY[1] | 0.14 ns @ 5 V<br>0.18 ns @ 3.3 V | 94 ps |
| MAX. SYSTEM FREQUENCY[2] | 70 MHz @ 5 V<br>50 MHz @ 3.3 V | 100 MHz |
| PACKAGES | QFP/QFN/TQFP/<br>LQFP/SSOP/<br>TFPBGA | QFP/QFN/TQFP/LQFP/<br>PBGA/FPBGA/TBGA/<br>ABGA/TFPBGA |

1) The propagation delay is measured for a 2 input NAND / 1 fan out wiring length 0 mm.
2) The system frequency is measured with a test circuit with 25 logic stages between two registers.

CMOS-12M technology is based on a sea-of-gates architecture combined with embedded high-density SRAMs, PLL and DLL macros.

| FAMILY | | CMOS-12M (0.150 nm) |
|---|---|---|
| RAW GATE COUNT | | up to 4.0 Mgates |
| # OF METAL LAYERS | | up to 6 |
| CORE VOLTAGE | | 1.5 V ± 10% |
| I/O VOLTAGES | | 3.3 V, 2.5 V, 1.8 V, 1.5 V |
| POWER CONSUMPTION [µW/MHz/gate] | | 0.0196 |
| PROPAGATION DELAY | | 62 ps<br>(2-input NAND, F/O = 1, typical length) |
| MAX. SYSTEM FREQUENCY | | 200 MHz (333 MHz @ local parts) |
| PACKAGES | | QFP / FPBGA / PBGA / ABGA |
| EMBEDDED MACROS | SRAM | up to 2.6 Mbits |
| | DLL | up to 8 (supports 100 to 175 MHz) |
| | APLL | 1 or 2 SSCG, up to 3 phase shift PLL |

## 1.4 Embedded Array Technology Details

Embedded array technology allows the implementation of high-density, cell-based memory blocks in a gate array technology.

| FAMILY | EA-9HD (0.35 µm) |
|---|---|
| RAW GATE COUNT | 11k – 1.6 Mgates (3ML)<br>592k – 2.5 Mgates (4ML) |
| # OF METAL LAYERS | 3 or 4 |
| CORE VOLTAGE | 3.3 V |
| I/O VOLTAGES | 3.3 V/5 V full swing |
| POWER CONSUMPTION [µW/MHz/gate] | 0.048 |
| PROPAGATION DELAY[1] | 94 ps |
| MAX. SYSTEM FREQUENCY[2] | 100 MHz |
| PACKAGES | QFP/QFN/TQFP/LQFP/PBGA/FPBGA/ TBGA/ABGA |

1) The propagation delay is measured for a 2 input NAND / 1 fan out wiring length 0 mm.
2) The system frequency is measured with a test circuit with 25 logic stages between two registers.

## 1.5 Customizable MCU Technology Details

### 1.5.1 System-on-Chip Lite+

System-on-gate array / Customizable Microcontroller

| FAMILY | System-on-Chip Lite+ |
|---|---|
| EMBEDDED CPU | ARM7TDMI-S |
| SYSTEM FREQUENCY | 133 MHz |
| EMBEDDED MACROS | SDRAM Controller, 10/100M Ethernet MAC, Interrupt Controller, UART, Timer, Watchdog, APB, AHB |
| TECHNOLOGY | 0.25 µm – CB10VX |
| GATE COUNT | 250K/440 Kgates (raw) |
| CORE VOLTAGE | 2.5 V |
| I/O VOLTAGES | 3.3 V / 5 V tolerant |
| PACKAGES | FPBGA-240 |

### 1.5.1 PfESiP

Platform for Embedded System In Package / Customizable Microcontroller

| FAMILY | | PfESiP EP-1 |
|---|---|---|
| EMBEDDED CPU | | V850E2S |
| PERFORMANCES | | 430 Mips |
| TECHNOLOGY | | 150 nm – CB12 |
| EMBEDDED MACROS | | Memory controller, USB2.0 Host and Function, UARTs, Timers, A/D converter |
| EXTERNAL BUS | | 16- or 32-bit |
| USER DEFINED LOGIC | TECHNOLOGY | 0.35 µm EA9HD (default) |
| | GATES COUNT | up to 240K |
| CORE VOLTAGE | | 1.5 and 3.3 V |
| PACKAGES | | 417 to 572 PBGA |

| FAMILY | | PfESiP EP-3 |
|---|---|---|
| EMBEDDED CPU | | V850E2M |
| PERFORMANCES | | 600 Mips |
| TECHNOLOGY | | 90 nm– CB90 |
| EMBEDDED MACROS | | Memory controller, USB2.0 Host and Function, UARTs, A/D and D/A converter, Ethernet MAC, CAN |
| EXTERNAL BUS | | 32-bit |
| USER DEFINED LOGIC | TECHNOLOGY | 0.35 µm EA9HD (default) |
| | GATES COUNT | up to 600K |
| CORE VOLTAGE | | 1.5 and 3.3 V |
| PACKAGES | | 417 to 572 PBGA |

## 1.6 Cell-based (Standard Cell) ASICs Technology Details

| FAMILY | CB-12 (150 nm) | CB-130 (130 nm) |
|---|---|---|
| RAW GATE COUNT | up to 32 Mgates | up to 52 Mgates (@M Library) |
| # OF METAL LAYERS | up to 8 | up to 9 |
| CORE VOLTAGE | 1.5 V | 1.2 V |
| I/O VOLTAGES | 2.5 V, 3.3 V, 5 V tolerant | 1.2 V, 1.8 V, 2.5 V and 3.3 V |
| POWER CONSUMPTION [nW/MHz/gate] | 13 CB-12L<br>13 CB-12M<br>24 CB-12H | 7 CB-130L<br>7 CB-130M<br>9 CB-130H |
| PROPAGATION DELAY[1] | 31.7 ps @ 1.5V CB-12L 21.2 ps @ 1.5 V CB-12M 17.1 ps @ 1.5 V CB-12H | 16.2 ps CB-130H<br>19.0 ps CB-130M |
| MAX. SYSTEM FREQUENCY[2] | 400 MHz CB-12H<br>266 MHz CB-12M<br>100 MHz CB-12L | 500 MHz CB-130H<br>311 MHz CB130M<br>100 MHz CB130L |
| PACKAGES | QFP/ FPBGA/PBGA/ TBGA/ ABGA /FCBGA | QFP/FPBGA/PBGA/TBGA/ ABGA/FCBGA |

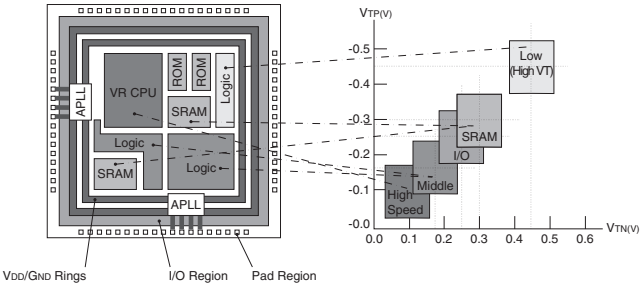
| FAMILY | CB-90 (90 nm) | CB-55 (55 nm) |
|---|---|---|
| RAW GATE COUNT | up to 100 Mgates (@H Library) | up to 200 Mgates |
| # OF METAL LAYERS | up to 9 | up to 7 |
| CORE VOLTAGE | 1.0 V | 1.0/1.2V<br>(@ same architecture) |
| I/O VOLTAGES | 1.0 V, 1.8 V, 2.5 V and 3.3 V | 1.8 V, 2.5 V and 3.3 V |
| POWER CONSUMPTION [nW/MHz/gate] | 2.6 CB-90H<br>1.8 CB-90M | 0.29 @ 1.0 V<br>0.40 @ 1.2 V |
| PROPAGATION DELAY[1] | 14.1 ps CB-90H<br>16.7 ps CB-90M | 11.8 ps @1.2 V<br>22.8 ps @ 1.0 V |
| MAX. SYSTEM FREQUENCY[2] | 1 GHz CB-90H<br>366 MHz CB90M<br>200 MHz CB90L | 1.2 GHz CB-55H<br>450 MHz CB-55L (1.2 V)<br>233 MHz CB-55L (1.0 V) |
| PACKAGES | FPBGA/PBGA/TBGA/<br>ABGA/FCBGA | PBGA, FPBGA, FCBGA |

| FAMILY | CB-40 (40 nm) |
|---|---|
| RAW GATE COUNT | up to 400 Mgates |
| # OF METAL LAYERS | up to 7 |
| CORE VOLTAGE | 1.0 V and 1.1 V |
| I/O VOLTAGES | 1.8 V, 2.5 V and 3.3 V |
| POWER CONSUMPTION [nW/MHz/gate] | 0.18 @ 1.0 V<br>0.21 @ 1.1 V |
| MAX. SYSTEM FREQUENCY[2] | 1.5 GHz CB-40H<br>500 MHz CB40L |
| PACKAGES | PBGA/FPBGA/FCBGA |

1) The propagation delay is measured for a 2 input NAND / 1 fan out wiring length 0 mm.
2) The system frequency is measured with a test circuit with 25 logic stages between two registers.

## 1.7 Multi-Transistor-Type Concept

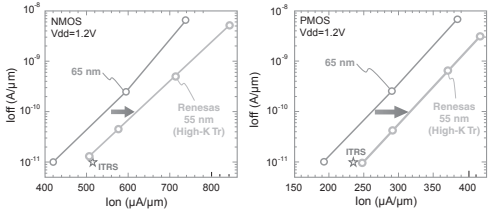
Starting from CB-12 all cell based technologies do provide a multi-transistor-type concept. The picture below illustrates this concept as an example for the CB-12 technology.




Three different types of transistors are available, which can be mixed by using the different libraries. Thereby the H stands for high speed, M for standard libraries and L for low power libraries.

## 1.8 High-k Transistors

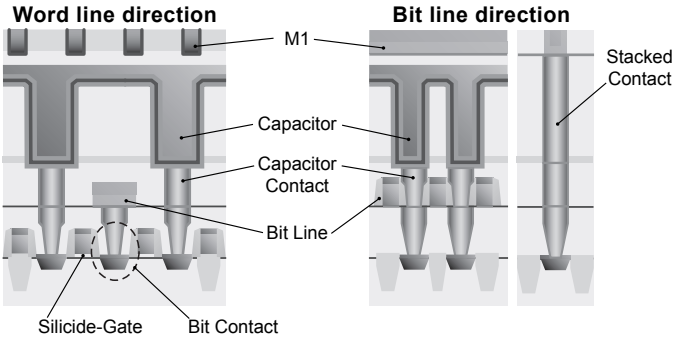
With CB-55 Renesas introduced the high-K transistors technology in its cell based solutions.




Using this type of transistor over silicon dioxide in CB-55 and further technology allows Renesas to reduce the leakage current at these nodes length significantly.

## 1.9 eDRAM

Renesas' eDRAM technology eliminates the usual bottleneck between the chip and separate memory with all the benefits of fast memory access and high overall system speeds. The metal/insulator/metal capacitor on the bit line (MIM COB) process from Renesas allows to reduce the cell size and to improve the performances compared to other standards. This technology also facilitates system design by allowing orientation-free cells and signal routes that permit active wires to run over eDRAM macros for optimized integration and performance.

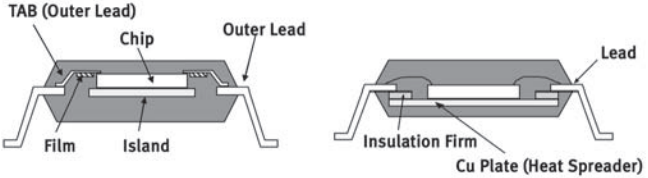


# 2 Packages

## 2.1 QFP (Quad Flat Pack)

### 2.1.1 Description

Quad Flat Package with leads along the edges of the packages. The chip is connected to the leads via tape (TAB: tape automated bonded) or wires. For thermally enhanced QFPs the chip is placed on a heat spreader.



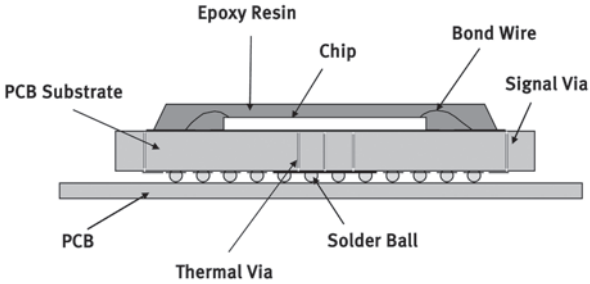

### 2.1.2 Features

- Well-established, general purpose packages
- 44 to 376 pins
- 0.4 mm to 1 mm pin pitch
- 1 or 2.7 mm package height

## 2.2 BGA (Plastic & Fine Pitch Ball Grid Array)

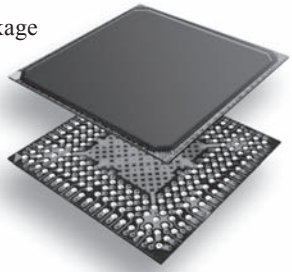
### 2.2.1 Description

Plastic ball grid array packages are surface mount packages consisting of a plastic substrate, whose input/output connections consist of solder balls in an array on the bottom of the package. Standard substrate of this type of package has two layers, but it can be designed with more layers. The chip is mounted “face up” and connected to the substrate via wires. Also available as fine pitch variation (FPBGA).




### 2.2.2 Features

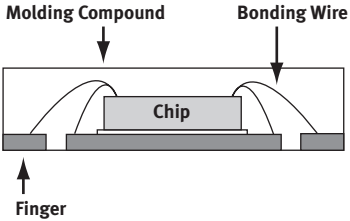
- High-ball count, low cost BGA package
- 61 to 672 balls
- Ball pitch:
  PBGA 1.0 or 1.5 or 1.27 mm
  FPBGA 0.8 or 0.65 mm



## 2.3 QFN (Quad Flat-pack No leads)

### 2.3.1 Description

QFN packages are ideally suited for applications where a low footprint and low height are important. On the other other hand the 0.5 mm lead-pitch still allows for using cost efficient PCBs.



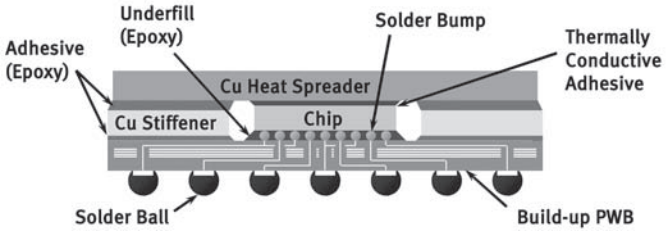

### 2.3.2 Features

- Very small footprint
- Cost optimized
- 28 to 48 pins
- 0.5 mm lead pitch

## 2.4 FCBGA (Flip-Chip BGA)

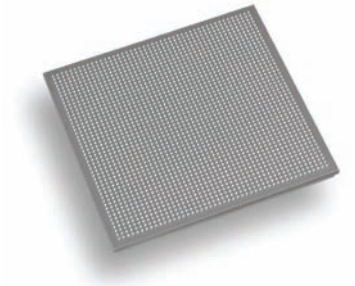
### 2.4.1 Description

In the Flip-Chip-Ball-Grid-Array-Package the chip has bumped terminations spaced on the device and is intended for a face down attach to a multi-layer substrate to reduce die size and increase signal counts.




### 2.4.2 Features

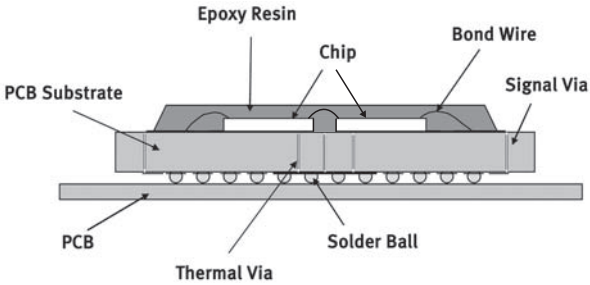
- Optimum thermal and electrical characteristics
- 600 to 3000 balls
- 0.8 or 1 or 1.27 mm ball pitch



## 2.5 SiP (System in Package)

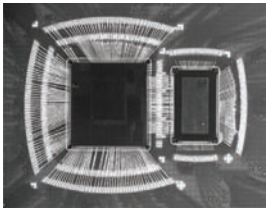
### 2.5.1 Description

Systems in Package allow embedding several chips, which are internally connected by fine wires, within one package in order to reduce the size of the board and global cost.



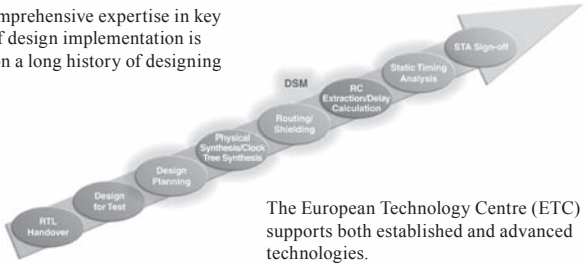

### 2.5.2 Features

- Multiple chips/dies in one single package
- For cost/area balancing
- High peformance interchip connections



# 3 Design Services

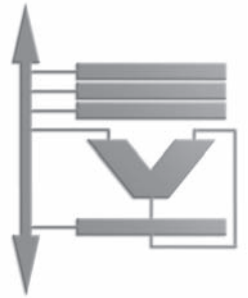
Our comprehensive expertise in key areas of design implementation is based on a long history of designing ASICs.




The European Technology Centre (ETC) supports both established and advanced technologies.

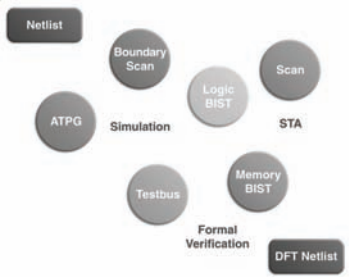
## 3.1 RTL-Handover

To save you time in verification and system design, Renesas offers a complete synthesis service. With our extensive knowledge of all Renesas technologies our experts provide individual solutions for all design details from specification to final layout.



## 3.2 Design for Test

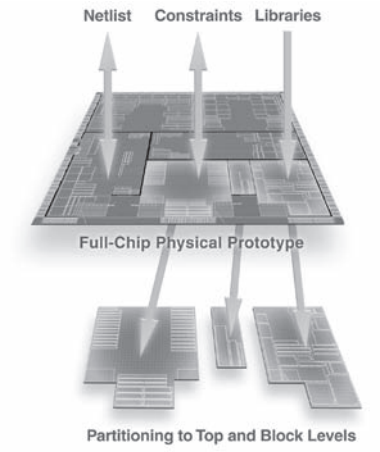
Renesas offers comprehensive test services to improve the quality of your chip.



Full scan insertion including ATPG, boundary scan as well as memory and logic BIST running at the target operating frequency will be inserted using a fully automated script environment. All these DFT services can be mixed, adapted and inserted to your requirements. Formal verification, a complete STA for each test mode and pattern simulation are included in Renesas' DFT service. The hierarchical approach is well established for handling large designs fast and efficiently.

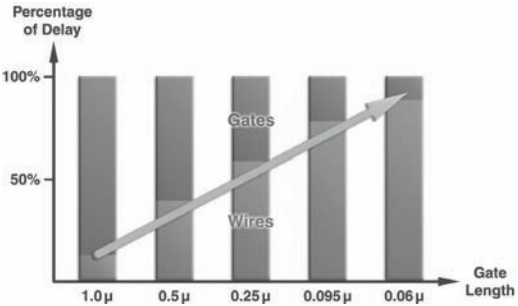
## 3.3 Design Planing

To bring your multi-million gate design early to market Renesas supports a design planning step with full virtual prototyping. This guarantees reliable feedback on the performance and physical feasibility of your design at the beginning of the implementation phase. Partitioning is also performed to allow concurrent implementation work on the top and block hierarchies.



## 3.4 Physical Synthesis combined with CTS

With decreasing structure size on silicon, the effects of wire interconnect increasingly dominate the overall path delay.
Physical synthesis enables Renesas to take this into account by relying on actual placement information instead of wire load models. This means that timing and routing information can be taken into account concurrently during placement. This, combined with clock tree synthesis (CTS) and timing-driven multi-mode, multi-corner optimization, achieves the best timing correlation compared to post layout results. In this way, Renesas significantly reduces iterations and the overall response time.



## 3.5 SI known Routing / Shielding – RC Extraction / Delay Calculation

The prevention and fixing of signal integrity (SI) effects is addressed with a dedicated routing engine. Special attention is also given to suppress clock jitter, chattering and cross talk on clock related nets.

## 3.6 Static Timing Analysis - STA sign-off

STA sign-off is a very fast and efficient method for timing verification of highly complex designs. Renesas' timing calculation considers the different on-chip delay variations like crosstalk and process variation as well as voltage and temperature sensitivity for cell and wire delay. This assures high reliability in the STA sign-off procedure for your project.

## 3.7 DSM effects counter measurements

Renesas' deep sub-micron activities cover issues like signal integrity, long-term reliability and manufacturability. All these effects are given consideration throughout implementation from design planning, placement and routing, to RC extraction and delay calculation. All currently known DSM effects are considered in the flow. Timing variances due to deep sub-micron effects are also taken into account during static timing analysis.

# 4 IP Macro Blocks

**CPU Cores:**

- Renesas: V850E family
- ARM: ARM7TDMI-S™,
  ARM966E-S™, ARM946E-S™,
  ARM926EJ-S™,
  ARM946E-S Supermacro,
  ARM1136J(F)-S™
  ARM1156T2(F)-S™
  ARM11 MPCore (multi-processor)
  ARM Cortex™ (M3, R4, A5, A8, A9)
- MIPS Technologies: 4KEc™, 24KEm™, 24KEc™, 24KEf™, 74Kf™ families
- x86 compliant: V30MZ

**System Integration Cores:**

- SRAM, multiported SRAM
- ROM
- UART, timer, interrupt controller, I²C, PWM, SSI, SPI, etc.
- Memory controller
  (DDR-SDRAM, SDRAM, SRAM, ROM, Flash)
- DMA controller, LCD controller
- PCI, PCI-X, PCI-Express
- AMBA™ bus architecture
- Network-on-Chip (NoC) bus architecture

**Networking Cores:**

High-speed serial interfaces and SERDES cores
- from 120 Mbps up to 6.5 Gbps
- Various interface options: LVDS, LVDSS, pCML, pECL

XAUI, 1G/10G Ethernet, FibreChannel, Serial-ATA, sRIO
SPI 4.2, POS L3
10/100 M Ethernet MAC and PHY
10/100/1000 M Ethernet MAC
8B/10B coder/decoder
UTOPIA interface
CAN

**Multimedia Cores:**

IEEE1394-a, LINK layer and PHY
USB1.1, USB2.0
JPEG
MPEG
Cryptographic cores

**Technology Specific Cores:**

A/D converter, D/A converter
Analogue PLLs
Embedded DRAM, CMOS-compatible
Embedded Flash
Power-on-Reset
Voltage regulator

# 5 Acronyms

| Acronym | Long Form |
|---|---|
| A | |
| ADC | Analog Digital Converter |
| AGP | Advanced Graphics Port |
| AHB | Advanced High-performance Bus |
| ALU | Arithmetical Logical Unit |
| AMPS | Advanced Mobil Phone System |
| ANSI | American National Standards Institute |
| APB | Advanced Peripheral Bus |
| APLL | Analog Phase Locked Loop |
| ASB | Advanced System Bus |
| ASCII | American Standarad Code for Information Interchange |
| ASCP | Appliciation-Specific Customer Product |
| ASIC | Application-Specific Integrated Circuit |
| ASSP | Application-Specific Standard Part |
| ATPG | Automatic Test Pattern Generation |
| B | |
| BGA | Ball Grid Array |
| BiCMOS | Bipolar Complementary Metal Oxide Semiconductor |
| BIST | Build in Self-Test |
| C | |
| CAD | Computer Aided Design |
| CAE | Computer Aided Engineering |
| CAM | Content Addressable Memory |
| CAN | Controller Area Network |
| CCIT | Consultive Commitee for International Telephone |
| CDMA | Code Division Multiple Access |
| CISC | Complex Instruction Set Computer |
| CML | Current Mode Logic |
| CMOS | Complementary Metal-Oxide-Silicon |
| CPRI | Common Protocol Radio Interface |
| CPU | Central Processing Unit |
| CRC | Cyclical Redundancy Check |
| CSI | Clock Serial Interface |
| CSP | Chip Size Package |
| CTS | Clock Tree Synthesis |
| CTT | Center Tap Terminated Interface |

| Acronym | Long Form |
|---|---|
| D | |
| DAC | Digital Analog Converter |
| DEF | Design Exchange Format (Floorplaner to place and route) |
| DFT | Design For Testability |
| DIP | Dual In-Line Package |
| DLL | Delay-Locked Loop |
| DMA | Direct Memory Access |
| DPLL | Digital Phase Locked Loop |
| DRAM | Dynamic Random Access Memory |
| DRC | Design Rule Checker |
| DSM | Deep Sub-micro |
| DSP | Digital Signal Processor |
| E | |
| ECL | Emitter-Coupled Logic |
| ECO | Engineering Change Order (bug-fixing during layout) |
| EDA | Electronic Design Automation |
| EDIF | Electronic Data Interchange Format |
| eDRAM | embedded DRAM |
| EIA | Environmental Impact Assessment |
| EIAJ | Electronic Industries Association of Japan |
| EMI | Electromagnetic Interference |
| EMS | Electromagnetic Susceptibility |
| ESD | Electro Static Discharge |
| F | |
| FDDI | Fiber Distributed Data Interface |
| FET | Field Effect Transistor |
| FIFO | First In First Out |
| FPBGA | Fine Pitch Ball Grid Array |
| FPGA | Field Programmable Gate Array |
| FPLD | Field Programmable Logic Device |
| FSM | Finite State Machine |
| G | |
| GPIB | General Purpose Interface Bus |
| GSM | Global System for Mobile Communication |
| GTL | Gunning Transceiver Logic |
| GUI | Graphic User Interface |

| Acronym | Long Form |
|---|---|
| H | |
| HDL | Hardware Description Language |
| HDLC | High Level Data Link Control |
| HHBT | High Temperature High Humidity with Biased Test |
| HSTL | High Speed Transceiver Logic |
| HTOL | High Temperature Operating Life Test |
| I | |
| IBIS | Input/Output Buffer Information Specification |
| IEEE | Institute of Electrical and Electronics Engineers |
| IMAPS | International Microelectronics and Packaging Society |
| IPO | In Place Optimization |
| IrDA | Infrared Data Association |
| ISA | Industry Standard Architecture |
| ITRS | International Technology Roadmap for Semiconductor |
| J | |
| JEDEC | Joint Electronic Devices Engineering Council |
| JPEG | Joint Photographic Experts Group |
| JTAG | Joint Test Action Group |
| K | |
| KGD | Known Good Die |
| L | |
| LCC | Leadless Chip Carrier |
| LEF | Library Exchange Format (library data for the place&route tool) |
| LGA | Land Grid Array |
| LQFP | Low-profile QFP |
| LSB | Least Significant Bit |
| LSD | Least Significant Digit |
| LSSD | Level Sensitive Scan Design |
| LUT | Look-Up Table |
| LVCMOS | Low-Voltage CMOS |
| LVDS | Low Voltage Differential Signaling |
| LVPECL | Low-Voltage PECL |
| LVTTL | Low-Voltage TTL |

| Acronym | Long Form |
|---|---|
| M | |
| MAC | Media Access Control |
| MAC | Multiply Accumulate |
| MCM | Multi Chip Module |
| MCP | Multi Chip Package |
| MDRAM | Multi Port DRAM |
| MIPS | Million Instructions Per Second |
| MPEG | Moving Pictures Experts Group |
| N | |
| NEMI | National Electronics Manufacturing Initiative |
| NRE | Non-Recurring Engineering (Cost) |
| NRZ | No-Return Zero |
| NRZI | No-Return Zero Inverted |
| NTSC | National Television System Comittee |
| O | |
| OBSAI | Open Basestation Architecture Initiative |
| P | |
| PBGA | Plastic Ball Grid Array |
| PCB | Printed Circuit Board |
| PCI | Peripheral Controller Interface |
| PCMCIA | Personal Computer Memory Card International Association |
| PCT | Pressure Cooker Test |
| PDEF | Physical Design Exchange Format (Synthesis to Floorplaner) |
| PECL | Pseudo Emitter Coupled Logic |
| PGA | Pin Grid Array |
| PLCC | Plastic Leaded Chip Carrier |
| PLD | Programmable Logic Device |
| PLL | Phased Lock Loop |
| PWB | Printed Wiring Board |
| Q | |
| QFP | Quad Flat Package |
| R | |
| RAM | Random Access Memory |
| RISC | Reduced Instruction Set Computer |
| ROM | Read Only Memory |
| RTL | Register Transfer Level |

| Acronym | Long Form |
|---|---|
| RTOS | Real Time Operating System |
| S | |
| SATA | Serial ATA |
| SCSI | Small Computer System Interface |
| SDF | Standard Delay Format (delay information for synthesis and simulator tools) |
| SDH | Synchronous Digital Hierarchy |
| SDIP | Shrink Plastic Dual In-line package |
| SEMI | Semiconductor Equipment and Materials International |
| SGRAM | Synchronous Graphics Random Access Memory |
| SIA | Semiconductor Industry Association |
| SIMM | Single In-Line Memory Module |
| SiP | System in a Package |
| SMD | Surface Mount Device |
| SMT | Surface Mount Technology |
| SOC | System on a Chip |
| SOJ | Small Outline J-leaded |
| SOP | Small Outline Package |
| SPICE | Simulation Program with Integrated Emphasis |
| SRAM | Static Random Access Memory |
| SSCG | Spread Spectrum Clock Generation |
| SSO | Simultaneously Switching Outputs |
| SSTL | Stub Series Terminated Transfer Logic |
| STA | Static Timing Analysis |
| S-TSOP | Super Thin Small Outline Package |
| T | |
| TAB | Tape Automated Bonded |
| TBGA | TAB Ball Grid Array |
| TC | Temperature Cycle Test |
| TCP | Tape Carrier Package |
| THT | Through-Hole Technology |
| TQFP | Thin QFP |
| TSOP | Thin SOP |
| U | |
| UART | Universal Asynchronous Receiver/Transmitter |
| USB | Universal Serial Bus |

| Acronym | Long Form |
|---|---|
| USRT | Universal Synchronous Receiver/Transmitter |
| V | |
| VHDL | Very High-Speed Integrated Circuit Hardware Description Language |
| VITAL | VHDL Initiative Towards ASIC Libraries |
| VPS | Vapor Phase Soldering |
| W | |
| WLP | Wafer Level Packaging |
| WS | Wave Soldering |
| WSTS | World Semiconductor Trade Statistics Organisation |
| X | |
| Y | |
| Z | |

# ASIC Technology Handbook

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