

ACCELERATING POWER CONVERSION GROWTH WITH GAN DEVICES AND ECOSYSTEM PRODUCTS

Today, most converters employ switch-mode topologies. At their core, power transistors switch on and off at high frequency, and contribute to a significant portion of power losses. The innovation on power device technology is key for continuous efficiency improvement. After the IGBTs in the 1980s and the superjunction in 1990s, we are now witnessing a leap ahead in the 2020s thanks to SiC and GaN. The implementation of wide bandgap semiconductors into power conversion system could boost energy conversion efficiency to 95%-99% and would save more than 630 TWh of energy every year—a truly substantial savings for the benefit of our society, economy and ecology.

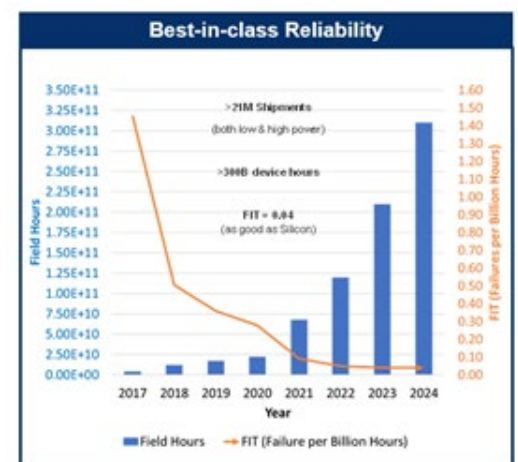
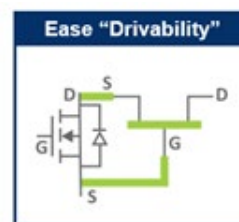
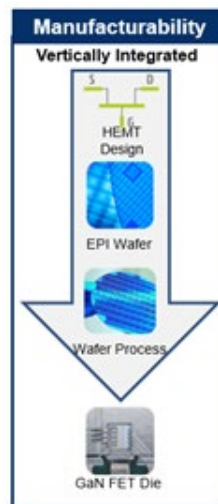
WHAT'S INSIDE

- 02 Executive Summary
- 05 Paralleling Renesas GaN devices for high power
- 07 Reliability of Renesas HV GaN
- 10 Applications and topologies for HV GaN
- 14 Simple platform to replace Silicon & evaluate Renesas GaN
- 16 Portfolio and Packages of Renesas HV GaN

and more >>

Accelerating Power Conversion Growth with GaN Devices and Ecosystem Products

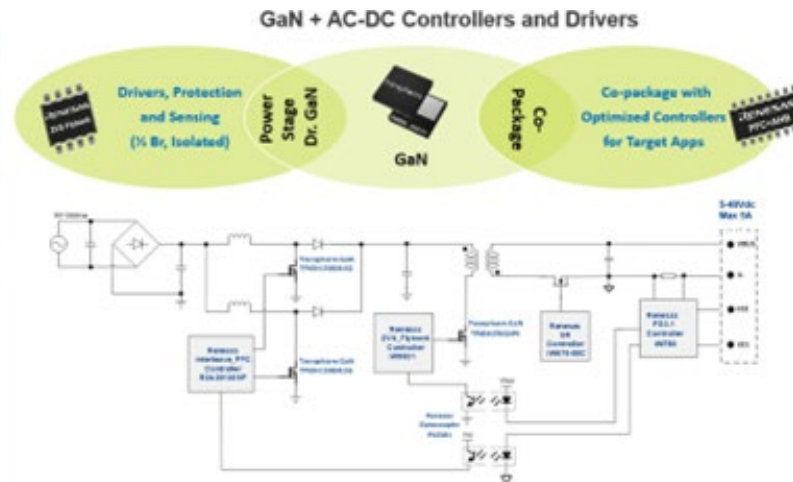
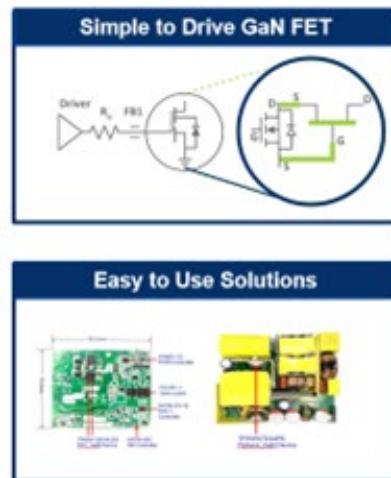
Wide bandgap semiconductors are attractive for power switches because they alleviate the trade-off between conduction and switching losses. Conduction loss increases with device resistance, whereas switching loss increases with device capacitance. Resistance and capacitance are at a trade-off: decreasing resistance needs bigger chip area which inevitably results in higher capacitance (Figure 1). With wide bandgap semiconductors, we can finally alleviate the trade-off and reduce resistance and capacitance at the same time, resulting in a win-win situation: higher efficiency and smaller system size. And this is possible for two reasons: first, wide bandgap semiconductors have higher breakdown field, therefore, they can hold a higher voltage across a smaller distance, minimizing resistance and chip-size. Second, GaN (but not SiC) has a much higher electron mobility than silicon, therefore, can carry the same current with fewer electrons, resulting in lower stored charge and faster switching. In summary, with its fundamental benefits of high electron mobility and high switching speed,



Key differentiating features of Renesas GaN, backed by successful field deployment

Accelerating Power Conversion Growth with GaN Devices and Ecosystem Products

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GaN excels over Si and also SiC in efficiency, power density and cost – not only system cost but now actually device level cost as well, including over Silicon MOSFETs in some applications.

Renesas is a leading GaN manufacturer, supplying high-performance, high-reliability Gallium Nitride (GaN) power semiconductor products over the widest range of applications – from 25 Watts/low power to over 10 kilowatts/high power for market areas including Infrastructure and Computing, Industrial and Renewable, e-Mobility and xEVs, IOT/Consumer (fast

chargers). Renesas GaN is shipping across the power spectrum, from 25W to 10KW, in production with multiple customers across the segments.

Built on the world's leading IP platform covering the full value chain for GaN Power with proprietary epi and wafer fab technology, we are already supplying GaN power conversion products to a large customer base, with more than 20M devices shipped, uniquely in both high and low power with over 300 billion hours in the field.

The success across the power spectrum has come from our fundamentally superior d-mode GaN architecture, with inherent GaN performance and ability to offer the widest range of packages from compact PQFN to the time tested and robust TO leaded for high power and recently an array of surface mount high power packages both with bottom side and top side cooling options. This is simply not possible with other GaN, notably e-mode GaN due to the fundamental device limitations of e-mode GaN. Our robust normally off architecture with an integrated low voltage Silicon

Accelerating Power Conversion Growth with GaN Devices and Ecosystem Products CONTINUED

MOSFET front end, enables our GaN products to be used with off the shelf silicon drivers, complementing the wide package offerings to lend itself to easier design-ins.

Renesas provides customers with a complete ecosystem that includes the GaN power device along with controller and driver ICs and in many cases backed by strong MCU/MPU and other IC product offerings, allowing our customers to benefit from a one-stop shop for their power

conversion and system design needs. Whether the application requires designing a low, mid, or high-power solution, SuperGaN offers the simplicity of drivability. For example, a standard 2V or 4V drive without the need for negative drive and using standard off-the-shelf controllers with integrated drivers for low power and stand-alone silicon gate drivers for mid and high-power applications. In many cases, the driver(s) that designers are using on their current platform don't

have to change. This simplifies design time and reduces time to market, offering a wide variety of package solutions continues to enable customers.

Next we will review key technical product specifications, reliability, key application topologies in low- and high-power, paralleling GaN devices and benchmarking examples.



Providing integrated GaN / widebandgap power conversion solutions

Paralleling GaN FETs in High-Power Applications: PCB Design and Efficiency Insights

Introduction to GaN FET Technology in High-Power Applications

Gallium Nitride (GaN) FETs have increasingly become crucial in high-power electronic applications, including automotive, industrial, renewable energy, and consumer electronics. The high switching speeds, compact form factors, and enhanced thermal performance make GaN FETs superior to traditional silicon-based FETs, particularly in applications that require low conduction losses and high efficiency.

Three primary packages, PQFN, TO220 and TO-247-3L, enable GaN FETs to perform effectively in high-current, high-voltage configurations. The PQFN package integrates a

Direct Plated Copper (DPC) substrate, ensuring efficient thermal dissipation and a compact form factor. For the TO-247-3L package, the 650V D-mode normally-off GaN HEMTs, part of the SuperGaN family, with a low on-state resistance of 15 mΩ, aid in efficiently powering industrial and automotive applications.

Key PCB Design Considerations for Paralleling GaN FETs Symmetrical Circuit Layout and Thermal Management

For high-performance applications, symmetrical PCB layouts are essential to ensure even current distribution, reduce electromagnetic interference (EMI), and

optimize thermal management. This layout symmetry as shown in figures 1, 2 and 3 minimizes the potential for hot spots and improves the FETs' performance stability. The parallel half-bridge circuit, featuring high- and low-side devices, is commonly used for high-power applications, where symmetrical layouts help distribute the heat generated more effectively.

To further support thermal dissipation, GaN FET packages are mounted on large copper plates, and additional thermal vias are included to channel heat away from the FETs. PQFN packages, in particular, benefit from

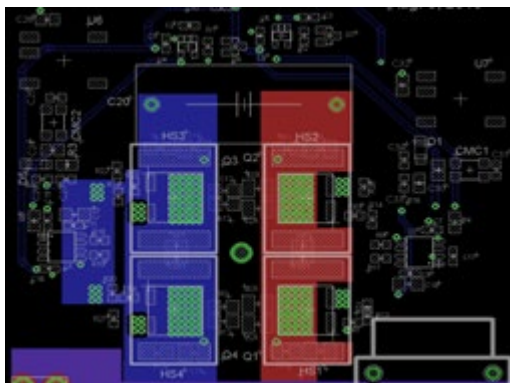


Figure 1

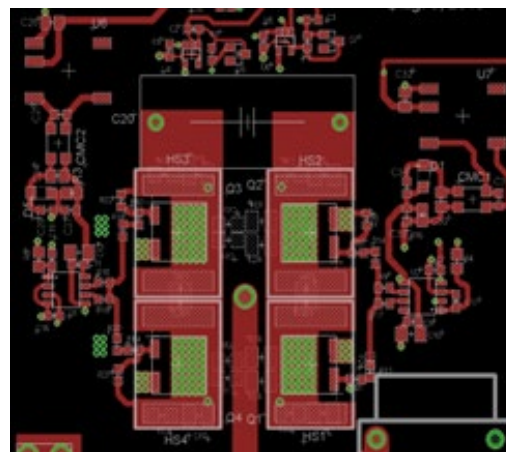


Figure 2

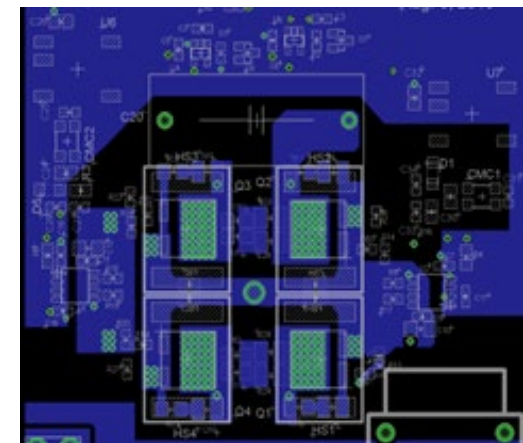


Figure 3

Paralleling GaN FETs in High-Power Applications: PCB Design and Efficiency Insights

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solderable heatsinks that manage power levels up to 2.5 kW, with options to add larger heatsinks for applications exceeding this power range. These design considerations ensure that the devices remain within acceptable thermal limits even at high switching frequencies.

Detailed guidelines on optimal PCB design to parallel Renesas GaN FETs can be found in the PQFN GaN FETs Paralleling PCB app note.

Noise and Voltage Spike Suppression

Paralleling GaN FETs at high power levels can introduce noise and voltage spikes, especially during switching transitions. To mitigate these effects, we recommend:

- **Ferrite Beads:** Installed on gate connections to suppress high-frequency noise
- **RC Snubbers:** Positioned near each FET can reduce voltage spikes during turn-off events

These components effectively limit electromagnetic interference (EMI), ensuring smoother operation in noise-sensitive environments. By combining these methods, the circuit maintains stable performance without substantial voltage overshoot or ringing.

Voltage and Current Stability During Operation

In these high-power circuits, the turn-on and turn-off dv/dt are controlled using gate resistors. This allows the user to achieve a balance of fast transitions and low voltage overshoot. The use of ferrite beads and RC snubbers effectively limits voltage spikes to a safe level for the device. This stability ensures that the circuit can handle high power without compromising on efficiency due to over voltage conditions.

Performance Results of a 30kW Application with Paralleled GaN Devices

Performance of GaN FETs in parallel configuration was tested with a synchronous boost converter to emulate a hard-switched half bridge. The boost converter contained three GaN FETs in parallel, each on the high side and low side of the boost converter. The converter was operated up to a power of 30kW. This arrangement yielded a peak efficiency exceeding **99.3%**, achieved at 240V to 400V operation in boost mode at a frequency of 30 kHz. High efficiency is attributed to the effective current sharing among paralleled FETs and the effective low on-state resistance of the paralleled devices.

To ensure stable performance at such high power, the switching is carefully controlled to maintain uniform current distribution.

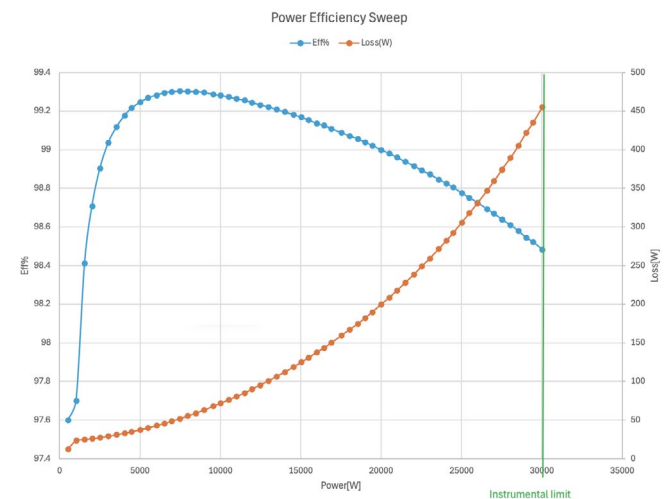


Figure 4. Efficiency curve of a boost converter with 3 GaN FETs in parallel

Synchronization in turn-on and turn-off minimizes the risk of thermal imbalances, with observed junction temperatures kept below 120°C, even at peak output.

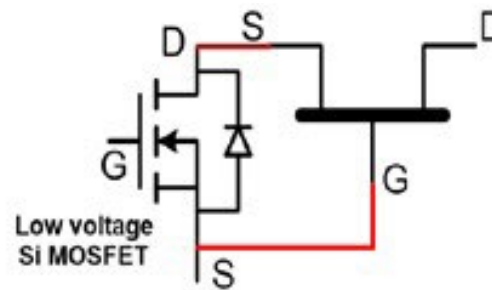
Paralleling GaN FETs has proven effective in delivering high efficiency, thermal stability, and controlled voltage levels in high-power applications. This configuration is ideal for advanced energy systems, automotive applications, and industrial infrastructure, where power densities and reliability are paramount. Moving forward, GaN technology holds promise for even higher frequencies and power capacities, potentially allowing its integration into broader markets such as electric vehicles (xEV) and grid infrastructure.

Renesas GaN Offers Best-in-class Reliability for Demanding Applications

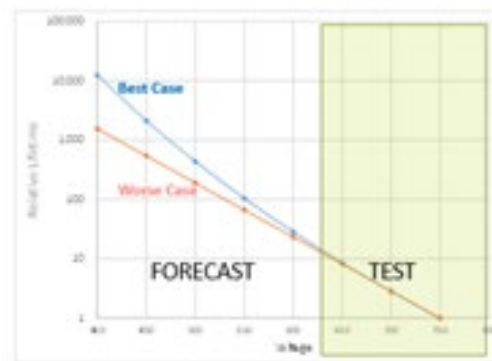
For any power device and especially with new technologies such as GaN-on-Silicon platforms, device and product reliability is extremely critical, as these devices can power products ranging from renewable energy, computing, e-mobility, infrastructure and automotive applications. Renesas' reliability tests have included lifetime testing based on a deep understanding of the physics of failure in addition to qualification tests based on industry standards.

Renesas GaN is built on a robust and proprietary platform with well over a decade of refining to provide the best-in-class reliability, in addition to its best-in-class performance. The approach combines inherently superior GaN devices with an input low-voltage Si MOSFET for driving and ease of driving with standard existing and economical drivers. Essentially, the Renesas high voltage GaN packaged product consists of a normally off device and a low voltage silicon MOSFET in series with a D-Mode GaN HEMT, in a cascode configuration as diagramed.

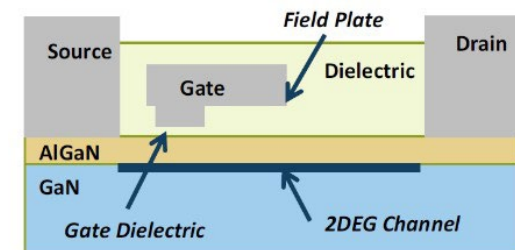
Lifetime testing of the GaN HEMT is the focus of much of our reliability testing, along with the switching related reliability of the two-chip device.



In addition, all Renesas high voltage GaN devices must pass a series of qualification tests as defined in industry standards. The specific tests that are required can vary depending on the package type, and if the device is intended for automotive or industrial (commercial) applications. Not all products are subject to all qualification testing and this list does not include all possible tests that may be conducted, but typical tests can include:

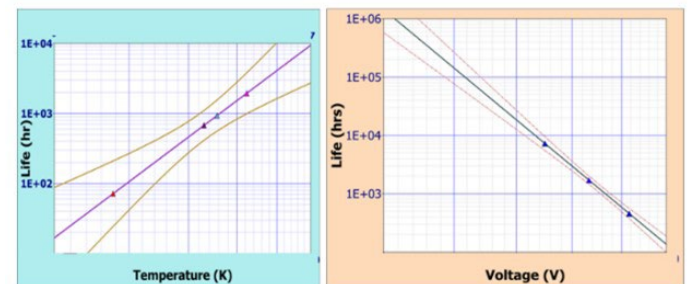


Simplified Cross Section of GaN HEMT



High Temperature Reverse Bias (HTRB), High Temperature Gate Bias (HTGB), High Temperature Operating Life (HTOL), Temperature Cycling (TC), Intermittent Operational Life (IOL), Destructive Physical Analysis (DPA), High Accelerated Stress Test (HAST), High Humidity High Temperature Reverse Bias (H3TRB), Unbiased HAST (UHAST).

Preconditioning and MSL qualification are required as appropriate to the package type.



Renesas GaN Offers Best-in-class Reliability for Demanding Applications

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Lifetime Failure Mode

Accelerated Lifetime Testing (ALT) is the industry accepted method for determining the acceleration factors, infant mortality and device wear out. The important “first step” is to determine the primary failure mode of the device, and the appropriate stress conditions. The simplified cross-section schematic diagram of the GaN device (shown on page 7) shows the important elements of the HEMT. Device failure is dominated by Time Dependent Dielectric Breakdown (TDDDB) of the dielectric material between the Gate/Field Plate and Drain due to the high electric field between the two elements that eventually degrades the dielectric material and causes failure of the device. The physics of this wear out mechanism is common to many (if not most) semiconductor devices. It is important to ensure that all the ALT tests that are run have the same failure mode to ensure accuracy in the results.

Acceleration Factor and Lifetime Determination

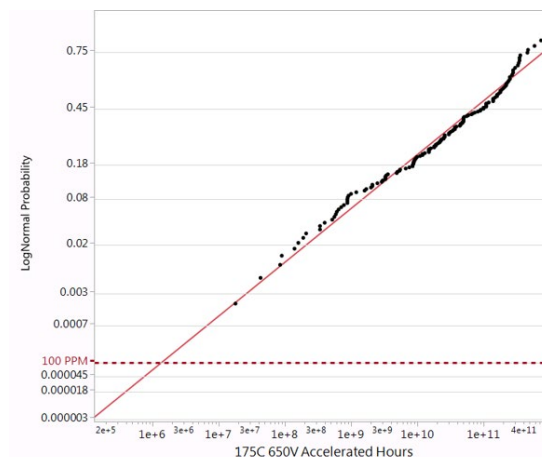
Industry standard methods for determining acceleration factors are employed where applicable. Typical methodology to determine voltage and temperature acceleration is to stress three separate samples of devices at three different voltages and temperatures until a significant number of devices fail, then apply the appropriate model to determine the acceleration factor. When there are

“competing models” the model that produces the “worse” result (shortest lifetime) is the one that is used, in compliance with the principle of conservative reliability engineering. “Cherry picking” models to give an optimistic result is not allowed. Normally at least three lots at three different temperatures and/or voltages are used to determine the acceleration factors. The Arrhenius model is used for temperature acceleration, while an exponential model ($e^{-(Y*\Delta V)}$) is used for voltage acceleration. Other proprietary models may be employed as needed for specialized conditions.

The data from these lots are then combined into what is known as a “Use Plot” that can be used to determine device lifetime under a specific mission profile. Following best practices Renesas reports the 100 ppm lifetime of the device depending on the customer’s application.

Infant Mortality and Early Life Failure Testing

It is critically important to assess the warranty risk during the development of any new device or technology. The testing that is performed to determine the risk of premature failure is referred to as Early Life Failure (ELF) and is designed to assess the risk during the Infant Mortality and Constant Failure region of the bathtub curve. The methodology used is well documented by JEDEC. During life test, described earlier, the acceleration factors are extracted.

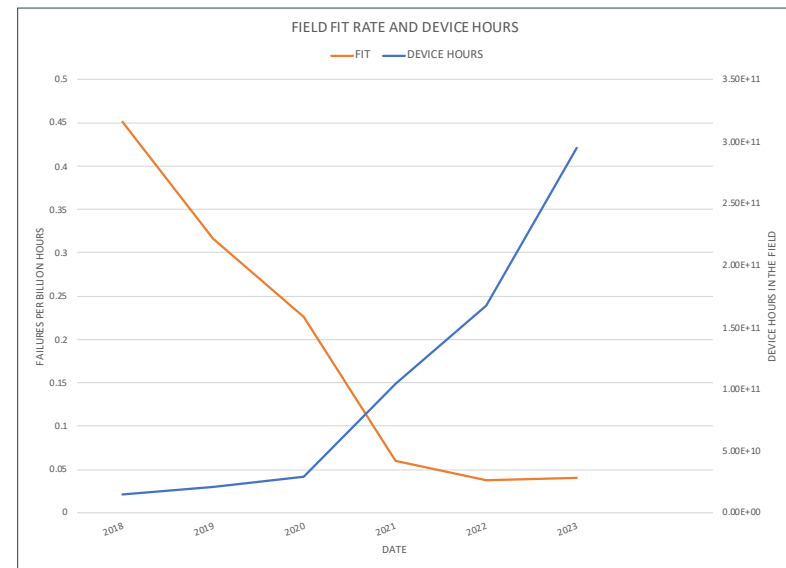
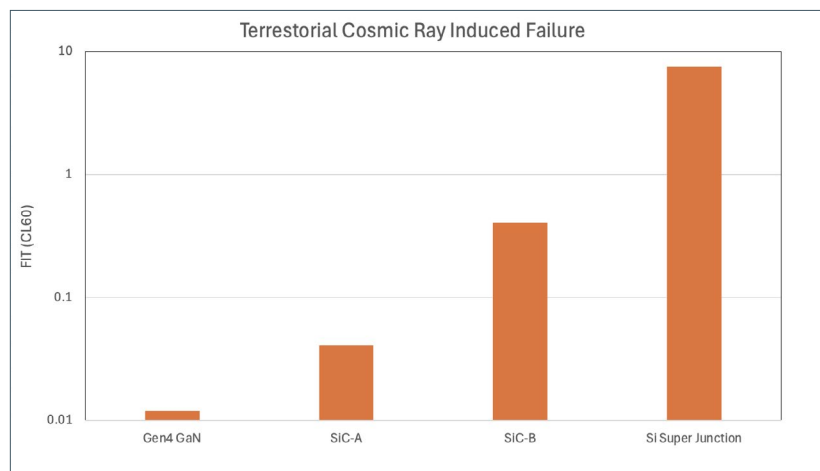


The Weibull shape parameter (m) that determines if the failure rate is changing (increasing or decreasing) with time is also extracted. Additionally, η (η), which is defined as the characteristic lifetime of the Weibull distribution is determined. During ELF testing these acceleration and Weibull parameters are used to build a model that can assess the field failure risk, under a given mission profile.

Single Event Burn Out

Power devices that are used in critical applications exposed to the outside environment are subject to their own failure risks due to exposure to the sun’s radiation or cosmic rays. When protons from these cosmic rays enter the atmosphere, high energy neutrons are generated. Automotive and high-altitude applications are especially prone to this. Renesas device platforms have been tested to determine the risk under terrestrial exposure using appropriate JEDEC standards.

Renesas GaN Offers Best-in-class Reliability for Demanding Applications CONTINUED



Tests have been conducted at the Research Center for Nuclear Physics at Osaka University which involve neutron bombardment to simulate extended exposure to terrestrial radiation. Unlike most silicon and SiC devices, Renesas GaN devices do not require voltage derating to achieve excellent FIT making them suitable for these demanding applications.

Field Reliability - Over 300 billion hours in the field

Renesas tracks product performance in the field, following industry standard methods.

The cumulative device hours in the field are first calculated. Because there is some

uncertainty between when parts are shipped and when they are actually put into service, the device hours are reduced by 50%. This actually increases the reported field failure rate, but is in compliance with the Renesas' policy of conservative reliability engineering and reporting. The calculations assume an exponential function and Poisson distribution with the appropriate value for chi-square (X^2) given the number of failed parts in the field. The calculations are as follows in FITs (failures per billion device hours).

$$\text{Field Failure FIT} = 10^9 \times X^2 / \{2 \times (\# \text{Devices Hours}) \times (50\%)\}$$

Because reported failures and applications between high and low power devices can be expected to vary considerably, Renesas also generates separate reports for power levels greater than 500W and units used in systems at 500W and below. Most recent results can be found on the Renesas website.

Applications and Topologies for HV GaN

Renesas's SuperGaN technology achieves faster switching speed while maintaining the industry's best-in-class $R_{ds(on)}$ stability. Additionally, Renesas GaN products have the widest range of packages from 5x6mm surface mount power quad flat no-lead (PQFN) to through-hole TO-247-x or TO-220 packages. Combined with Renesas' extensive and highly innovative AC/DC controllers, the Renesas GaN product lineup is well suited to provide low cost, highly efficient and high-power density system solutions from 25W to 10kW+ power levels. Renesas GaN products are easy to drive and reliable. Reference designs are available, including comprehensive data on full schematic, suggested layout, form-factor component placement, thermal, efficiency, EMI, transformer design, BOM, and load response. They support power supply designers to meet faster time-to-market goals.

Figure 1 is a 100W design offering size reduction in AC/DC power adaptors for cell phones, tablets, small laptop computers, LED drivers and home portable battery tools. The quasi-resonant flyback (QRF) shown is a popular low cost and high efficiency topology in this power level. The QRF controller operates the SuperGaN FET in critical

A listing of dominant topologies for typical applications and power levels serviced by Renesas GaN is summarized in the table below:

Power Level	Typical Applications	Dominant Topologies
<65W	Power adapters, USB PD Type-C, LED Lighting	QRF, ACF, SSR, PFC Flyback, PFC Buck, PFC Boost
75W to 150W	Adapters, Computer, TV, Appliances, LED Lighting	PFC Boost + QRF or ACF, PFC Flyback, Dual OOP PFC FB, PFC + Forward, PFC + HB-LLC
150W to 750W	Gaming consoles, Computer, TV, Servers, Appliances, e-bike chargers, E 2/3W OBC, UPS, high power Lighting, Microinverters	PFC Boost + DC-DC, Totem-pole PFC + DC-DC, Micro-Inverter, Cycloconverter
>750W to 1.5kW	Computing, Electric 2/3W Chargers, UPS, Residential MPPT & Inverters	Sync PFC Boost + HB-LLC, BL or Totem-pole PFC, HB/FB-LLC, PSFB, Inverters
>1.5kW to 10+kW	Computing, 5G, EV OBC & LBC, UPS, Industrial scale MPPT & Inverters	BL PFC/TTP PFC, PSFB, HB/FB-LLC, Multi-phase HB-LLC Inverters

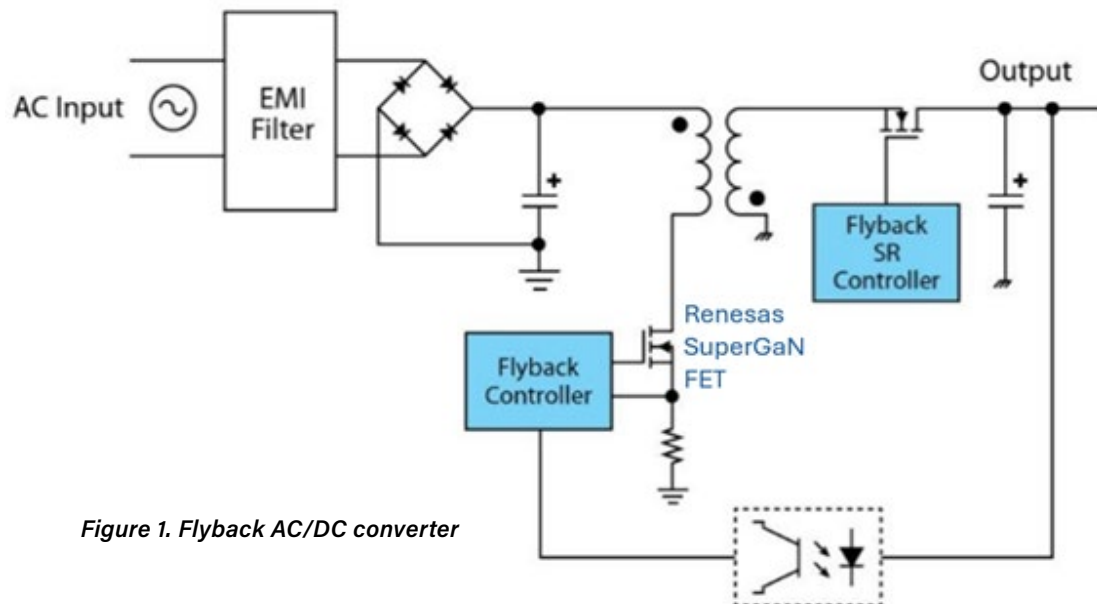


Figure 1. Flyback AC/DC converter

Applications and Topologies for HV GaN CONTINUED

Featured System Designs	Power Board Photos	Key Features & Benefits
EBC10286 240W, 48V USB PD3.1 EPR ZVS Design		Complete, low-cost solution for USB PD 3.1. EPR using ZVS topology to support 240W from wall to batteries
EBC10285 140W, 28V USB PD3.1 EPR High-Efficiency ZVS Design		Adaptive ZVS control, with low-voltage aux-switch, achieves ultra-high efficiency (>94% at 28V5A) with competitive BOM cost. Smart PFC ON/OFF control enables high efficiency at light loads
EBC10287 65W USB PD 3.1 Dual-C-Port ZSP Design		Zero standby power consumption (<5mW at 230Vac), adaptive QR operation and multi-mode control (MMC) optimizes size, efficiency and EMI
EBC10288 65W USB PD 3.1 Ultra-Compact ZSP Design		Zero standby power consumption (<5mW at 230Vac), ultra-compact small size, adaptive QR operation and multi-mode control (MMC) optimizes size, efficiency and EMI
EBC10284 100W USB PD3.1 Dual-C-Port Ultra-Compact, Low-Cost Design		Ultra-compact small size, dual-port USB-C output with single-stage PFC simplifies external circuits and reduces BOM cost
EBC10282 Low-Cost 140W USB PD3.1 EPR 28V Dual-C-Port Design		Single stage sdaptive ZVS control with PFC, achieves ultra-high efficiency (>94% at 28V5A) with dual-C ports and lowest cost

Reference designs for driving HV GaN to achieve Zero Standby Power and Zero-Voltage Switching

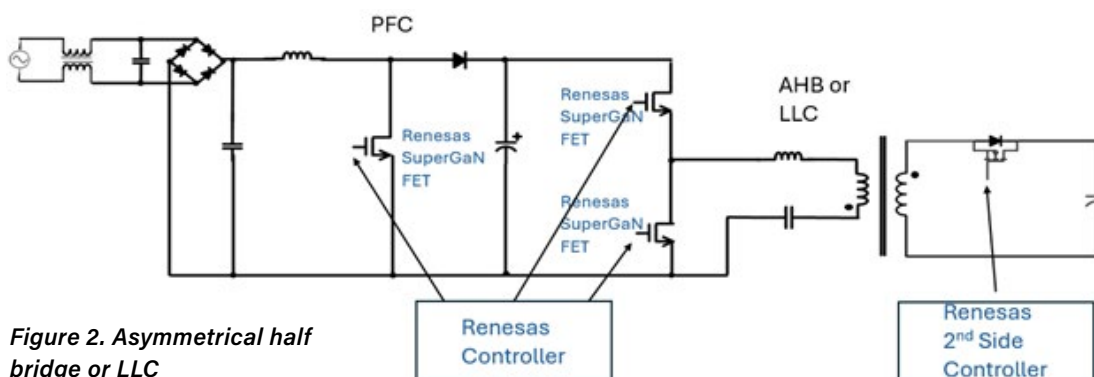


Figure 2. Asymmetrical half bridge or LLC

conduction mode where the FET drain zero voltage is detected after the flyback primary current is reduced to zero before the next switching cycle turn on. With zero voltage switching on (ZVS), QRF can achieve best-in-class efficiency.

AC/DC adapters, except in LED driver applications, are built to suit universal input line voltages, as wide as 90Vac to 264Vac. QRF controllers in the market have difficulty achieving ZVS at high AC line (220~240Vac). Switching loss at high line for these QRF controllers cannot be optimized. Renesas has a line of QRF controllers (for example iW9870) with built in proprietary technology that can achieve ZVS operation at high line, thus further optimizing converter efficiency for both high and low lines.

AC/DC adapters plug into an AC outlet and stay powered all the time. They can consume power in standby mode when not connected to a load. Renesas WattZero™ controller chipsets (eg. iW9870 + iW610 + iW780) can achieve an industry best, virtually zero (<5mW) standby power consumption.

From 100W to 1kW, SuperGaN and controller products are suitable for AC/DC applications, such as powering computers, LCD or OLED TVs, appliances, horticulture LED lighting, gaming consoles, computing

Applications and Topologies for HV GaN CONTINUED

servers, e-bikes, 2/3 wheelers and DC/AC applications like solar panel inverters and home appliances. Starting above 100W, power factor correction (PFC) is a requirement for most applications and a PFC power stage is required to interface with the AC line. For AC/DC applications that require wide output voltage range, like USB power delivery (PD), an asymmetrical half bridge (AHB) output stage provides optimal efficiency, as shown in Figure 2. For applications only requiring constant voltage (CV) or constant current (CC) with limited range of output voltage variation, an LLC output stage is appropriate.

For DC/AC applications in photovoltaic and home appliances, a simple highly efficient half bridge inverter is the key. Figure 3 shows a 700W Renesas inverter solution utilizing a low-end microcontroller. The controller accepts a switching frequency and AC output frequency configurations to operate either in constant output voltage (CV) or constant volt/Hz mode.

For over 1kW loads, applications for SuperGaN and controller products range from computer servers, UPS, onboard chargers (OBC) for electric vehicles and large-scale photovoltaic inverter systems.

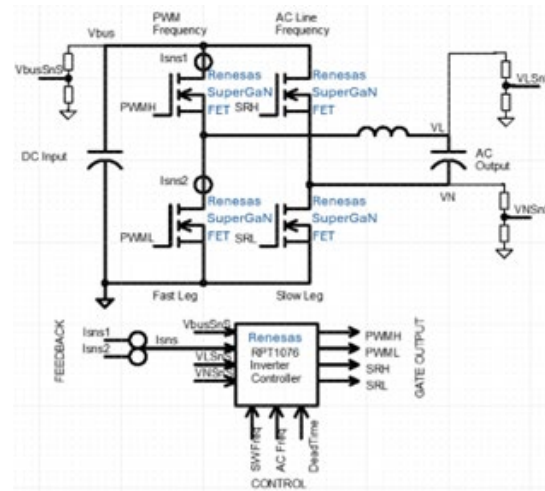


Figure 3. A cost-effective inverter implementation

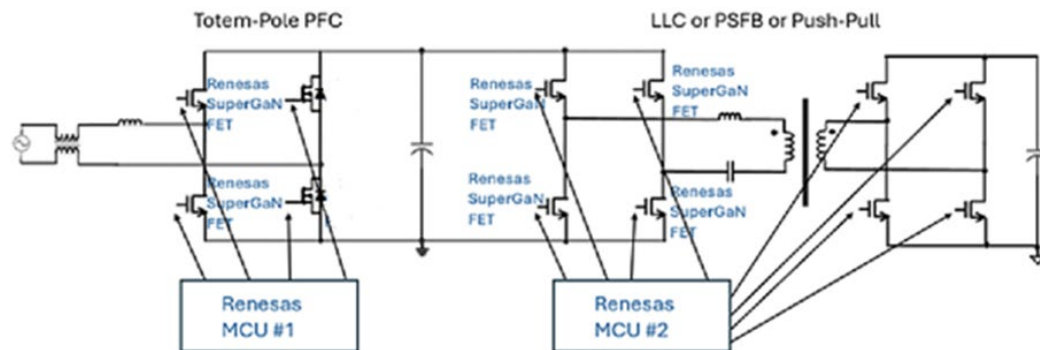
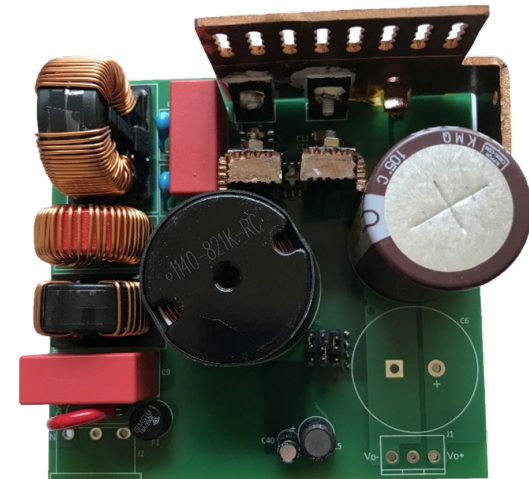


Figure 4. Totem-Pole PFC and DC-DC for high power

Applications and Topologies for HV GaN CONTINUED

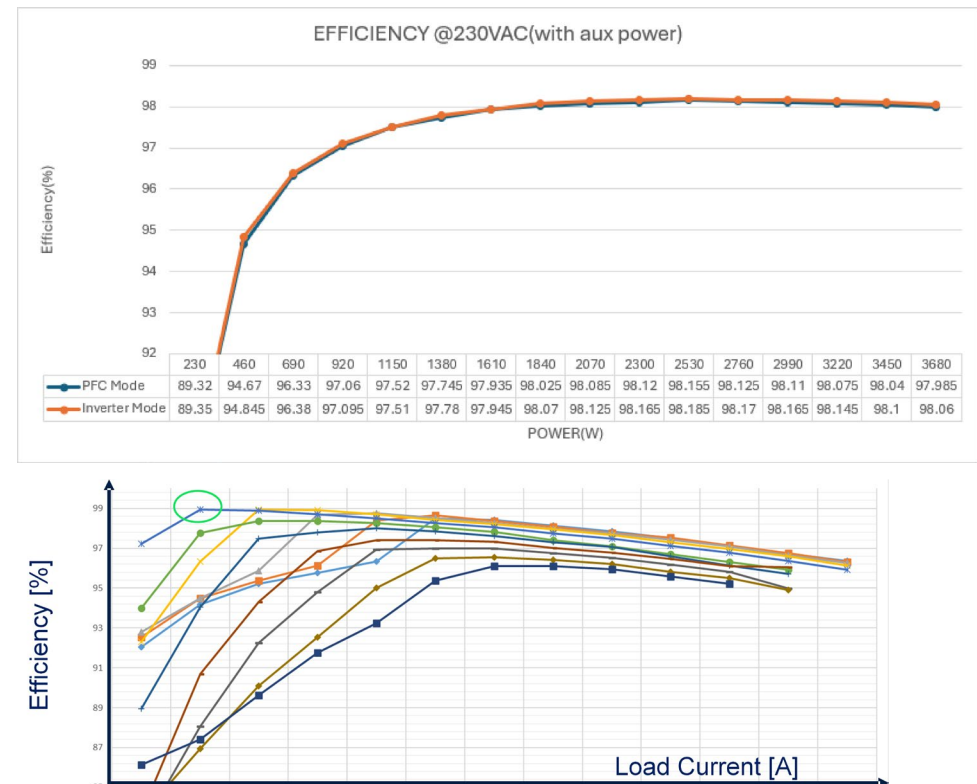
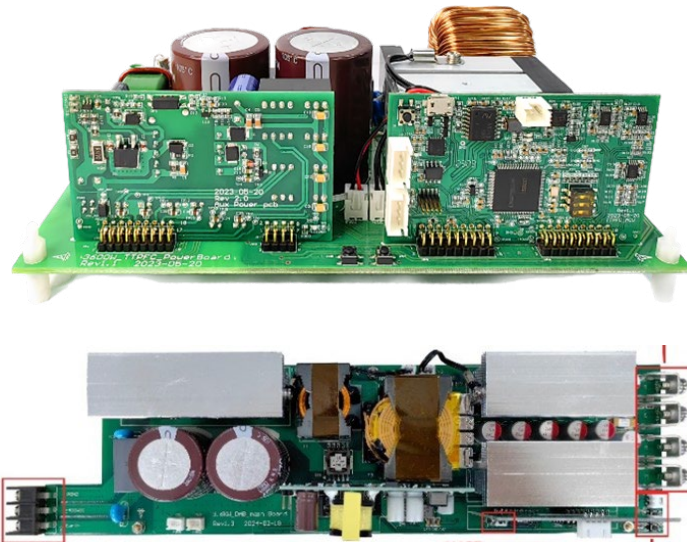


Figure 5. Bi-directional power flow system with Renesas SuperGaN and MCU

These systems usually implement the AC/DC PFC stage using a totem-pole topology. Totem-pole topology with Renesas SuperGaN and controller achieves the highest efficiency for the AC/DC stage. A block diagram is depicted in Figure 4. The DC/DC stage topology can be chosen from LLC resonant converter, DAB (Dual-active Bridge), phase shifted full bridge (PSFB) or a push-pull converter according to the requirements of the load.

Applications in this power range associated with battery energy storage may require bi-directional power flow. Renesas has developed a 3.6kW bi-directional system solution as shown in Figure 5 using a totem-pole PFC and a dual active bridge (DAB), achieving >98% system efficiency for each stage.

These are but a few examples of the extensive offerings from Renesas to enable customers not only with superior GaN devices, but reference solutions with the GaN ecosystem of controllers and digital processors to develop leading edge products with shorter time to market. See more reference solutions on the [Power Adapters and Chargers](#) application page.

Renesas GaN Evaluation System Enables Rapid Benchmarking versus Silicon FETs

GaN power devices have numerous technical benefits over Si power devices. This is evident from comparing the figure of merits of the two device technologies published in data sheets. There are also several system level benefits that can be realized through comprehensive analysis, calculations, simulations and finally testing. However, there is a growing demand from users to be able to quickly evaluate GaN devices in their existing solutions by replacing the Si device. To enable this, Renesas has developed the daughter card TPHDC001 with compatible pin configuration to fit in the Silicon MOSFET TO-220 footprint on the board. TPHDC001 solves the device pin out incompatibility which arises from the difference in device structures of Si and GaN. With TPHDC001, the user can simply install it in place of the existing Si device and proceed with the testing. The advantage of Renesas GaN, that it can be driven by the same gate drive architecture as the existing silicon device, further simplifies the user's effort.

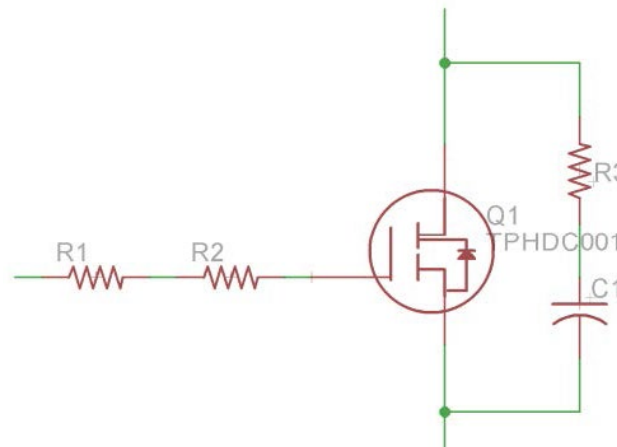


Figure 1. TPHDC001 Schematic

TPHDC001 is a universal evaluation board that can accommodate any of the Renesas GaN devices in the PQFN 8x8 or PQFN 5x6 packages. This flexibility makes it possible for the users to find a best fit for their topology and understand the system tradeoff between the different $R_{ds(on)}$ class or package type.

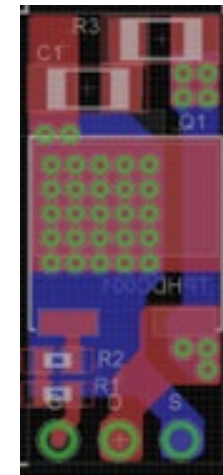


Figure 2. TPHDC001 PCB Layout (GDS output terminal)

Figures 1 and 2 show the schematic and PCB layout of TPHDC001. The pin outs of the board are configured as Gate-Drain-Source (GDS) to match the Si TO-220 footprint. The design also includes a gate resistor to tune the turn on speed of the device, if needed. In addition, a gate ferrite bead is provided to filter any noise on the gate-source signal. A provision for a snubber is made in case the topology is prone to excessive drain-source voltage overshoot and ringing.

Renesas GaN Evaluation System Enables Rapid Benchmarking versus Silicon FETs

CONTINUED

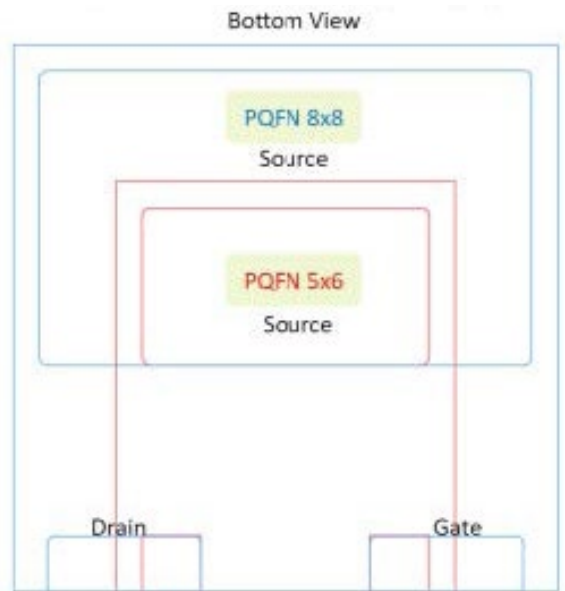


Figure 3. Device Landing Pattern



Figure 4. TPHDC001 Top View



Figure 5. TPHDC001 Bottom View

Figure 3 shows the device landing pattern on the PCB and how it accommodates both the PQFN 8x8 and 5x6 devices.

The daughter cards are shown in Figures 4 and 5 with the device mounted. The exposed copper shown in figure 5 is designed for users to install a heatsink for high power testing purposes.

A similar approach can be used to test Renesas GaN devices in Silicon sockets with TO-247-3 packages. In this case, Renesas has mounted the GaN TOLL package on a daughter card which is pin-pin and dimensionally compatible with the TO-247-3 Silicon Power Devices.

Renesas GaN Product Portfolio Enables a Wide Range of Applications

Renesas offers one of the broadest portfolios of power range and package options in the industry. From the tiny SMD PQFN 5x6 mm² packages to the leaded TO-247-x packages, Renesas GaN can cover power levels from a low 25W to 10KW+, hence addressing numerous applications.

A featured listing of the Renesas GaN portfolio is in the table. For the latest products and more information, click the link below:

[Gallium Nitride \(GaN\)
Power Solutions | Renesas](#)

Part Number	Vds min (V)	RDSON (Typ) (mΩ)	RDSON (max) (mΩ)	Id max @ 25°C (A)	Pkg. Type
TP65H015G5WS	650	15	18	95	TO-247
TP65H035G4QS	650	35	41	46.5	TOLL
TP65H035G4WS	650	35	41	46.5	TO-247
TP65H035G4WSQA	650	35	41	46.5	TO-247
TP65H035G4YS	650	15	18	95	TO-247
TP65H050G4BS	650	50	60	34	TO-263
TP65H050G4QS	650	50	60	34	TOLL
TP65H050G4WS	650	50	60	34	TO-247
TP65H050G4YS	650	50	60	34	TO-247-4L
TP65H070G4LSG	650	72	85	29	PQFN88
TP65H070G4LSGB	650	72	85	29	PQFN88
TP65H070G4PS	650	72	85	29	TO-220
TP65H070G4QS	650	72	85	29	TOLL
TP65H070G4RS	650	72	85	29	TOLT
TP65H100G4LSGB	650	92	110	18.9	PQFN88
TP65H100G4PS	650	92	110	18.9	TO-220
TP65H150BG4JSG	650	150	180	16	PQFN56
TP65H150G4LSG	650	150	180	16	PQFN88
TP65H150G4PS	650	150	180	16	TO-220
TP65H300G4JSGB	650	240	312	6.5	PQFN56
TP65H300G4LSG	650	240	312	6.5	PQFN88
TP65H300G4LSGB	650	240	312	6.5	PQFN88
TP65H480G4JSG	650	480	560	3.6	PQFN56
TP65H480G4JSGB	650	480	560	3.6	PQFN56

Renesas GaN Product Portfolio Enables a Wide Range of Applications CONTINUED

The package footprints are shown in the figure below:

Package Type	Renesas Branded Image
TO-220	
TO-263	
TO-247	
TO-247-4L	
TOLT	
TOLL	
PQFN-56 Performance	
PQFN-88 Performance	

Renesas GaN is unique in the range of packages as seen to the left. Its versatility in different PQFN packages is even more interesting, in that, the 8-pin PQFN packages have an industry standard footprint, whereas the performance-package version is a 3-pin PQFN with a larger thermal pad. The industry standard footprint allows customers to have a pin-to-pin GaN with e-mode products, whereas the Performance Package allows for higher efficiency, lower temperature and better EMI footprint with the same $R_{ds(on)}$. Another interesting feature or specification of the PQFN packages is the ability for Renesas to use MOSFETs with V_{th} and $V_{gs(max)}$ depending on the gate driver desired by the customers. Designers can be accommodated whether they need pin-to-pin operation with e-mode GaN products using a 6V gate driver or want to drive the GaN with standard Silicon gate drivers without any

modifications, protection or level shifting. This flexible approach saves components, space and efficiency, not to mention the additional cost and reliability concerns. Refer to the table below.

While the PQFNs can be made pin-to-pin with e-mode GaN devices, the TO-247-4 are compatible with industry standard SiC power devices and can be driven with even simpler gate drivers and lower current.

Additionally, Renesas GaN is available in a variety of industry standard packages such as TOLL (TO-Leadless), TOLT (TO-Leaded Topside Cooling), TO-220, TO-247-3 and some DxPAKs for certain GaN SKUs.

All-in-all, Renesas with the addition of best-in-class 650V/700V GaN power device portfolio from Transphorm, will enable efficient, smaller and cost-effective products that are robust and reliable.

Package Type	GaN FET	PQFN 5x6	PQFN 8x8	Features
8-pin "Industry"				- Pin-to-pin Compatible with e-mode - Includes Kelvin Sense - Improved immunity vs. e-mode - 12V $V_{gs(max)}$ - E-mode drive compatible
3-pin "Performance"				25% larger pad size compared to industry - Best heat dissipation & reliability in industry - Improved EMI 18V+ $V_{gs(max)}$, compatible with Si FET drivers - Dual foot-print i.e. 5x6 can fit in 8x8 socket



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At Renesas we continuously strive to drive innovation with a comprehensive portfolio of microcontrollers, analog and power devices. Our mission is to develop a safer, healthier, greener, and smarter world by providing intelligence to our four focus growth segments: Automotive, Industrial, Infrastructure, and IoT that are all vital to our daily lives, meaning our products and solutions are embedded everywhere.

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