Picking your package

Jitesh Shah looks at how to improve return loss performance in wire bond packages for 10Gbps SerDes applications

Signal integrity products demand high-performance from the package interconnects but cannot sustain expensive packaging technologies. These devices will soon be used to condition or buffer signals at data rates of 10Gbps and beyond. At these rates, the unit interval for each bit is much smaller with rise and fall times of signals approaching 20-30ps range. Selecting the right package interconnect structure to effectively transmit these signals and minimise signal integrity concerns such as poor return loss, increased crosstalk, impedance discontinuities etc. is crucial. For low cost applications, wire bond packages are the preferred alternative to relatively expensive flip-chip packages, but lack the design flexibility of implementing large I/O count, controlled impedance interconnects and efficient power delivery to the chip.

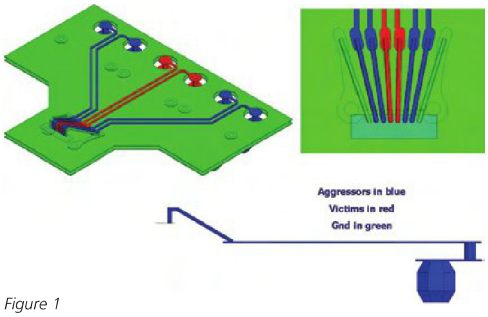

Figure 1

Here we discusses one aspect of meeting the 10Gbps SerDes specification in wire bond packages by optimising the impedance discontinuities within the package and improving its return loss performance.

Differential impedance

A typical SerDes channel involves information exchange between the transmitter and receiver using complimentary signals on two separate interconnect structures. The physical layer between the two endpoints consists of a transmitter device packaged in a wire bond or flip-chip package attached to a daughter-card. The daughter-card is plugged into the backplane through a connector. The routing on the backplane connects to one or a series of connectors with daughter cards plugged in. Receiver devices, also packaged in wire bond or flip-chip packages are located on the daughter cards.

These multiple transitions in a channel will affect signal integrity performance if not designed correctly. At 10Gbps and beyond, proper interconnect design by minimising impedance discontinuities becomes an important consideration in improving system performance. The transceiver packages present a significant bottleneck to superior return loss performance because of the numerous discontinuity regions within a package.

A SerDes channel is typically designed to a differential impedance of 100Ω. Since differential signalling follows odd-mode propagation, the odd-mode impedance of each line of a differential pair needs to be 50Ω. The signal on each line of a differential pair needs to see a constant impedance of 50Ω to minimise return loss and maximise Odd-mode impedance for a loss-less system is defined as performance.

In order to optimise the impedance of each line, all four components need to be balanced to achieve 50Ω impedance. For differential pairs, with each signal within a pair routed as a single-ended signal, the L12 and C12 components are non-existent and Zodd is a simply a square root of the self L/C.

1st pass package

A section of a typical wire bond package with three differential pairs is shown in Figure 1. The transmitter pairs are shown in blue with the centre receiver pair in red. The package substrate is a conventional 4-layer substrate with microstrip traces on the top layer, power/ground on layers two and three and solder balls on the last layer. This first pass design will be optimised to meet the return loss target of -15dB at the fundamental frequency and -10dB at the first harmonic frequency of the data rate.

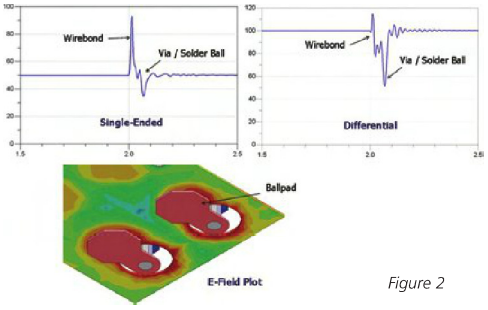

Figure 2

A typical wire bond package can be split into three impedance zones; the predominantly inductive wire bond region, the transmission line region of the trace routing and the capacitive solder ball and via region.

TDR response

The Time Domain Reflectometry (TDR) technique is used to monitor the impedance a signal encounters from the chip to the PCB. Figure 2 shows the TDR response of each line in the differential pair driven as a single-ended signal and also as a differential signal. Only one pair from Figure 1 is used for TDR analysis with the other pairs grounded, ignoring the impact of crosstalk on the TDR response.

The single-ended TDR plot shows the predominantly inductive, high impedance wire bond region of the interconnect structure followed by a small transmission line segment which is followed by the capacitive, low impedance via and solder ball region. The inductive wire bond spike is less pronounced when the same structure is driven differentially because of the strong mutual inductive coupling in the wire bond region of the differential pair. The capacitive dip is significantly worse due to the double multiplier of the mutual capacitance in the differential setup. Removing the excess capacitance from the via/solder ball region is critical in bringing the differential impedance in line with 100Ω.

Figure 2 also shows the E-field plot of the solder ballpad region with strong E-field concentration right above the ballpad.

TDR performance

Figure 3 shows the changes made to the original layout (in the solder ballpad/via region) and its impact on differential TDR performance. Holes slightly bigger than the ballpads are implemented in Layout_2 in the metal layer above the solder ballpads. The capacitive dip in the original layout is now smaller by about 20Ω. Another attempted modification originating from Layout_2 is the change in via orientation from loosely coupled to tightly coupled as shown in Layout_3. The intent of the tightly coupled via is to improve the crosstalk performance of the differential pair. It has been proven in a separate study that the crosstalk performance improvement is marginal and is not pursued for the rest of this study. The pink

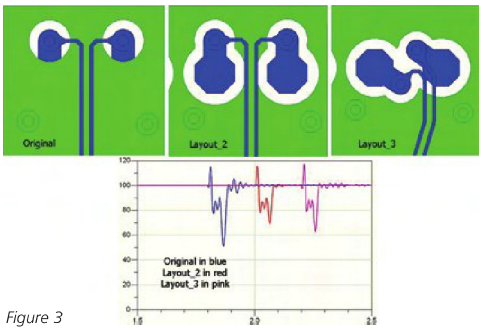

Figure 3

waveform for Layout_3 does show a slightly worse capacitive dip because of the extra capacitive coupling between the two vias.

Figure 4 shows the impact on return loss performance with each subsequent modification. The overall return loss is the worst for the original layout followed by Layout_3. Layout_2 shows the best overall return loss which directly correlates to its TDR performance.

Return loss for Layout_2 at 5GHz is -16dB and at 10GHz is -14dB which handily meets the target of -15dB at the fundamental frequency and -10dB at the first harmonic frequency for 10Gbps SerDes interface.

Die pad ring layout

To minimise inter-pair crosstalk, it is ideal to have each differential pair on the chip separated by a return pad. This is critical when edge rates are in the order of 20-30ps which can severely deteriorate

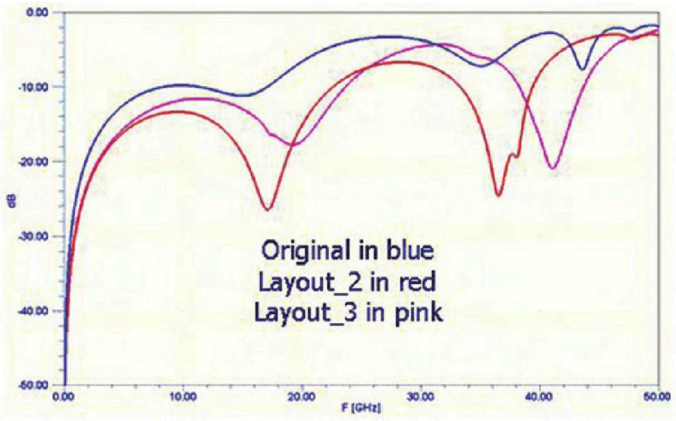

Figure 4

receiver performance due to aggressor-victim crosstalk. Keeping the via and solder ball pad region consistent with Layout_2, Figure 5 shows two additional changes in the package layout with respect to the chip to package wire bond connections.

Figure 6 shows the differential TDR and return loss performance of the three layouts. The response for Layout_2 in blue is the same as shown before. Layout_4 has slightly better TDR performance due to the relatively smaller inductive discontinuity and its impact in frequency domain is unchanged. Layout_5 TDR response shows almost 2x the inductive spike due to the wire bonds compared to the other two layouts. The direct impact of long wire bonds on return loss performance deterioration is also shown in Figure 6 below.

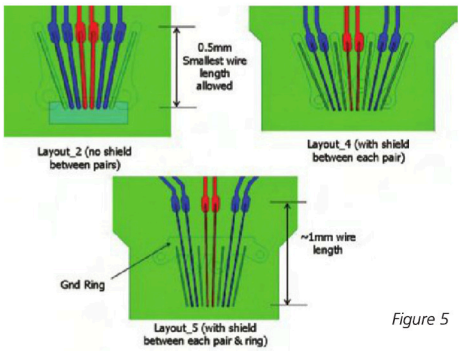

Figure 5

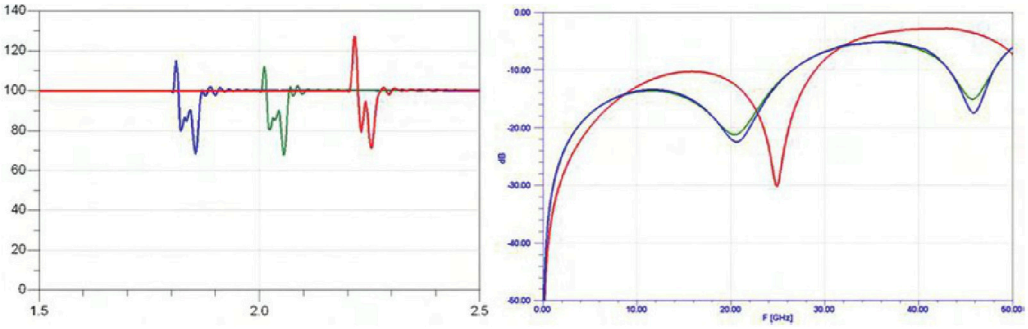

Figure 6

In this article we have applied optimisation techniques to a relatively rigid package solution typically used for signal conditioning type products. We've identified the two major discontinuity regions in a wire bond package and looked at techniques in optimising the wire bond package layout for data rates in the 10Gbps range.

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