1.8-MHz, 48-V Resonant VRM: Analysis, Design, and Performance Evaluation

Laszlo Huber[1], Kevin Hsu[2], Milan M. Jovanović[1], Dennis Solley[3], Gennady Gurov[3], and Robert Porter[3]

[1] Delta Products Corporation
Power Electronics Laboratory
P.O. Box 12173
5101 Davis Drive
RTP, NC 27709, U.S.A.

[2] Delta Electronics, Inc.
DC/DC Engineering BU
3 Tung Yuan Road
Chung Li Industrial Zone
Taoyuan Shieh, Taiwan, R.O.C.

[3] Advanced Energy Industries, Inc.
1625 Sharp Point Drive
Fort Collins, CO 80525, U.S.A.

Abstract - A detailed analysis of operation and a basic design procedure for a new high-frequency (HF) resonant-converter technology with phase-shifted regulation is presented. The new HF resonant technology has a good potential to be a cost-effective solution for the voltage regulation modules (VRMs) for the next generations of microprocessor systems. The new HF resonant technology is employed in the development of a 1.8-MHz, 48-V, 130-W (0.95-1.7 V, 100 A) VRM. Experimental results are provided.

I. INTRODUCTION

To further increase the processing speed and efficiency, future generations of microprocessor systems require lower operating voltages (below 1 V) at higher load currents (above 130 A) with high slew rates (up to 150 A/μs) [1]. High load currents with high slew rates and tighter output-voltage regulation windows require voltage regulation modules (VRMs) with fast transient responses. To achieve a fast transient response, the power conversion must be performed at higher switching frequencies (above 1 MHz). Higher switching frequencies enable controls with higher bandwidth feedback, which in turn require less output capacitance. As a result, only surface mount ceramic capacitors can be used at the output, which are less expensive and potentially more reliable than the commonly used electrolytic and tantalum capacitors. Further, at increased power levels, the 48-V distribution bus voltage is more feasible than the 12-V distribution bus voltage in order to keep the distribution losses low, especially for the high-end server and workstation applications [2]. To meet all these requirements, new high-performance VRMs are needed.

Recently, a new high-frequency (HF) resonant-converter technology with phase-shifted regulation was introduced by Advanced Energy (AE) [3], [4]. AE's new HF resonant technology has proven to be a cost-effective solution for VRMs for the next generation of microprocessor systems.

To facilitate the understanding of AE's new resonant technology, in this paper a detailed analysis of operation and a basic design procedure for AE's HF resonant converter with phase-shifted regulation are presented. The new HF resonant-converter technology with phase-shifted regulation is employed in the development of a 1.8-MHz, 48-V, 130-W (0.95-1.7 V, 100 A) resonant VRM.

The paper is organized as follows. In Section II, a detailed analysis of operation is performed. In Section III, a basic design procedure is given. The implementation of the 1.8-MHz, 48-V, 130-W resonant VRM is presented in Section IV. Experimental results are provided in Section V.

II. ANALYSIS

A. Principle of Operation

The simplified circuit diagram of AE's new resonant converter with phase-shifted regulation is shown in Fig. 1. This is an isolated converter with a half-bridge inverter on the primary side and a current-doubler rectifier on the secondary side. The primary-side half-bridge inverter operates in open loop with 50% duty cycle and generates a rectangular (trapezoidal) ac voltage. The secondary-side current-doubler rectifier uses synchronous rectifiers Q_1 and Q_2. Diodes D_1 and D_2 represent the body diodes of the synchronous rectifiers. For the resonant operation, an external inductor L_{ext} is added in series with the transformer primary winding, and capacitors C_1 and C_2 ($C_1 = C_2 = C$) are added in parallel to the synchronous rectifiers.

To simplify the analysis, it is assumed that output-filter inductances L_{F1} and L_{F2} and output-filter capacitance C_F are sufficiently large, so that they can be represented with current sources $I_o/2$ and a voltage source V_o, respectively, as shown in the equivalent circuit in Fig. 2. Also, it is assumed that the synchronous rectifiers Q_1 and Q_2 are ideal, except for their output capacitances, which are included into the parallel

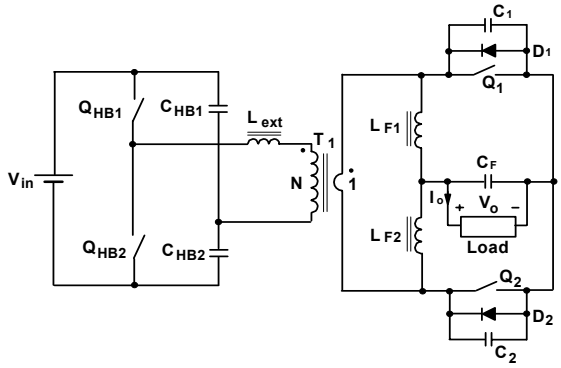

Fig. 1 Simplified circuit diagram of AE's new resonant converter

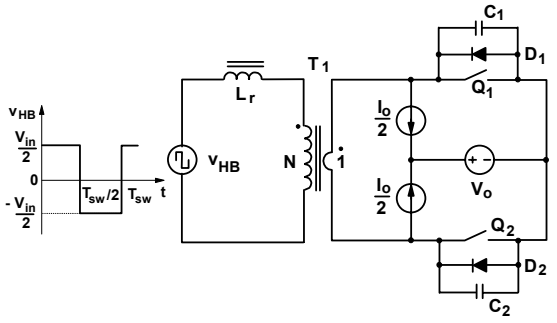

Fig. 2 Equivalent circuit of AE's new resonant converter

resonant capacitances C_1 and C_2. Finally, it is assumed that the magnetizing inductance of transformer T_1 is sufficiently large, so that it can be neglected, while the leakage inductance of the transformer is lumped with external inductance L_{ext}. The total primary-side inductance is denoted as resonant inductance L_r, as shown in Fig. 2. For simplicity, in Fig. 2, the primary-side half-bridge inverter in Fig 1. is replaced by a rectangular ac voltage source v_{HB}. To further simplify the analysis, transformer T_1 in Fig. 2 is eliminated by transferring the whole primary-side circuit to the secondary side, as shown in Fig. 3. In Fig 3, the transferred L_r from the primary side to the secondary side is denoted as L, while the transferred ac voltage source is denoted as v_s.

Under steady-state operation, six topological stages can be identified within a switching cycle T_{sw}, as shown in Fig. 4. These six topological stages can be arranged in two modes of operation. In the first mode of operation, the sequence of topological stages is (a)→(b)→(a)→(d)→(e)→(d), while in the second mode of operation the sequence of topological stages is (a)→(b)→(c)→(d)→(e)→(f). Key waveforms in the two modes of operation are presented in Figs. 5 and 6. In Mode I, shown in Fig. 5, the resonant voltage on capacitors C_1 and C_2 reaches zero before the ac voltage source v_s changes direction, while in Mode II, shown in Fig. 6, the resonant voltage on capacitors C_1 and C_2 reaches zero after the ac voltage source v_s changes direction. In Fig. 5, the solid-line and dotted-line waveforms of inductor current i_L and capacitor voltages v_{C1} and v_{C2} illustrate the operation at maximum load and zero load, respectively. In Fig. 6, only the waveforms at maximum load are presented. Initial values of inductor current i_L and capacitor voltages v_{C1} and v_{C2} in each topological stage are also shown in Fig. 4.

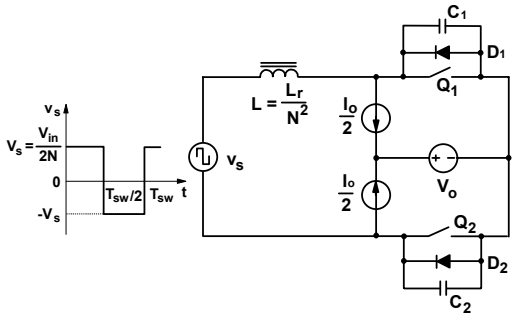

Fig. 3 Simplified equivalent circuit of AE's new resonant converter

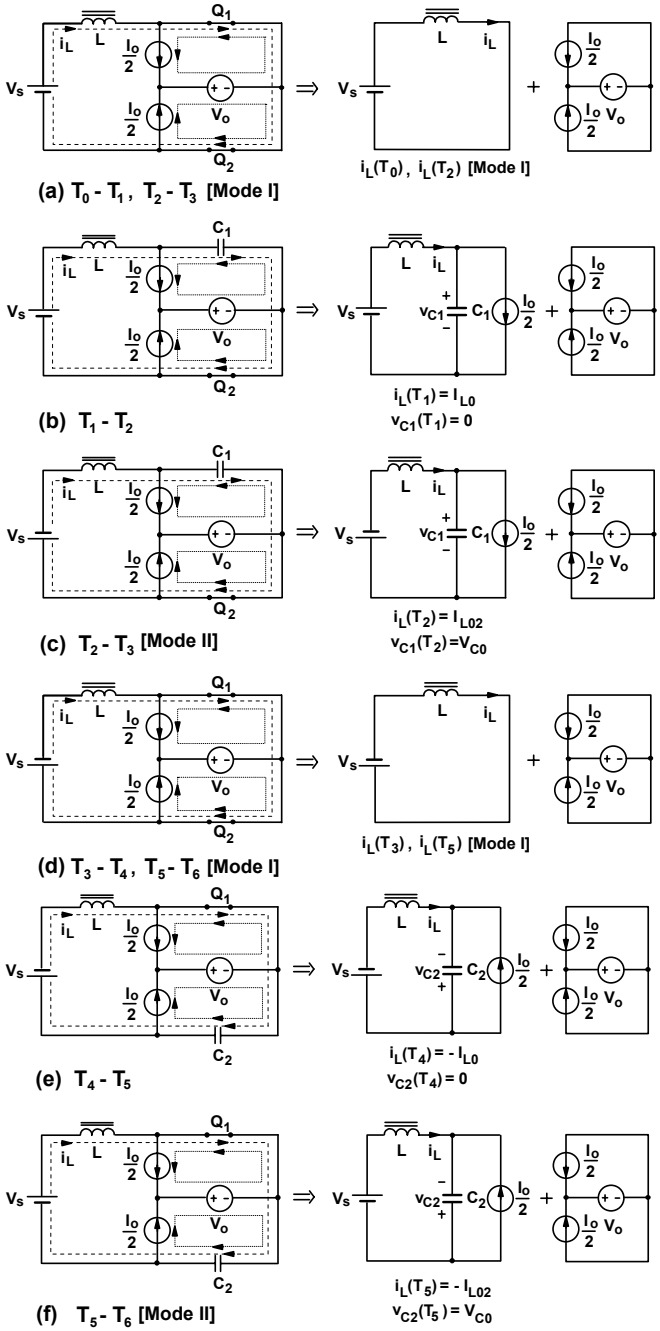

Fig. 4 Topological stages

During interval $[T_0 - T_1]$, Fig. 4(a), both switches, Q_1 and Q_2, are on and the inductor current linearly increases as

$$i_L(t) = i_L(T_0) + \frac{V_s}{L}(t - T_0)\,, \tag{1}$$

At $t = T_1$, switch Q_1 turns off and a resonance starts between L and C_1. The equivalent resonant circuit is shown in Fig. 4(b). This is a series resonant circuit with a capacitor-parallel load. The initial conditions are

$$i_L(T_1) = I_{L0} \qquad \text{and} \qquad v_{C1}(T_1) = 0\ . \tag{2}$$

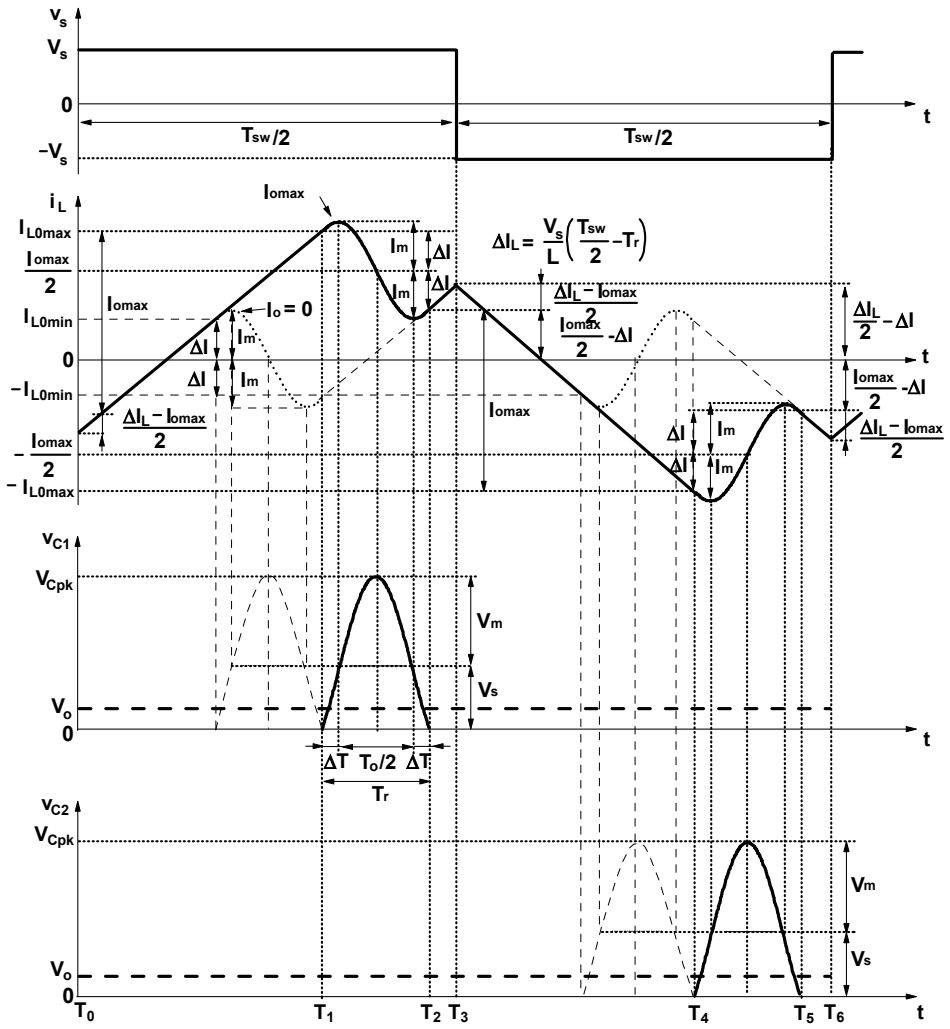

Fig. 5 Key waveforms in Mode I

During the resonance, the inductor current and the capacitor voltage vary as [5]

$$i_L(t) = \frac{I_o}{2} + \Delta I \cdot \cos \omega_o (t - T_1) + \frac{V_s}{Z_c} \cdot \sin \omega_o (t - T_1) \ , \quad (3)$$

and

$$v_{C1}(t) = V_s - V_s \cdot \cos \omega_o (t - T_1) + Z_c \Delta I \cdot \sin \omega_o (t - T_1) \ , \quad (4)$$

where ΔI is defined as

$$\Delta I = I_{L0} - \frac{I_o}{2} \ ; \quad (5)$$

$$\omega_o = \frac{2\pi}{T_o} = \frac{1}{\sqrt{LC}} \quad (6)$$

is the angular resonant frequency, and

$$Z_c = \sqrt{\frac{L}{C}} \quad (7)$$

is the characteristic impedance of the series resonant circuit in Fig. 4(b). Using the trigonometric angle-sum and angle-difference relationships, (3) and (4) can be rewritten as

$$i_L(t) = \frac{I_o}{2} + I_m \cdot \cos[\omega_o (t - T_1) - \Delta\theta] \ , \quad (8)$$

and

$$v_{C1}(t) = V_s + V_m \cdot \sin[\omega_o (t - T_1) - \Delta\theta] \ , \quad (9)$$

where

$$V_m = \sqrt{V_s^2 + (Z_c \Delta I)^2} \ , \quad (10)$$

$$I_m = \frac{V_m}{Z_c} \ , \quad (11)$$

and

$$\Delta\theta = \omega_o \Delta T = \text{atan} \frac{V_s}{Z_c \Delta I} \ ; \quad 0 \le \Delta\theta \le \frac{\pi}{2} \ . \quad (12)$$

The relationship between V_m, V_s, $Z_c \Delta I$, and $\Delta\theta$, defined in (10) and (12) is also shown in Fig. 7.

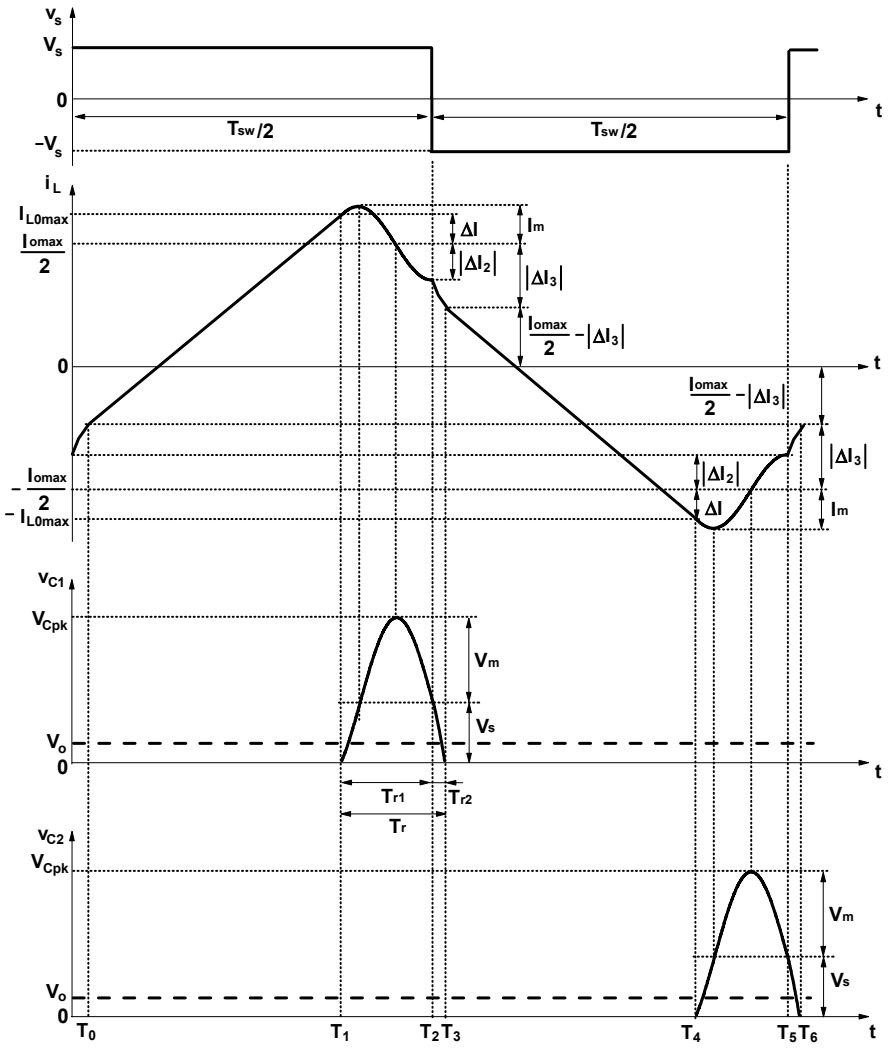

Fig. 6 Key waveforms in Mode II

The sinusoidal waveforms of the inductor current and capacitor voltage determined in (8) and (9), respectively, can be easily recognized in Figs. 5 and 6 during interval $[T_1 - T_2]$. In Fig. 5, interval $[T_1 - T_2]$ is the total resonant interval,

$$T_r = \frac{T_o}{2} + 2 \cdot \Delta T \quad . \tag{13}$$

At the beginning and at the end of the resonant interval T_r in Fig. 5, the resonant-inductor current is determined as

$$i_L(T_1) = \frac{I_{o\max}}{2} + \Delta I \quad \text{and} \tag{14}$$

$$i_L(T_2) = \frac{I_{o\max}}{2} - \Delta I \ , \tag{15}$$

respectively, whereas, the resonant-capacitor voltage is equal to zero. Therefore, at $t = T_2$, switch Q_1 can be turned on with zero-voltage switching (ZVS). If $T_2 < T_3$, from T_2 until the end of the positive half switching cycle the inductor current linearly increases with the same slope as during interval $[T_0 - T_1]$.

In Fig. 6, interval $[T_1 - T_2]$ is only the first part, T_{r1}, of the total resonant interval T_r. At $t = T_2$, the resonant-inductor current and resonant-capacitor voltage have the values

$$i_L(T_2) = \frac{I_o}{2} + I_m \cdot \cos[\omega_o T_{r1} - \Delta\theta] = \frac{I_o}{2} + \Delta I_2 = I_{L02} \tag{16}$$

and

$$v_{C1}(T_2) = V_s + V_m \cdot \sin[\omega_o T_{r1} - \Delta\theta] = V_{C0} \ , \tag{17}$$

respectively. At $t = T_2$, ac voltage source v_s changes direction and the topology of the equivalent resonant circuit changes

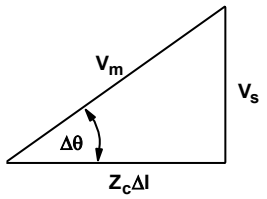

Fig.7 Relationship between V_m, V_s, $Z_c \Delta I$, and $\Delta\theta$

from Fig. 4(b) to Fig. 4(c). As the topology in Fig. 4(c) differs from the topology in Fig. 4(b) only in the sign of the voltage source V_s, the expressions for the inductor current and capacitor voltage during the second resonant interval $T_{r2} = [T_2 - T_3]$ in Fig. 6 can be easily obtained by rewriting equations (8) and (9) as

$$i_L(t) = \frac{I_o}{2} + I_{m2} \cdot \cos[\omega_o (t - T_2) - \Delta\theta_2] \ , \qquad (18)$$

and

$$v_{C1}(t) = -V_s + V_{m2} \cdot \sin[\omega_o (t - T_2) - \Delta\theta_2] \ , \qquad (19)$$

where

$$V_{m2} = \sqrt{V_s^2 + (Z_c \Delta I_2)^2} \ , \qquad (20)$$

$$I_{m2} = \frac{V_{m2}}{Z_c} \ , \qquad (21)$$

and

$$\Delta\theta_2 = \omega_o \Delta T_2 = \text{atan} \frac{-V_s - V_{C0}}{Z_c \Delta I_2} \ ; \quad \pi \le \Delta\theta_2 \le 2\pi \ . \qquad (22)$$

At the end of the second resonant interval T_{r2}, the resonant inductor current is determined as

$$i_L(T_3) = \frac{I_o}{2} + I_{m2} \cdot \cos[\omega_o T_{r2} - \Delta\theta_2] = \frac{I_o}{2} + \Delta I_3 \ , \qquad (23)$$

whereas, the value of resonant-capacitor voltage is zero, as shown in Fig. 6. Therefore, at $t = T_3$, switch Q_1 can be turned on with zero-voltage switching (ZVS). It should be noted in both Fig. 5 and Fig. 6 that at $t = T_1$, when switch Q_1 turns off, the switch current is equal to only ΔI, which means that the switch turns off with almost zero current switching (ZCS).

During the negative half cycle of a switching period T_{sw}, the behavior of the circuit is the same as during the positive half cycle. The only difference is that switches Q_1 and Q_2 change roles.

The total linear increase/decrease of the inductor current during a half switching cycle in both Fig. 5 and Fig. 6 is obtained as

$$\Delta I_L = \frac{V_s}{L} \left(\frac{T_{sw}}{2} - T_r \right) \ . \qquad (24)$$

It should be noted in Fig. 5 that if $T_3 = T_2$ and $T_6 = T_5$, i.e., if the termination of the resonant interval coincides with the end of a half switching cycle, $\Delta I_L = I_{o\max}$, because

$$i_L(T_3) - i_L(T_4) = \left(\frac{I_{o\max}}{2} - \Delta I \right) + \left(\frac{I_{o\max}}{2} + \Delta I \right) = I_{o\max} \ . \qquad (25)$$

If, in Fig. 5, $T_3 > T_2$ and $T_6 > T_5$, the linear change of the inductor current during intervals $[T_3 - T_2]$ and $[T_6 - T_5]$ is

$$i_L(T_3) - i_L(T_2) = \left| i_L(T_6) - i_L(T_5) \right| = \frac{\Delta I_L - I_{o\max}}{2} \ , \qquad (26)$$

which follows from the half-wave symmetry of the inductor current waveform. Consequently,

$$i_L(T_3) = -i_L(T_6) = -i_L(T_0) = \\ = \frac{\Delta I_L - I_{o\max}}{2} + \left(\frac{I_{o\max}}{2} - \Delta I \right) = \frac{\Delta I_L}{2} - \Delta I \ , \qquad (27)$$

as shown in Fig. 5.

Finally, using the half-wave symmetry of the inductor current waveform, ΔI_L in Fig. 6 can be expressed as

$$\Delta I_L = I_{o\max} + \Delta I - \left| \Delta I_3 \right| \ . \qquad (28)$$

B. Output Voltage Regulation

The output voltage regulation can be explained observing the waveforms in Fig. 5. The output voltage is equal to the average voltage across capacitor C_1 (or C_2) during a switching period T_{sw},

$$V_o = \frac{V_s}{\pi} \cdot \frac{T_o}{T_{sw}} \left(\frac{\pi}{2} + \text{atan} \frac{V_s}{Z_c \Delta I} + \frac{Z_c \Delta I}{V_s} \right) \ . \qquad (29)$$

It follows from (29) that the regulation of output voltage V_o versus load current variations, at a constant input voltage V_s, can be achieved by keeping ΔI constant. Because $\Delta I = I_{L0} - I_o / 2$, as defined in (5), with increasing I_o, I_{L0} should also increase in order to keep ΔI constant. As illustrated in Fig. 5, the waveform of the ac component of the inductor current, $i_L - I_o/2$, which charges and discharges the resonant capacitor during the resonant interval T_r is the same at $I_{o\max}$ and $I_o = 0$. Therefore, the corresponding waveforms of the resonant-capacitor voltage at $I_{o\max}$ and $I_o = 0$ are identical and the output voltage is the same at $I_{o\max}$ and $I_o = 0$. However, the waveforms of the inductor current and capacitor voltage at $I_{o\max}$ are phase shifted compared to the corresponding waveforms at $I_o = 0$. In fact, with increasing load current the resonant interval T_r is more phase shifted with respect to the beginning of a half switching cycle.

Comparing the waveforms in Figs. 5 and 6, it can be seen that the phase shift of the resonant interval T_r in Fig. 6 is larger than the maximum possible phase shift in Fig. 5. In fact, by extending the operation of the circuit from Mode I in Fig. 5 to Mode II in Fig. 6, an additional phase shift can be achieved, i.e., the operation range of the circuit can be extended to larger load currents without changing the values of the resonant inductance and resonant capacitance. Because of the two resonant intervals, the output voltage in Mode II cannot be expressed in a simple closed form such as (29) in Mode I. Nevertheless, the output voltage regulation in Mode II is similar to the output voltage regulation in Mode I.

To facilitate the understanding of the output voltage regulation versus input voltage and load current variations in the whole output-voltage range from $V_{o\min}$ to $V_{o\max}$, Eq. (29) which defines $V_o = f(V_s, \Delta I)$ is graphed in Fig. 8 as a family of characteristics $V_o = f(V_s)$ with ΔI used as a parameter. The four extreme operating points, $Q_1 - Q_4$, are also defined in Fig. 8. From Fig. 8, the following relationships can be observed:

- At ΔI = constant, V_o increases approximately linearly with increasing V_s;
- The slope of characteristics $V_o = f(V_s)$ slightly decreases with increasing V_o;
- At V_s = constant, ΔI increases with increasing V_o;
- At V_o = constant, ΔI decreases with increasing V_s;
- $\Delta I = \Delta I_{\min}$ at $V_{s\max}$ and $V_{o\min}$ (operating point Q_1);
- $\Delta I = \Delta I_{\max}$ at $V_{s\min}$ and $V_{o\max}$ (operating point Q_3).

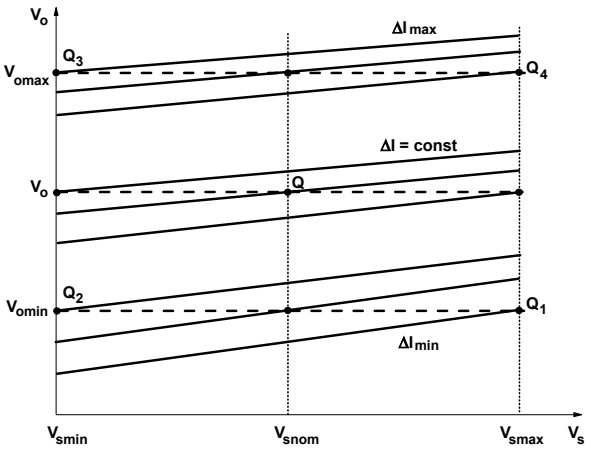

Fig. 8 $V_o = f(V_s, \Delta I)$ characteristics

III. DESIGN

After selecting the switching frequency f_{sw}, the key design parameters are the turns ratio of the transformer N, the resonant inductance L, and the resonant capacitance C. Design constraints are defined in the four extreme operating points $Q_1 - Q_4$ in Fig. 8. To use the characteristics $V_o = f(V_s, \Delta I)$ in Fig. 8, first the turns ratio of the transformer should be selected.

After selecting the turns ratio of the transformer, resonant inductance L and resonant capacitance C can be obtained by considering the four extreme operating points in Fig. 8.

First, operating point $Q_1 = Q(V_{s\max}, V_{o\min})$ is considered. In operating point Q_1, the regulation parameter $\Delta I = \Delta I_{\min}$. It follows from Fig. 5 and Eq. (12) that ΔI must have a positive value, i.e., $\Delta I \geq 0$. In addition, it follows from Fig. 8 that a larger $\Delta I_{\min}$ in operating point Q_1 results in a larger $\Delta I_{\max}$ in operating point Q_3. Obviously, a larger $\Delta I_{\max}$ means larger rms values of the inductor current and switch current. Therefore, to obtain the smallest possible $\Delta I_{\max}$, the minimum value of the regulation parameter ΔI should be selected as

$$\Delta I_{\min} = 0 \quad . \tag{30}$$

It should be noted in Fig. 5 that at $\Delta I = 0$, ΔT increases to $T_o/4$, therefore, $T_r = T_o$, and the inductor-current waveform during the resonant interval T_r becomes a full sine wave, while the capacitor-voltage waveform becomes a full cosine wave.

The output voltage in operating point Q_1 at $\Delta I = \Delta I_{\min} = 0$ is obtained from (29) as

$$V_{o\min} = V_{s\max} \cdot \frac{T_o}{T_{sw}} \quad . \tag{31}$$

Finally, from (31), the resonant period can be determined as

$$T_o = T_{sw} \cdot \frac{V_{o\min}}{V_{s\max}} \quad . \tag{32}$$

Second, operating point $Q_2 = Q(V_{s\min}, V_{o\min})$ is considered. In operating point Q_2, at $I_o = I_{o\max}$, the following time constraint can be defined

$$T_1 - T_0 + T_r = \frac{T_{sw}}{2} \ , \tag{33}$$

which means that the termination of resonant interval T_r coincides with the end of a half switching cycle. In this case, the total linear increase/decrease of the inductor current during a half switching cycle, ΔI_L, is equal to $I_{o\max}$ as explained in (25). Substituting (13) and (12) in (24), ΔI_L is determined as

$$\Delta I_L = \frac{V_s}{L}\left(\frac{T_{sw}}{2} - \frac{T_o}{2} - \frac{T_o}{\pi} \cdot \operatorname{atan}\frac{V_s}{Z_c \Delta I}\right) \quad . \tag{34}$$

It can be proven analytically that ΔI_L in (34) has minimum in operating point Q_2. However, the same can be concluded with the following simple reasoning. Because in operating point Q_2 the input voltage is $V_s = V_{s\min}$, the inductor current increases with a minimum slope equal to $V_{s\min}/L$; therefore, the inductor current needs the longest time interval to increase by $I_{o\max}$. Further, along the vertical characteristic $V_s = V_{s\min}$ in Fig. 8, resonant interval T_r has maximum value in operating point Q_2, as follows from (12) and (13). In fact, in operating point Q_2, ΔI has a minimum value, therefore, ΔT has a maximum value, resulting in a maximum value of T_r. The longest time interval needed for the inductor current to increase by $I_{o\max}$ and the maximum resonant interval T_r satisfy the constraint defined in (33).

Substituting $\Delta I_L = I_{o\max}$ and $V_s = V_{s\min}$ in (34), it follows that in operating point Q_2

$$\frac{V_{s\min}}{L}\left(\frac{T_{sw}}{2} - \frac{T_o}{2} - \frac{T_o}{\pi} \cdot \operatorname{atan}\frac{V_{s\min}}{Z_c \Delta I_{Q2}}\right) = I_{o\max} \quad . \tag{35}$$

The product $Z_c \Delta I_{Q2}$ in (35) can be determined from (29),

$$V_{o\min} = \frac{V_{s\min}}{\pi} \cdot \frac{T_o}{T_{sw}}\left(\frac{\pi}{2} + \operatorname{atan}\frac{V_{s\min}}{Z_c \Delta I_{Q2}} + \frac{Z_c \Delta I_{Q2}}{V_{s\min}}\right). \tag{36}$$

After substituting $Z_c \Delta I_{Q2}$ from (36) in (35), the resonant inductance is obtained as

$$L = \frac{V_{s\min}}{I_{o\max}} \cdot \left[\frac{T_{sw}}{2} - \frac{T_o}{2} \cdot \left(1 + \frac{2}{\pi} \cdot \operatorname{atan}\frac{V_{s\min}}{Z_c \Delta I_{Q2}}\right)\right] \quad . \tag{37}$$

If the design includes Mode II in Fig. 6, then $I_{o\max}$ in (37) represents the maximum load current in Mode I in Fig 5,

which is, typically, 50-75% of the total maximum load current.

Finally, the resonant capacitance is determined directly from (32) and (37) as

$$C = \frac{1}{L} \cdot \left(\frac{T_o}{2\pi} \right)^2 \quad . \tag{38}$$

Third, operating point $Q_3 = Q(V_{s\min}, V_{o\max})$ is considered. It can be proven analytically that the switches in Fig. 3 have maximum voltage stress in operating point Q_3. The voltage stress on the switches is determined by the peak value of the resonant-capacitor voltage, defined in Figs. 5 and 6 as

$$V_{Cpk} = V_s + V_m \quad . \tag{39}$$

Substituting V_m from (10) in (39), the maximum voltage stress on the switches is determined as

$$V_{Q\max} = V_{s\min} + \sqrt{V_{s\min}^2 + \left(Z_c \Delta I_{\max}\right)^2} \quad . \tag{40}$$

The maximum voltage stress on the switches determined by (40) is used for checking the proper selection of the turns ratio of the transformer. If the maximum voltage stress on the switches is smaller than the breakdown voltage of the switches with enough safety margin, it can be concluded that the turns ratio of the transformer was properly selected.

IV. Implementation of 1.8-MHz 48-V VRM

The 1.8-MHz, 48-V, 130-W VRM is implemented as two 65-W VRM modules connected in parallel. The current-source property of the VRM topology (L_{ext}) allows paralleling of two or more modules without special current-sharing precautions. The two VRM modules are implemented on the same printed circuit board (PCB). Each VRM module occupies half of the PCB area. The simplified circuit diagram of one 1.8-MHz, 48-V, 65-W VRM module is shown in Fig. 9. The input voltage range is 48 V ± 10% = 43.2-52.8 V. The output voltage range is 0.95-1.7 V. The maximum load current per VRM module is 50 A at 0.95-1.3-V output voltage range, while at 1.3-1.7-V output voltage range, the maximum load current is determined by the maximum output power of 65 W.

The primary-side half-bridge inverter is implemented with FDS3672 (100 V, 7.5 A, 22 mΩ) MOSFETs from Fairchild. Each of the secondary-side synchronous rectifiers, Q_1 and Q_2, is implemented with five parallel IRF7811W (30 V, 14 A, 9 mΩ) MOSFETs from IR.

Transformer T_1 is implemented with planar cores PC50ER14.5/6-Z from TDK and with helical windings. The turns ratio of the transformer is $N = 5$. The primary-side magnetizing and leakage inductance of the transformer is around 25 μH and 90 nH, respectively. External resonant inductance L_{ext} is implemented with a toroidal core T37-2 from Micrometals and 9 turns, 2 strands of ϕ0.6 wire. The inductance of L_{ext} is around 330 nH. Therefore, the total primary-side resonant inductance is around 420 nH.

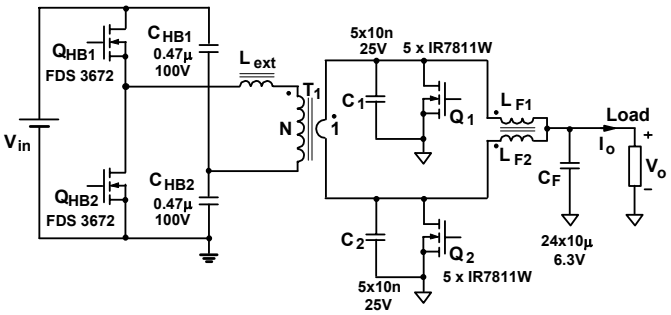

Fig. 9 Simplified circuit diagram of a 1.8-MHz, 48-V, 65-W VRM module

Output-filter inductances L_{F1} and L_{F2} are coupled. They are implemented with two stacked planar EI cores 14/3.5/5 (3F3), with 1-mil air gap, and with single turn copper bars. The inductance of each L_{F1} and L_{F2} is around 80 nH.

Finally, output-filter capacitance C_F is implemented with surface mount ceramic capacitors. The whole output-capacitance bank is arranged in a 3x8 matrix form.

The functional block diagram of the control circuit is shown in Fig. 10. Key waveforms are presented in Fig. 11. The clock signal in Fig 10 has a frequency equal to 3.6 MHz. The two D flip-flops, DFF SR and DFF HB, operate as frequency dividers by 2. Therefore, the frequency of the SR and HB gate drive signals is equal to 1.8 MHz. The phase-shifted control is achieved by phase shifting the SR control

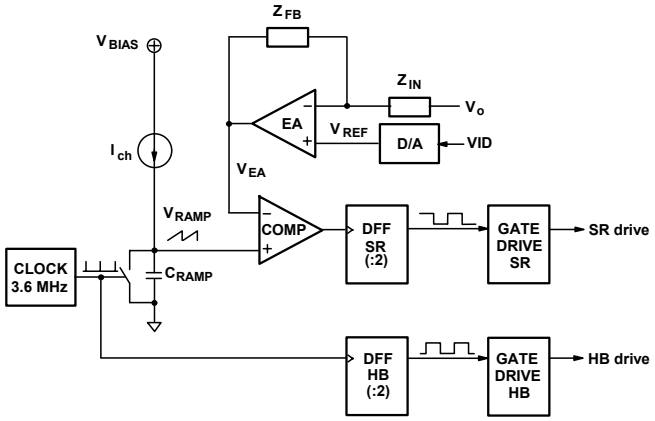

Fig. 10 Functional block diagram of the control circuit

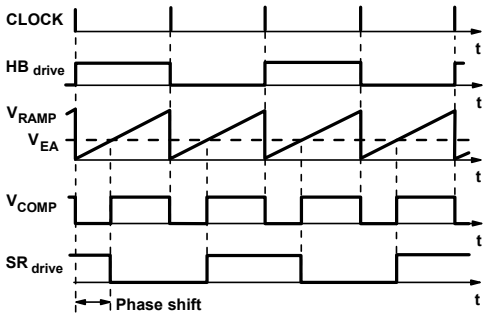

Fig. 11 Key waveforms of the control circuit

pulses with respect to the HB control pulses. With increasing load current, error-amplifier voltage v_{EA} increases and, through the comparator, the phase shift of the SR control pulses increases with respect to the HB control pulses.

The HB gate drive signals are applied to the gates of the HB switches through a gate-drive transformer. The HB switches operate with partial ZVS switching. The SR gate drive signals are applied to the gates of the SRs through a resonant circuit. A resonant gate drive for the SRs at 1.8-MHz switching frequency is absolutely necessary because of the large input capacitance of the SR MOSFETs. The circuit diagram of the resonant gate drive for the SRs is shown in Fig. 12. Transformer T_2 is implemented with planar cores PC50ER9.5/5-Z from TDK with 4-mil gap. The turns ratio of the transformer is $N = 5$. The primary-side magnetizing inductance L_m is around 2 μH. Key waveforms are presented in Fig. 13. The waveforms in Fig. 13 are obtained for the case when $L_1 = 0$. The basic operation of the resonant gate drive circuit in Fig. 12 is similar to the basic operation of the main resonant converter in Fig. 3. This can be concluded by comparing the waveforms of the resonant inductor current i_{Lm} and resonant capacitor voltage v_{Cp} in Fig. 13 with the corresponding waveforms in Fig. 5. It should be noted that the total resonant capacitance in Fig. 12 consists of capacitance C_p and the gate-source capacitance of the SR reflected to the primary side of the transformer. Bias capacitor C_b, resistor R_1, and diode D_1 in Fig. 12 form a peak detector circuit, which automatically provides a bias voltage for the SR.

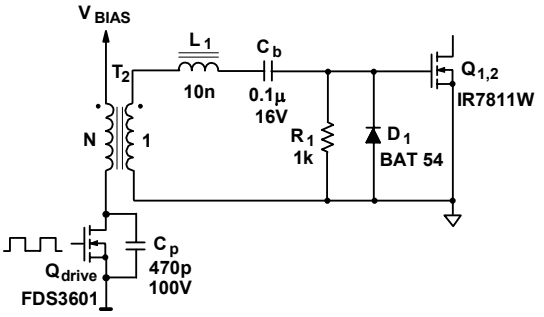

Fig. 12 Resonant gate drive circuit

An improvement of the gate-drive voltage waveform can be achieved by adding inductor L_1 as shown in Fig. 12. By proper selection of inductance L_1, a third harmonic can be injected in the gate-drive voltage waveform, which results in steeper edges and a wider pulse, as illustrated in Fig. 14.

It should be noted that the resonant gate drive circuit in Fig. 12 generates gate-drive pulses of a constant width. However, the optimal width of the gate drive pulses varies with both the input and output voltages, as follows from (12) and (13). Therefore, with the resonant gate drive circuit in Fig. 12 optimal gate drive pulses can be obtained only for a narrow range of input and output voltages. Otherwise, if the generated pulse width is greater than the optimal pulse width, the body diode of the SR will conduct; or, if the generated pulse width is smaller than the optimal pulse width, the SR will turn on with hard switching. In both cases, the efficiency of the VRM will be reduced. In applications, where the reduction of the efficiency is not acceptable, instead of the RCD bias circuit in Fig. 12, a controlled bias circuit has to be employed.

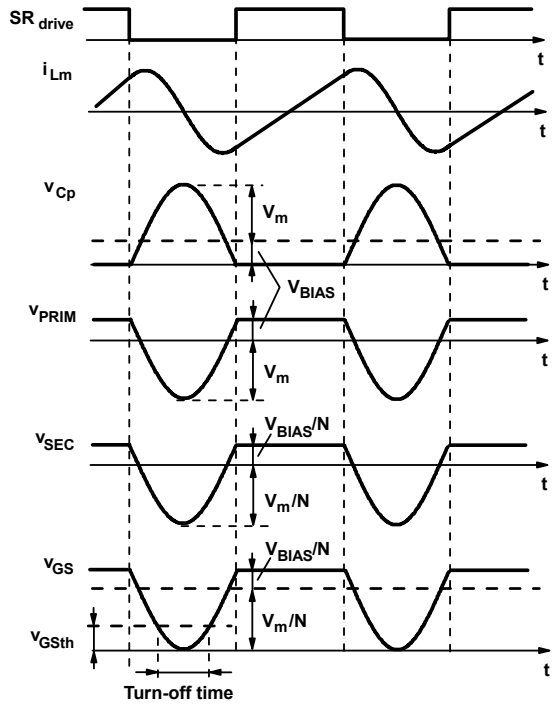

Fig. 13 Key waveforms of the resonant gate drive circuit

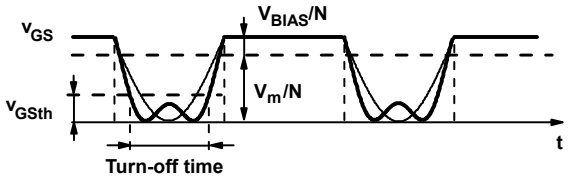

Fig. 14 Improved gate-drive voltage waveform

V. Experimental Results

Efficiency measurements at nominal output voltage $V_o = 1.3$ V are shown in Fig. 15. These measurements were obtained at the output of the connector. It should be noted that the output connector decreases the efficiency, typically, by 5-8 %. The results in Fig. 15 satisfy the spec. requirement, which asks for a minimum 78% efficiency at nominal input voltage of 48 V and nominal output voltage of 1.3 V, at output power levels larger than 65 W.

Transient-response measurements obtained at nominal input voltage of 48 V and nominal output voltage of 1.3 V are shown in Figs. 16 and 17. Figures 16(a) and (b) show the output voltage waveforms at fast load-current transients 75-100 A and 100-75 A, respectively, with a 100 A/μs current

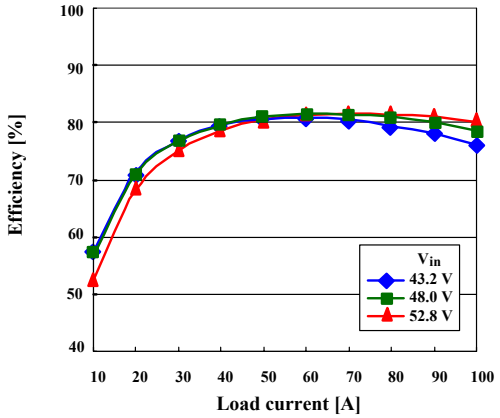

Fig. 15 Efficiency measurements at nominal output voltage V_o = 1.3 V

slope, while Figs. 17(a) and (b) show the output voltage waveforms at slow load-current transients 0-75 A and 75-0 A, respectively, with a 10 A/µs current slope. The maximum deviation of the output voltage is 86 mV in Fig. 16(b). These results satisfy the spec. requirement, which limits the deviation to ±7% of the output voltage (7% of 1.3 V is equal to 91 mV).

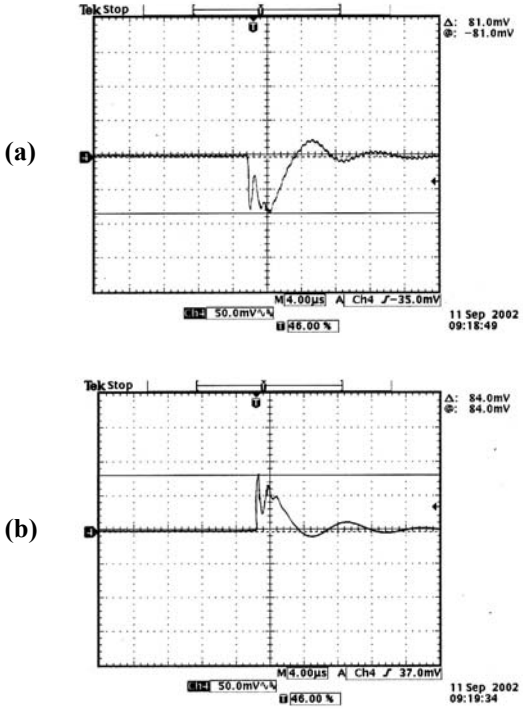

Fig. 16 Output voltage waveform at fast load-current transient (a) 75-100 A and (b) 100-75 A with 100 A/µs current slope (V_{in} = 48 V, V_o = 1.3 V)

VI. Summary

The main features of AE's new high-frequency resonant converter technology with phase-shifted regulation can be summarized as follows.

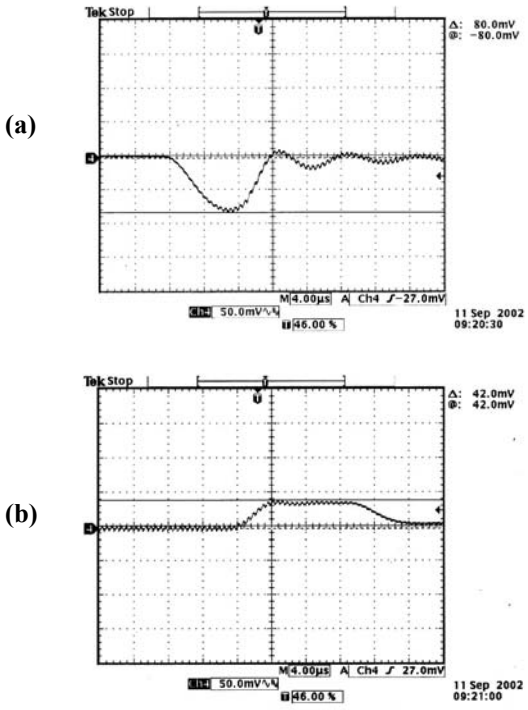

Fig. 17 Output voltage waveform at slow load-current transient (a) 0-75 A and (b) 75-0 A with 10 A/µs current slope (V_{in} = 48 V, V_o = 1.3 V)

- Simple isolated topology: half-bridge inverter + current-doubler rectifier with synchronous rectifiers (SRs);
- Topology suitable to utilize parasitics of components and layout;
- Only surface mount ceramic capacitors at the output;
- Simple control with overlapping conduction of SRs;
- Resonant gate drive of SRs;
- ZVS and partial ZCS of SRs
- Fast transient response;
- Efficiency measured at the output of the connector around 80%;
- Inherent current limit protection (due to series inductance);
- Cost-effective.

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