IDT Integrated Device Technology

Clock Tree Considerations for Base-Station RF Cards

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INTRODUCTION

There are a number of issues that need to be addressed by a clock tree for a fourth-generation (4G) Long-Term Evolution (LTE) or WiMax wireless base station radio card. In addition to the constraints imposed by the Orthogonal Frequency-Division Multiplexing (OFDM) protocols themselves, there are critical aliasing and filtering concerns for ADCs, DACs and RF mixers. These challenges around the modulation elements provide the focus of this article.

SIMPLIFICATION OF NETWORK DEPLOYMENTS AND UPGRADES

In order to support the simplification and economy of network deployments and upgrades, OEMs will look for radio card components that support software reconfiguration and can be re-used on multiple similar designs.

Because of the occasional need to support radio cards within a Remote Radio Head, most radio cards will be designed with a single input clock that may be recovered from the link to the base-station. These single input clocks may be poor in quality and significant jitter cleanup may be required in order to adequately generate other clocks on the radio card.

Thus, the core of a radio card clock tree must be a jitter attenuator with programmable output frequencies. The remainder of this article will discuss the performance attributes and why they are required, along with other clock tree requirements.

RADIO CARD ARCHITECTURAL CONSIDERATIONS

Most radio card designs in base-stations today perform many of the manipulations required to build-up or tear-down the signal for a protocol like LTE or Multi-carrier GSM in the digital domain. It is much simpler to handle error-correction, channel-mapping and splitting the I & Q streams digitally.

The complex data stream of this composite signal also requires very careful filtering / signal processing in both the transmit and receive directions. Doing this in the digital domain avoids the expense of things like precise component-value matching.

Despite the extensive digital manipulations, at some point, the signal must be modulated onto a carrier that can range from 824Mhz – 2.62GHz and transmitted as an analog signal. Most base-station architectures that address multi-channel protocols including LTE, WiMax and multi-carrier GSM use a single stage analog conversion approach as shown in Fig 1.

On the transmit side, the individual sub-carriers are combined into a single stream digitally without being modulated first. This baseband signal is then converted to phase-offset analog I & Q streams by DACs and then up-converted to the transmission frequency via quadrature analog mixers. Variable and fixed gain amplifiers and a duplex filter are used along the path to boost the desired signal to the required strength in its transmission band while adding only a small amount of noise & distortion and simultaneously minimizing energy outside the transmission band to prevent interference with other RF channels.

On the receive side, the RF signal is usually amplified, filtered, and then converted via a mixer to a much lower intermediate frequency (IF) in the 75MHz – 250MHz range where it is further amplified by a variable amount, filtered and finally sampled by a pipeline ADC in accordance with the Nyquist criterion. Down conversion and demodulation of the sub-carriers are then handled in the digital domain. The goal with the receiver is to accomplish this signal conditioning prior to the ADC with a minimum of added noise and intermodulation distortion while avoiding exceeding ADC full scale.

Radio card architects prefer that the clock tree be as integrated as possible. Not only for the reasons described, but because each clock tree component comes with its own jitter contribution that can push the clock signal out of spec. With this integration comes the need to generate not just the RF & IF clocks for modulation, but the sampling clocks for the ADCs & DACs and the clocks for the other digital components such as CPUs, ASICs and FPGAs.

The clocks for these digital components usually have quite lax specifications in comparison to the clocks involved in the RF signal path; period jitter is most often the primary concern. When generating these clocks on the same chip as the more sensitive clocks, there are two issues. First of all, the digital clocks are rarely integer multiples of the incoming clock signal to the radio card and so must be generated with fractional feedback or fractional output divider

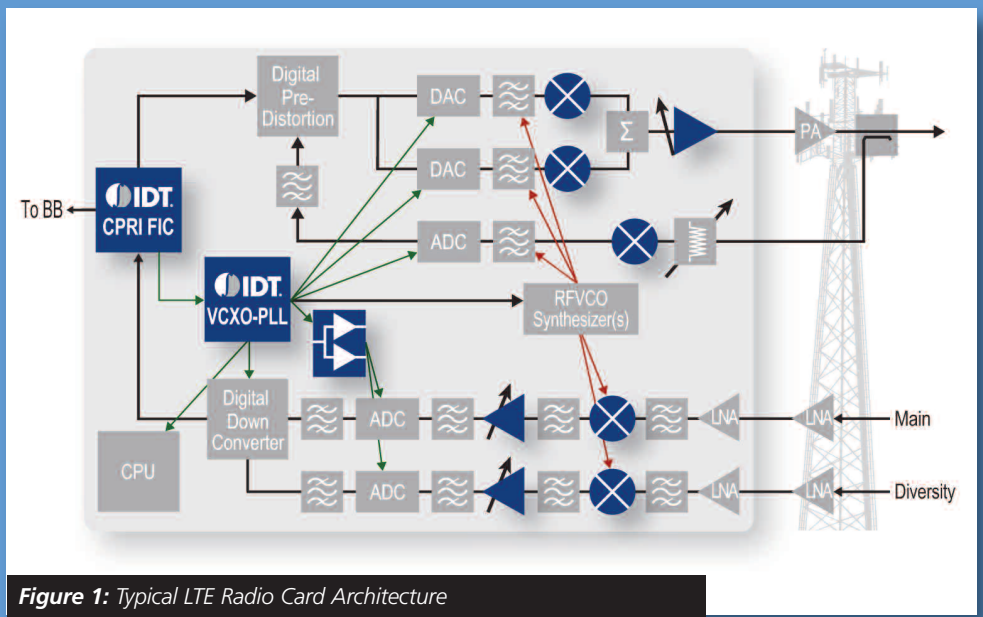

Figure 1: *Typical LTE Radio Card Architecture*

techniques. Both these techniques however, introduce significant spur content within the clock chip and onto the clock outputs. Secondly, digital-chip clocks (or any spurs produced while generating them) that fall near the RF, IF or sampling frequencies can't be filtered out easily and so must be avoided. Even frequency components outside those regions of interest may degrade the SNR either as wideband noise or, if they are not filtered, by aliasing into the critical frequency ranges.

FREQUENCY EFFECTS OF MIXERS, ADCS AND DACS

Mixers are the analog components used to convert a higher frequency signal to a lower frequency signal or vice-versa. In most base-station radio card designs they currently convert the signal from RF->IF or from Baseband->RF. The main issue of concern with respect to a clock tree design is the issue of frequency aliasing. When multiple frequencies pass through a non-linear device, those frequencies will interact with each other. These interactions are called inter-modulation products.

The function of a mixer is to take two input frequencies and produce an output frequency that is either the sum (up-conversion) or difference (down-conversion) of the two frequencies.

Present-day radio cards are designed to recover signals that are multi-carrier in nature. So, rather than a single tone line of desired signal, the ideal signal consists of a whole series of tone lines evenly spaced throughout the frequency band of interest. These lines represent the individual channels being recovered. Unfortunately as this multi-carrier signal proceeds through a non-linear element like a mixer, each of those channels will inter-modulate each other. The regular spacing of the channels will cause the odd order products to fall almost exactly on top of the channels being recovered. Filters placed before a mixer will be used to attenuate noise that will contribute to even-order products. Filters after the mixer will remove inter-modulation products that fall outside the frequency band of interest, however little can be done about the in-band odd-order products because they fall too close to the wanted signals.

While a band pass filter after the mixer can remove the undesired clean tone lines fairly well, any jitter on the sampling clock will turn those clean tone lines into a skirt as shown in Fig 2. The tails of the skirts from every undesired product will have some contribution within the pass band of the filter; this is referred to as wideband noise. Any clocks generated for the mixers (or ADCs or DACs) must have a very low noise floor in order to minimize their wideband noise contribution.

Unwanted signals called 'interferers' or 'blockers' that get into the mixer's input will have an effect on the specifications of clock signals. They can include other signals received by the antenna or signals internal to the system that get coupled into the receive signal path. While blockers that are widely separated in frequency from the desired signal can be significantly attenuated by the pre-filter, ones close to the desired signal's frequency will pass through. Furthermore, in a protocol like LTE where the wanted signal has a low average power, even a blocker attenuated by the filter may still contain enough energy to compete with the desired signal.

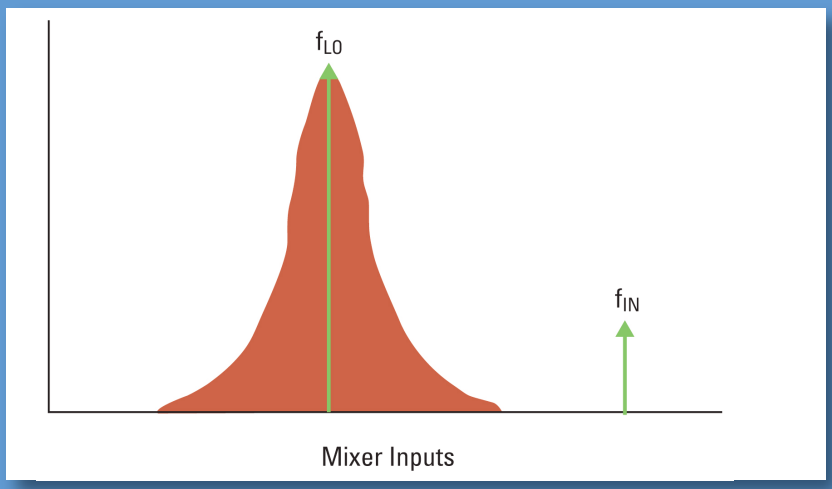

Figure 2: *Effect of reciprocal mixing*

This effect is why the phase noise skirt of the clocks into the mixers must be kept as 'narrow' as possible. The spread of the reciprocally mixed phase noise on the blockers must be kept to a minimum. One of the main challenges in the radio card design is the selection of frequencies on the card with an eye to maximizing the separation of blockers and their inter-modulation products from the frequencies of the wanted signals.

ADDITIONAL EFFECTS OF JITTER ON ADCS

Because ADCs are sampled data systems and are not perfectly linear in their translations, they too will suffer all the same effects of inter-modulation products between desired input signals, unwanted (blocker) signals and the sampling clock.

However, there is another effect driving the specifications of the sampling clock for the ADC. This is the aperture jitter effect illustrated in Fig 3.

The basic concept is that any uncertainty in the time that a sample is taken can be translated by trigonometry into an uncertainty in the amplitude for that sample. Uncertainty in amplitude results in degradation in the SNR of the ADC. Once the frequency of the input signal is known, a RMS jitter target can be determined for the desired SNR of the ADC. Once that target is arrived at then the intrinsic jitter of the clock tree within the ADC can be factored-out to determine the target RMS jitter spec for the sampling clock.

EFFECTS OF CLOCK JITTER ON DACS

Digital-Analog Converters (DACs) are used in the transmit path to turn a digital representation of the baseband signal into an analog one for

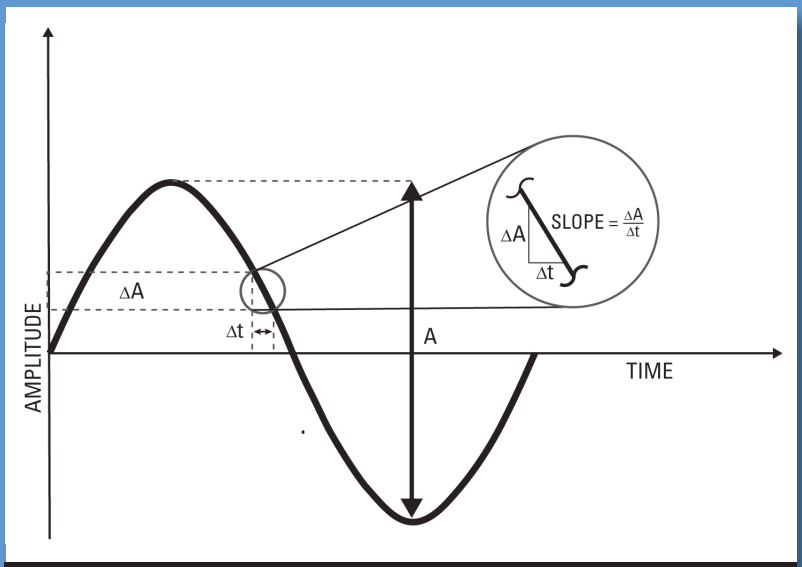

Figure 3: *Aperture jitter in an ADC*

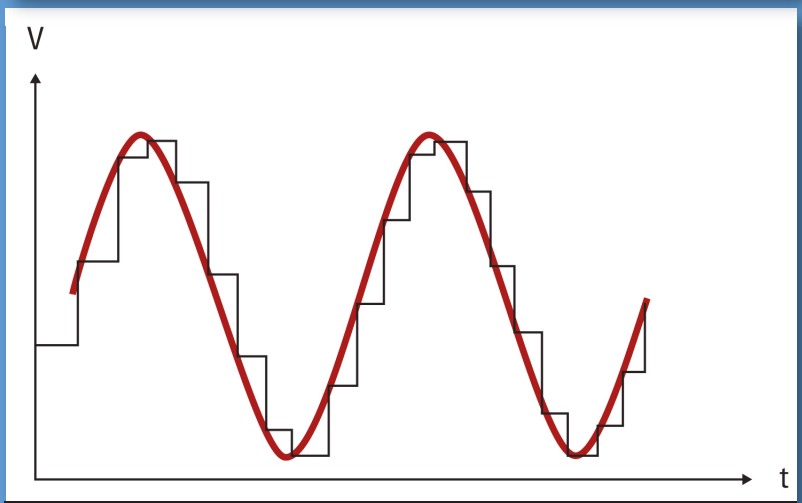

Figure 4: *DAC output compared to ideal output (prior to reconstruction filter)*

subsequent conversion to the RF frequency and amplification to the desired transmit power. The radio card designer will take care in fixing the card's frequency plan to ensure that the sampling frequency of the DAC does not overlap critical frequency bands on the receive side of the card. This is important because DACs suffer from the generation of image frequencies from two potential mechanisms.

The first mechanism is identical to what happens in ADCs and mixers, the convolution of the sampling clock (fLO) and the input signal (fIN) to produce frequencies at N · fLO + M · fIN. This convolution results from non-linearities in the converter. The effects on the requirements for the sampling clock jitter are similar to the ADC.

The second mechanism is an unavoidable result of the way most DACs operate. As shown in Fig 4, at every edge of the sampling clock the DAC's output will switch very quickly to a new voltage level as represented by the digital sample value. This value will be held until the next sampling clock edge. The output only matches the desired waveform once per sample clock.

This results in error energy being introduced. Additionally, most DACs will suffer from some level of clock feed-through, resulting in further spikes at N · fLO. For this reason, the sampling clock frequency will often be considerably higher than required by Nyquist so that the feed-through spikes are well beyond the frequency of interest and so can be easily filtered.

The DAC output waveform will be passed through an analog reconstruction filter to remove as many of these unwanted frequencies as possible. Design of the filter will be easier and implementation will be less costly if the clock jitter and phase noise skirt can are well controlled.

In addition to requirements for specific phase noise levels at specific offsets on the sampling clock, there will also be a specification for RMS jitter integrated over a range of frequencies. This is due to clock jitter causing distortion on the output waveform from the ideal. This will degrade the Total Harmonic Distortion (THD) or Signal-to-Noise-plus-Distortion (SINAD) of the DAC and must be kept within specification to prevent degradation of the radio card's Error Vector Magnitude (EVM). On the transmit side, lower clock jitter can either directly contribute to better EVM or be used to relax the design constraints for Crest Factor / Peak-Average Power Ratio reduction circuitry.

REQUIREMENTS FOR PHASE ALIGNMENT WITHIN A RADIO CARD

In addition to basic voice and data transmission services, many mobile users are demanding additional services. One example is precise location of the user via triangulation from a set of cell towers. Precise determination of location by radio triangulation is best achieved when all the antennas are transmitting and receiving signals in close phase alignment with each other. Some such services such are requiring separate base-stations to operate with less than 50 nsec of phase discrepancy between them. A radio card will be given a budget of how much phase discrepancy it may introduce relative to other radio cards in the same system. This is another reason why each radio card generates all its frequencies internally from a single clock input signal. It ensures that there is at least a common starting point for phase alignment for all the clocks on the card.

SUMMARY

RF cards need to generate a variety of clocks from a single, often noisy, input clock. Several of these output clocks will not have an integer relationship to the input clock. All clocks must pay attention to their total noise contribution in order to prevent noise coupling into critical circuitry. Clocks specifically for mixing functions including ADCs and DACs will have tight specs on their RMS jitter as well as on their 'noise skirt' to avoid generating blocker signals in the RF signal paths. The frequencies for these clocks will be carefully planned for the specific implementation details of the card and so are usually unique to each design. Also, a variety of phase delay adjustments must be possible for many of those same clocks. The result of this is a need for a very high-performance clock tree whose specs are essentially custom for each card, ideally implemented in a single component. Devices such as IDT's Netcom timing devices are uniquely positioned to provide those very high-performance devices tailored to the individual RF card design requirements.

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