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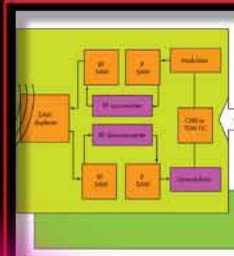
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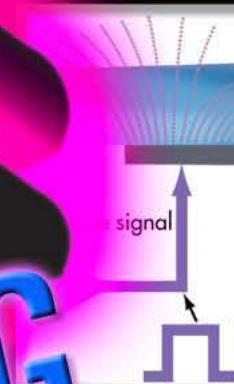
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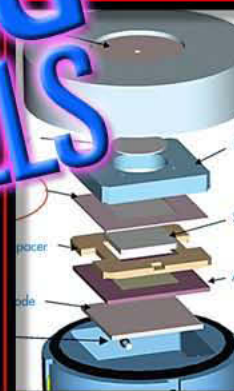
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MOVE TO SERIAL RAPIDIO 2.0
Standard meets mobile-user bandwidth demands



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MAKE THE MOVE TO SERIAL RAPIDIO 2.0

The next-generation standard meets the compute and bandwidth demands of mobile users.

Within wireless infrastructure equipment, such as cellular basestations, large amounts of data is processed, usually with clusters of DSPs. Moving the large volume of data to, from, and in between these DSPs is no small challenge. The required bandwidth continues to multiply as mobile traffic increases and as subscribers demand more bandwidth-intensive services on their handsets, like video on demand.

In 1997, work began on the creation of a standardised interface that could be implemented on processors and peripherals. In 1999, an open standard, RapidIO, was published. It addressed the needs of reliability, increased bandwidth, low latency, and other key needs in intrasystem interconnect. The specification gained rapid and widespread acceptance. The RapidIO Trade Association (RTA) was formed in 2000 and continues

to provide updated standards that address the needs of the industry.

These days, Serial RapidIO has turned into the embedded interconnect of choice. Wireless telecommunications infrastructures, particularly baseband, have been at the forefront of system developments, with European telecommunications OEMs being key players in the development and deployment of next-generation equipment.

MIGRATION TO SERIAL

The migration to 2G and 3G cellular basestation architectures, along with the expected services, required even larger banks of DSPs in basestation architectures. The original RapidIO interface, however, was a parallel architecture and did not easily support the required numbers of DSPs. Because of the number of interconnects required, the limitations of board space for traces and chip pin-count restrictions, migration to a serial interface was necessary.

The Serial RapidIO standard version 1.2 was released in 2002 and subsequently upgraded to version 1.3 in 2005. This has become the embedded interconnect of choice, adopted by major DSP, field-

programmable gate array (FPGA), switch-fabric, and microprocessor providers for DSP clusters in cellular basestations, backplanes, imaging, and industrial control applications.

Due to the interoperability ensured by the standard, a robust ecosystem of devices, software and development tools are based on Serial RapidIO. And because of the multiplicity of Serial RapidIO endpoint devices available, the need for bridging to other interconnects is minimised. Virtually all new basestation designs incorporate Serial RapidIO architectures.

The typical basestation architecture partitions the baseband processing onto one or multiple baseband cards. These cards utilise up to four DSPs and possibly other elements, such as control processors and FPGAs on a single board. A Serial RapidIO central packet switch (CPS) device acts as the switch fabric and aggregation point on the card.

Integrated Device Technology (IDT) even offers a pre-processing switch (PPS) family of devices that, in addition to standard switching functions, can offload some of the simple data pre-processing activities of the DSP or FPGA to allow those



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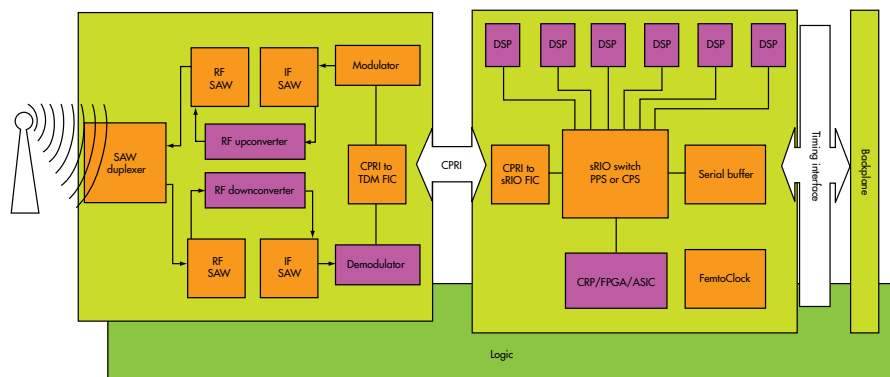
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IDT's standalone fabric interconnect (FIC) device bridges from the Serial RapidIO interface on the baseband card to a CPRI interface.

devices to function more efficiently. If multiple baseband cards are used in a system, they're typically interconnected across a backplane using Serial RapidIO to a control/switch card that would also employ CPS devices.

A standard implementation of a basestation architecture uses the Common Public Radio Interface (CPRI) serial interface for the link between the baseband cards and the radio cards. In addition, IDT offers a standalone fabric interconnect (FIC) device that bridges from the Serial RapidIO interface on the baseband card to a CPRI interface. Another FIC developed by IDT bridges from the CPRI interface to

the TDM interface on the RF card side (see the figure).

Many attributes of the Serial RapidIO 1.3 standard make it optimal for chip-to-chip communication in wireless infrastructure applications. It's a reliable, low-latency transport that supports 1x and 4x lane configurations per port at 1.25Gbps, 2.5Gbps, and 3.125Gbps lane rates, allowing up to 10Gbps on a single 4x port.

Combinations of 1x and 4x lane ports at different lane rates vary widely, depending on the system targets for bandwidth and user capacity for any given basestation architecture. The Serial RapidIO 1.3 standard requires lower over-

head than similar serial data communication standards, such as Ethernet and PCI Express. It also allows processor-to-processor communication (peer to peer) without a root complex.

NEXT-GEN SERIAL RAPIDIO 2.0

During the past few years, Internet traffic has shown tremendous, rapid growth in mobile access markets. The recent increased demand for 3G smart phones and wireless-enabled PDA-type devices will continue to push more mobile data traffic into the enterprise market.

On the general consumer side, the biggest driver for increased data traffic for the foreseeable future will be uploads and downloads of photos and video for watching and sharing. Resulting user demand for faster access and shorter download times—while looking for a richer multimedia experience—will encourage service providers to add higher-capacity 3.5G and 4G basestations to their existing wireless infrastructure mix.

In 3.5G and 4G basestation architectures, increasing data-rate capability and the push for a higher capacity of users per basestation lead to greater backplane speeds

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between radio and baseband cards. This overall bandwidth increase, in turn, requires more multicore DSPs interconnected in a standard cluster configuration on the baseband card. The multicore DSPs now offer triple- and quad-core architectures, operating as high as 1GHz. The natural migration to smaller geometry fabrication processes will allow even higher operating frequencies and possibly the incorporation of more processing cores on-chip.

Despite all of the benefits that Serial RapidIO 1.3 brings to wireless applications, continued demands for greater bandwidth motivated the RTA to publish the Serial RapidIO 2.0 standard in 2007. All leading wireless infrastructure equipment providers are adopting this technology in their next-generation platform designs and even, in some cases, adopting it as a cost- and power-saving measure in legacy platform updates.

IDT is collaborating with many of the key processor vendors in the industry, and support for Serial RapidIO 2.0 on processors and switches is just around the corner. According to IDT, it's one of the first companies in the industry to begin development on a family of Serial

RapidIO 2.0 switch devices. These devices will enable card designers to take full advantage of the bandwidth capabilities as the new processors become available.

Two key benefits that Serial RapidIO 2.0 provides over its predecessor are bandwidth and port flexibility, while still maintaining backward-compatibility with the earlier standard. Serial RapidIO 2.0 doubles the lane rate up to 6.25Gbps, which allows for higher peak data rates.

Adding 2x lane per-port configurations enables the same port rates as Serial RapidIO 1.3, with half the lane count for easy trace routing, and increased trace utilisation. It also adds support for virtual channels (VCs) and virtual output queuing (VOQs), improving overall traffic management and allowing more efficient use of the fabric.

Furthermore, improvements to quality of service (QoS) will appeal to carrier-grade communications applications. Within the physical layer, the new standard additions receive equalisation capabilities that will enable it to support extended long-reach (100cm) traces at the full data rate. This can even be done with conventional FR4-based printed-circuit-board materials.

CONCLUSION

The continuous advances in the wireless infrastructure to meet the growing demands of mobile users create the need for significant increases in system compute capability and bandwidth. The industry responded with its most successful interface standard to meet the needs for more bandwidth, more flexibility, and better quality of service.

The Serial RapidIO 2.0 standard addresses all of these needs and maintains backward-compatibility with the previous versions of the specification—helping to keep the installed infrastructure base from becoming obsolete. The device provider community is developing devices to support the new interface, including DSPs, CPUs, FPGAs, and switch fabrics. To that end, IDT is developing of a family of Serial RapidIO 2.0 switch devices so that next-gen systems can take advantage of the benefits afforded by Serial RapidIO 2.0. ■

PIETRO POLIDORI is vice president of Europe, Middle East, & Africa for IDT.

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