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April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

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R32C/100 Series

Watchdog Timer

1. Abstract

The watchdog timer detects a program runaway. This document describes the settings and shows an example for using the watchdog timer.

2. Introduction

The application described in this document applies to the following MCU:

- MCU: R32C/118 Group

This program can be used with other R32C/100 Series MCUs which have the same special function registers (SFRs) as the R32C/118 Group. Check the manual for any additions or modifications to functions. Careful evaluation is recommended before using this application note.

3. Application Example

When the count value of the watchdog timer underflows, a watchdog timer interrupt can be generated, or the MCU can be reset.

This section describes how to generate a watchdog timer interrupt or watchdog timer reset.

3.1 Watchdog Timer Period Example

The peripheral bus clock becomes the count source for the watchdog timer. The watchdog timer period is calculated with the following formula:

$$\text{Watchdog timer period} = \frac{\text{Prescaler divisor (16 or 128)} \times 32768}{\text{Peripheral bus clock frequency}}$$

The following table shows an example of the watchdog timer period when bits PCD1 to PCD0 (peripheral bus clock divide ratio select bit) in the CCR register are set to 01b (divide by 2), and bits BCD1 to BCD0 (base clock divide select bit) are set to 11b (divide by 2).

Table 3.1 Watchdog Timer Periods (when XIN = 16 MHz, XCIN = 32.768 kHz, PLL Clock = 100 MHz, On-chip Oscillator = approx. 125 kHz)

Setting Value					Watchdog Timer Count Source	Watchdog Timer Period
SEO	CM31 to CM30	BCS	WDC7	PCD1 to PCD0		
0	0 or 1	0	0	01b	Peripheral bus clock (PLL clock divided by 4) divided by 16	Approx. 20.9 ms
0	0 or 1	0	1	01b	Peripheral bus clock (PLL clock divided by 4) divided by 128	Approx. 167.7 ms
0 or 1	00b	1	0	01b	Peripheral bus clock (fC divided by 2) divided by 16	Approx. 32 s
0 or 1	00b	1	1	01b	Peripheral bus clock (fC divided by 2) divided by 128	Approx. 256 s
0 or 1	01b	1	0	01b	Peripheral bus clock (f256 divided by 2) divided by 16	Approx. 16.8 s
0 or 1	01b	1	1	01b	Peripheral bus clock (f256 divided by 2) divided by 128	Approx. 134.2 s
0 or 1	10b	1	0	01b	Peripheral bus clock (fOCO4 divided by 2) divided by 16	Approx. 33.5 s
0 or 1	10b	1	1	01b	Peripheral bus clock (fOCO4 divided by 2) divided by 128	Approx. 268 s

SEO: Bit in the PLC1 register.

CM31 to CM30: Bits in the CM3 register.

BCS: Bit in the CCR register.

WDC7: Bit in the WDC register.

PCD1 to PCD0: Bits in the CCR register.

3.2 Explanation

- (1) By writing to the WDTS register, the watchdog timer is initialized to 7FFFh, and decrement starts.
- (2) When writing to the WDTS register during a count, the watchdog timer is initialized to 7FFFh, and decrement continues.
- (3) When the MCU is in wait mode, stop mode, or when $\overline{\text{HOLD}}$ signal is low, the watchdog timer saves the mid-count value and stops. After exiting these modes and the $\overline{\text{HOLD}}$ signal is high, the count restarts from the saved value.
- (4) To use a watchdog timer interrupt: When the watchdog timer underflows, it is initialized to 7FFFh, and the count continues. At the same time, a watchdog timer interrupt is generated.

To use a watchdog timer reset: When the watchdog timer underflows, pins, the CPU, and SFRs are initialized, and the program is executed starting from the address shown in the reset vector.

The figure below shows an example of the watchdog timer operation.

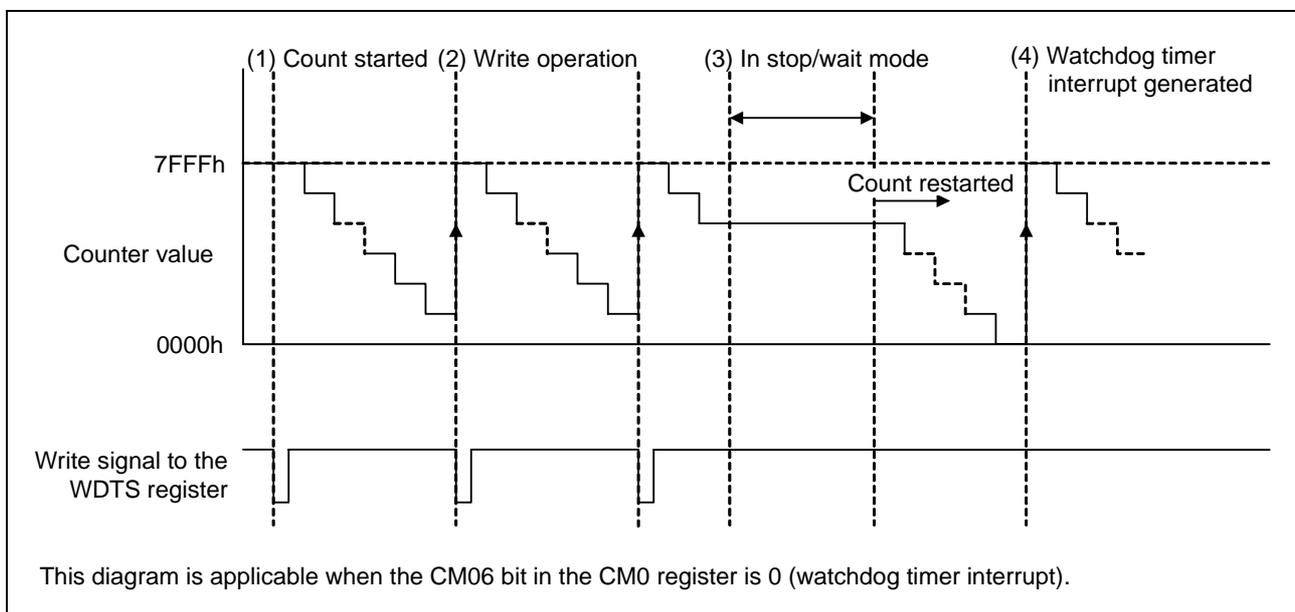
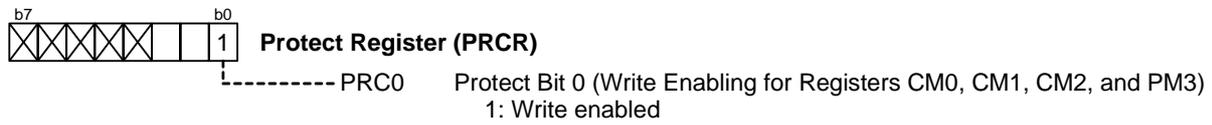


Figure 3.1 Operation of the Watchdog Timer

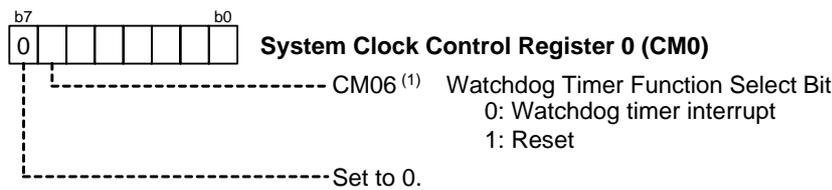
3.3 Setting

This section shows the procedures and values to set the example in section 3.2 “Explanation”. Refer to individual MCU hardware manuals for details on individual registers.

(1) Set the protect register.

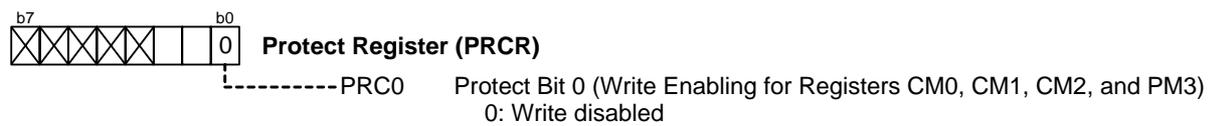


(2) Set the system clock control register 0.

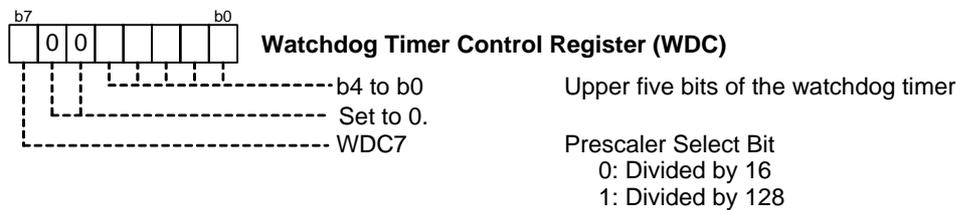


Note:
1. Once this bit is set to 1, it cannot be set to 0 by the user.

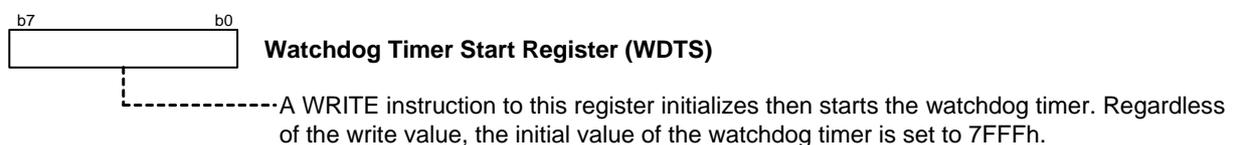
(3) Set the protect register.



(4) Set the watchdog timer control register.



(5) Set the watchdog timer start register.



4. Sample Program

A sample program can be downloaded from the Renesas Technology website.

An explanation of the sample program is given below.

4.1 When using the watchdog timer interrupt

When writing to the WDTS register, the P10 output value increments. When the value output from P10 becomes 40h, writing to the WDTS register is stopped, and the P10 output value stops updating.

When a watchdog timer interrupt is generated, as part of the watchdog timer interrupt processing, while writing to the WDTS register, the P10 output value decrements. When the P10 output value becomes 00h, the P10 output value stops updating.

4.2 When using a watchdog timer underflow-induced reset

While writing to the WDTS register, the P10 output value increments. When the P10 output value becomes 40h, writing to the WDTS register stops, and the P10 output value stops updating. The MCU is reset when the watchdog timer underflows, and processing restarts from the beginning of the program.

5. Reference Documents

Hardware Manual

R32C/118 Group Hardware Manual Rev.1.00

The latest version can be downloaded from the Renesas Technology website.

Technical Update/Technical News

The latest information can be downloaded from the Renesas Technology website.

C Compiler Manual

R32C/100 Series C Compiler Package Ver. 1.02 Compiler User's Manual Rev. 1.00

The latest version can be downloaded from the Renesas Technology website.

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REVISION HISTORY	Watchdog Timer
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Rev.	Date	Description	
		Page	Summary
1.00	Mar. 5, 2010	—	Initial release

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