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M16C/64 Group

Wait Mode Setup

1. Abstract

In wait mode, the CPU clock is turned off, so that the CPU and watchdog timer driven by the CPU clock stop operating. Because the main clock, sub-clock and 125 kHz on-chip oscillator clock do not stop, the peripheral functions operating on these clocks can continue working. Note 1

A hardware reset or an NMI interrupt, voltage-down detection interrupt or peripheral function interrupt Note 2 may be used to return from wait mode. The sample program uses an INTO interrupt for the cause of return from wait mode.

- Note 1: If the CM0 register CM02 bit = 1 (peripheral function clock turned off when in wait mode), the peripheral function clock, f1, that uses the main clock or PLL clock stops ticking.
- Note 2: Peripheral function interrupts are affected by the CM0 register's CM02 bit (wait mode time peripheral function clock stop bit). The resets and interrupts usable for the cause of return from wait mode and the condition under which they can be used are listed in Table 1.

Table 1. Resets and Interrupts Usable for the Cause of Return from Wait Mode and Usage Conditions

Table 1. Resets and interrupts Osable for the Cause of Return from wait mode and Osage Conditions				
Reset and interrupt		CM02 = 1 (peripheral function clock f1 turned off when in wait mode)		
NMI interrupt	Usable	Usable		
Serial interface interrupt	Usable when operating with internal or external clock	Usable when operating with external clock		
Key input interrupt	Usable	Usable		
A/D conversion interrupt	Usable in single shot or single sweep mode	Do not use		
Timer A interrupt Timer B interrupt	Usable in all modes	Usable in event count mode or when the count source is fC32 or fOCO-S		
INT interrupt	Usable	Usable		
Voltage-down detection interrupt	Usable	Usable		
Hardware reset 1	Usable			
Hardware reset 2	Usable			
Watchdog timer reset	Usable when CSPRO bit = 1 (count source protection mode enabled)			

2. Introduction

The application example described in this document applies to the following MCU:

• MCU: M16C/64 group

This application note can be used with other M16C Family MCUs which have the same special function registers (SFRs) as the above group. Check the manual for any modifications to functions. Careful evaluation is recommended before using the program described in this application note.



3. Setup Procedure

The following explains how to set the registers to enter wait mode and how the device will operate in wait mode. The setup procedure is shown in Figure 1.

- (1) Set the I flag to 0.
- (2) Set up the ILVL2–ILVL0 bits (interrupt priority level).
 - When using a hardware reset, NMI interrupt or voltage-down detection interrupt to return from wait mode
 - Set all of the ILVL2-ILVL0 bits for peripheral function interrupts to 000b (interrupt disabled).
 - When using a peripheral function interrupt to return from wait mode Set the interrupt priority level in the ILVL2–ILVL0 bits for the peripheral function interrupt used for return from wait mode.
 - Set the ILVL2–ILVL0 bits for the peripheral function interrupts not used for return from wait mode to 000b (interrupt disabled).
- (3) Set the PRC0 bit of the PRCR register to 1 (write enabled).
- (4) If the CM11 bit of the CM1 register is 1 (PLL clock selected for the CPU clock), set the CM11 bit to 0 (main clock selected for the CPU clock). Note 1
- (5) Set the I flag to 1.
- (6) Execute the WAIT instruction.(Insert at least 4 NOP instructions after the WAIT instruction.)

Note 1: To reduce the amount of power consumed in the chip during wait mode, set the PLC07 bit of the PLC register to 0 (PLL turned off). In the sample program, the PLC07 bit is set to 0.



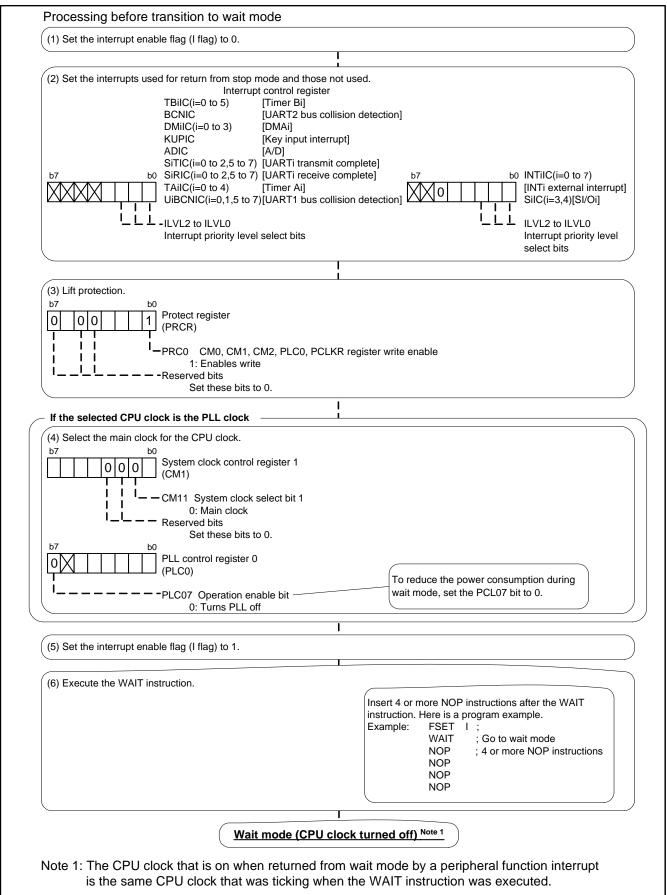


Figure 1. Example of Register Setup for Entering Wait Mode



4. Sample Programming Code

A sample program can be downloaded from the Renesas Technology website. To download, click "Application Notes" in the left-hand side menu of the M16C Family page.

5. Reference Documents

Hardware manual

M16C/64 Group Hardware Manual (Get the latest version from the Renesas Technology website.)

Technical updates and technical news

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