

# RZ Family

## Visual AI SLAM Solution Guide

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### Introduction

This application note describes the introduction of the Visual AI SLAM solution, which combines AI and SLAM (Simultaneous Localization And Mapping). The Visual AI SLAM solution is a solution that simultaneously performs location estimation (Localization) and driving map generation (Mapping) using images acquired from cameras mounted on automatic guided vehicles.

### Target Devices

RZ/V2H series

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## 1. Overview of Visual AI SLAM (YOLO-Planar-SLAM-DRP) and how to get

### 1.1 Overview

The Visual AI SLAM Solution developed based on [YoloPlanarSLAM](#). Visual AI SLAM Solution is released under a GPLv3 license.

This solution is realized by running the object detection AI model YOLO with the AI Accelerator (DRP-AI) in the Renesas AI MPU RZ/V2H and further image processing with the Vision Accelerator (DRP). This solution can be confirmed to operate with the RZ/V2H evaluation board kit.

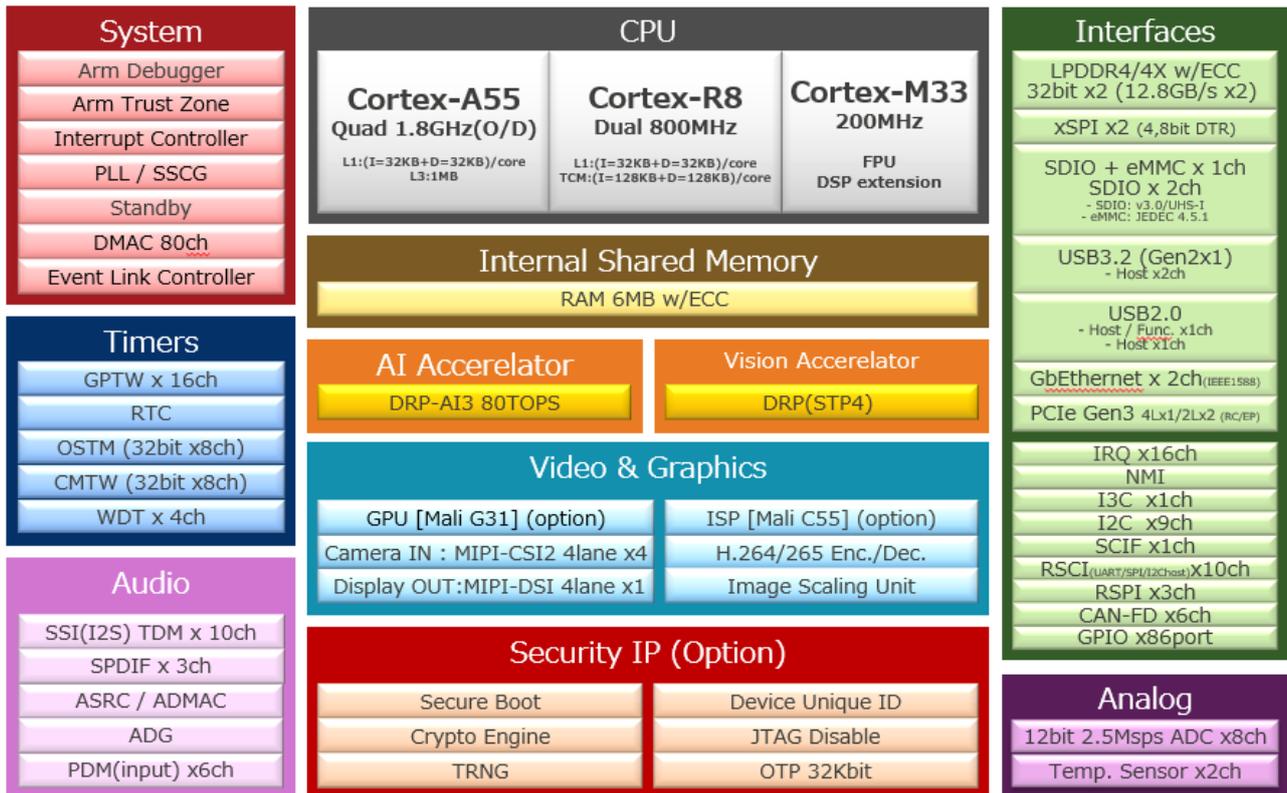


Figure 1-1 RZ/V2H System Block

#### AI-Accelerator : DRP-AI

DRP-AI consists of AI-MAC (multiply-accumulate processor) and DRP (reconfigurable processor). AI processing can be executed at high speed and low power consumption by assigning AI-MAC for operations on the convolution layer and fully connected layer, and DRP for other complex processing such as preprocessing and pooling layer. For more information, please refer to [AI Accelerator: DRP-AI](#) Web.

#### Vision Accelerator : DRP

The Dynamically Reconfigurable Processor (DRP) technology from Renesas is special purpose hardware built into select RZ Family microprocessor units (MPUs) that dramatically accelerates image processing algorithms by as much as 10X, or more. It combines the high performance of hardware solutions with the flexibility and expansion capability of a CPU. For more information, please refer to [Vision Accelerator : DRP](#) Web.

## 1.2 Use and Support

This solution is available free of charge. Please evaluate this solution thoroughly before using it in your products. For customization of this solution, please contact [Computermind Corp.](#)

Contact: [oss\\_slam\\_contact@compmind.co.jp](mailto:oss_slam_contact@compmind.co.jp)

## 1.3 How to get

Evaluation boards and software are available at the following URLs.

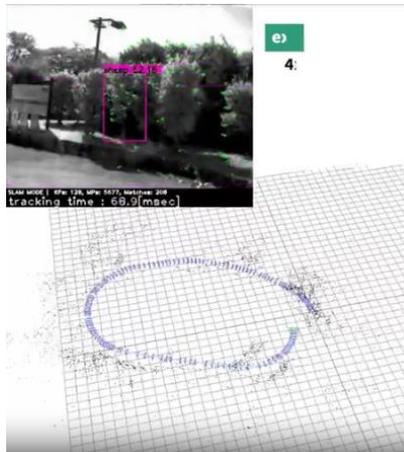
- ✓ RZ/V2H Evaluation Board Kit

[RZ/V2H-EVK - RZ/V2H Quad-core Vision AI MPU Evaluation Kit | Renesas](#)



- ✓ Visual AI SLAM (YOLO-Planar-SLAM-DRP) Solution

[GitHub - ComputermindCorp/yolo-planar-slam-drp: DRP-optimized version of yolo-planer-slam](#)



## 1.4 Target Application

- AMR (Autonomous Mobile Robot)
- AGV (Automatic Guided Vehicle)
- Lawnmower
- Service Robot
- Robot vacuum cleaner
- UAV(Drone)

## 2. Feature and Benefit of Visual AI SLAM Solution

### 2.1 Feature

The key features of this solution are processing speed and low power consumption. The increased processing speed and low power consumption are achieved by processing a portion of the YoloPlanarSLAM processing shown in Figure 2-1 using DRP-AI and DRP in the RZ/V2H.

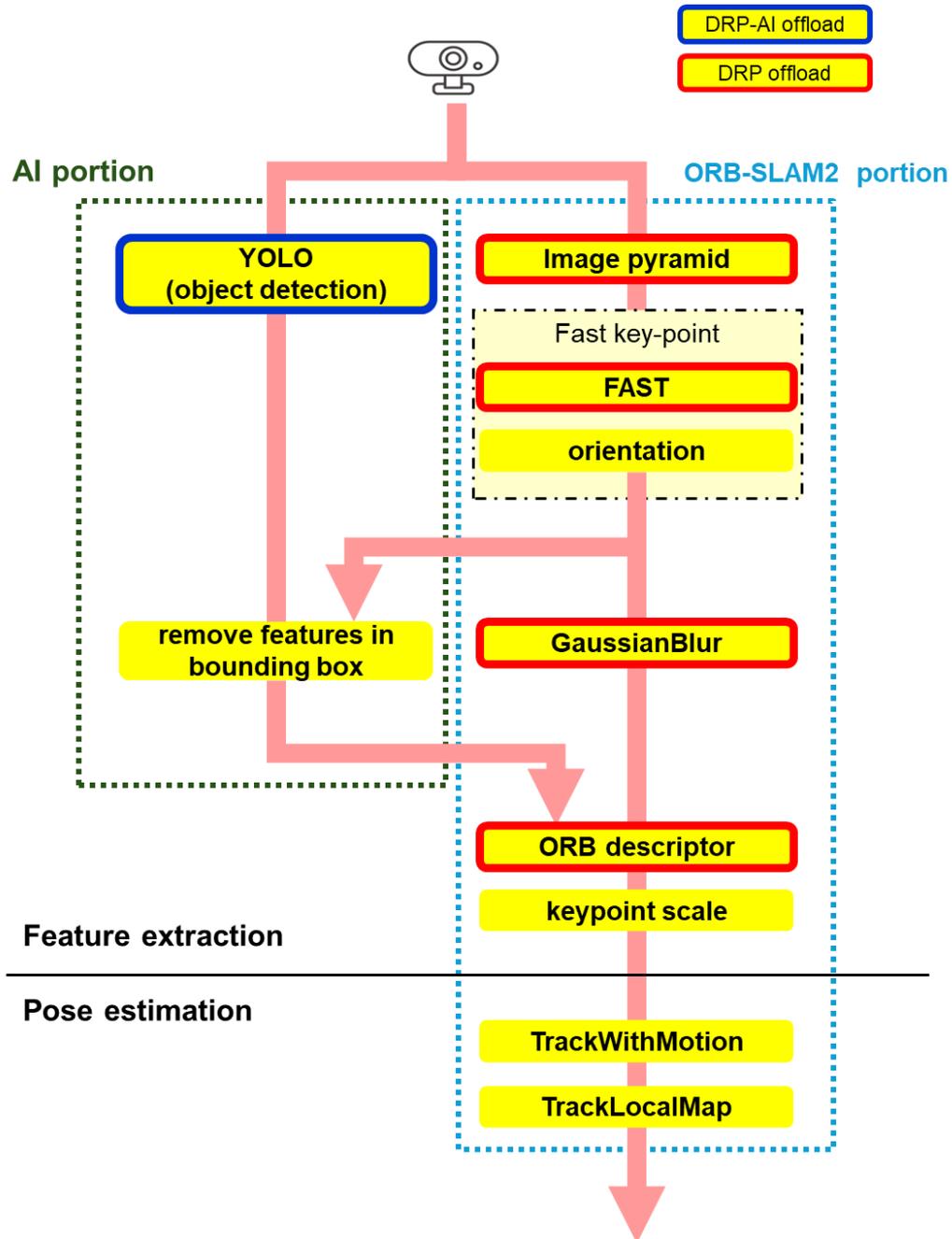


Figure 2-1 Tracking Operation Flowchart

Figure 2-2 shows the processing time when AI processing is performed with DRP-AI and CPU. The Visual AI SLAM solution uses the object detection model YOLOx-s and is up to 448x faster. This processing performance is also shown on the [DRP-AI GitHub](#).

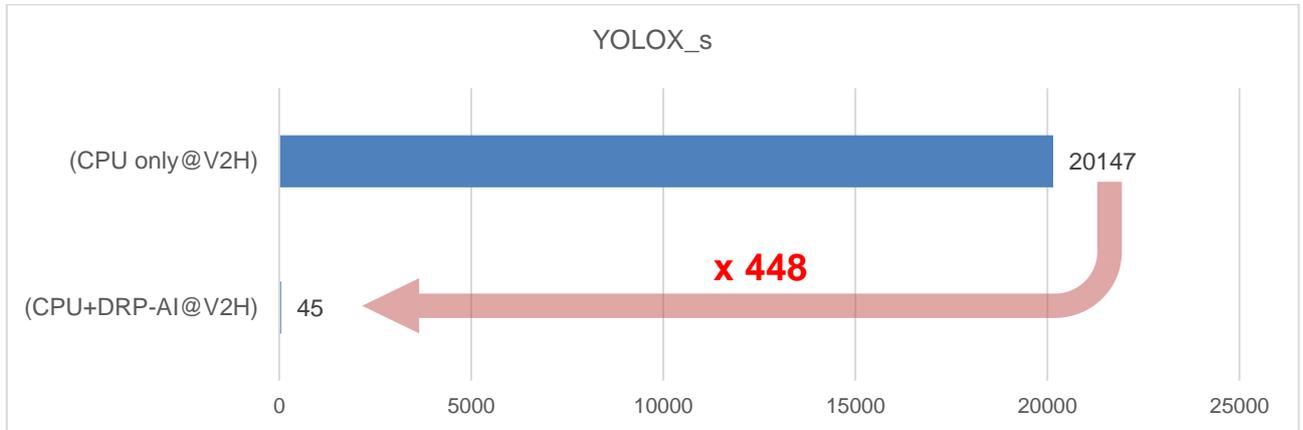


Figure 2-2 Comparison of DRP-AI and CPU AI processing performance

Figure 2-3 shows a comparison of image processing performance between DRP and CPU. The key to the processing speed improvement is FAST processing, which is approximately 12 times faster than CPU.

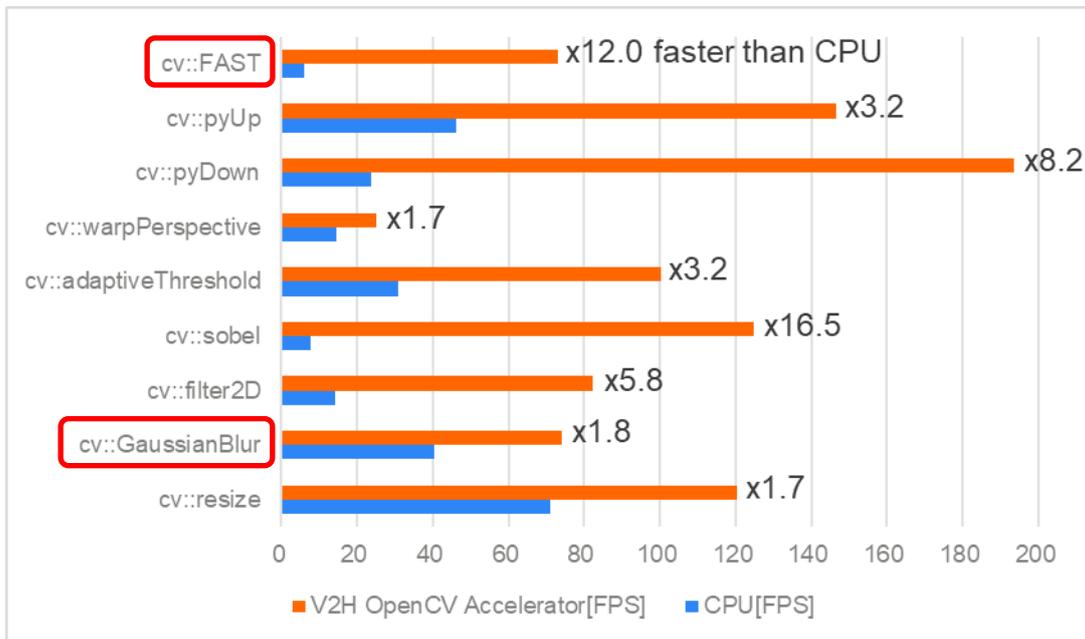


Figure 2-3 Comparison of DRP and CPU image processing performance

## 2.2 Benefit

The Visual AI SLAM solution is capable of smoothly executing the loop closing shown in the red circle in Figure 2-4 by accelerating the processing with DRP-AI and DRP, thereby reducing the time required to generate an accurate driving map.

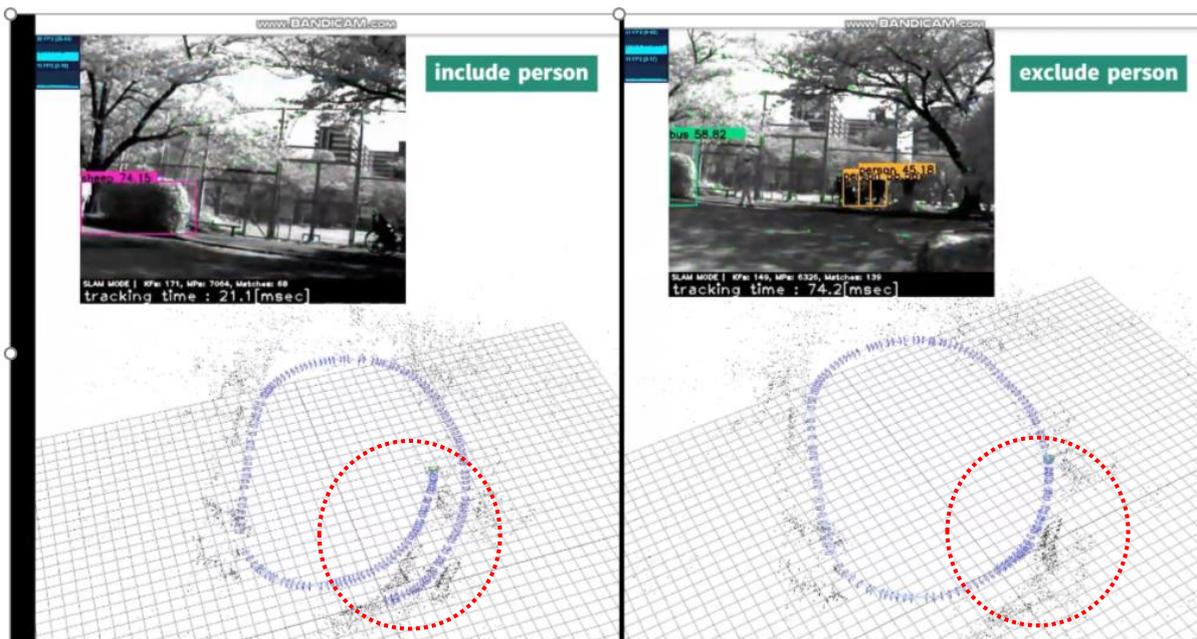


Figure 2-4 Loop-closing

### 3. Operating Environment for Visual AI SLAM Solution

To confirm the operation of this solution, the environment shown in Table 3-1 is required.

Table 3-1 Operating Environment

Item	Description
Target board	RZ/V2H EVK
Linux PC	Build embedded Linux, Create microSD Card. Ubuntu version 20.04 LTS (64 bit OS must be used.) 100GB free space on HDD is necessary.
Windows PC	For communication with target board. Windows10 recommended.
Terminal software	Terminal software to control the serial console of the target board. (Tera Term is recommended) Available at <a href="https://teratermproject.github.io">https://teratermproject.github.io</a>
VCP Driver	Virtual COM port driver Driver for communication between Windows PC and target board via USB <a href="http://www.ftdichip.com/Drivers/VCP.htm">http://www.ftdichip.com/Drivers/VCP.htm</a> Please install VCP Driver corresponding to the target board.
Broadband router	DHCP server
microSD card	Required capacity: 8 GB or more. Store Kernel image, device tree, Linux root system.
USB camera	ELP-USBGS720P02-L36 (Camera is not required when using Datasets.)
USB cable micro-B	Connect Win PC and Target board. (Accessories for RZ/V2H EVK)
USB cable Type-C PD 100W / 5A	Connect Win PC and Target board. The board will not power on if the cable is less than 100W.
FFC cable	Connect CPU board and EXP board. (Accessories for RZ/V2H EVK)

Figure 3-1 shows a connection diagram of the V2H evaluation board and other components to operate the Visual AI SLAM Solution.

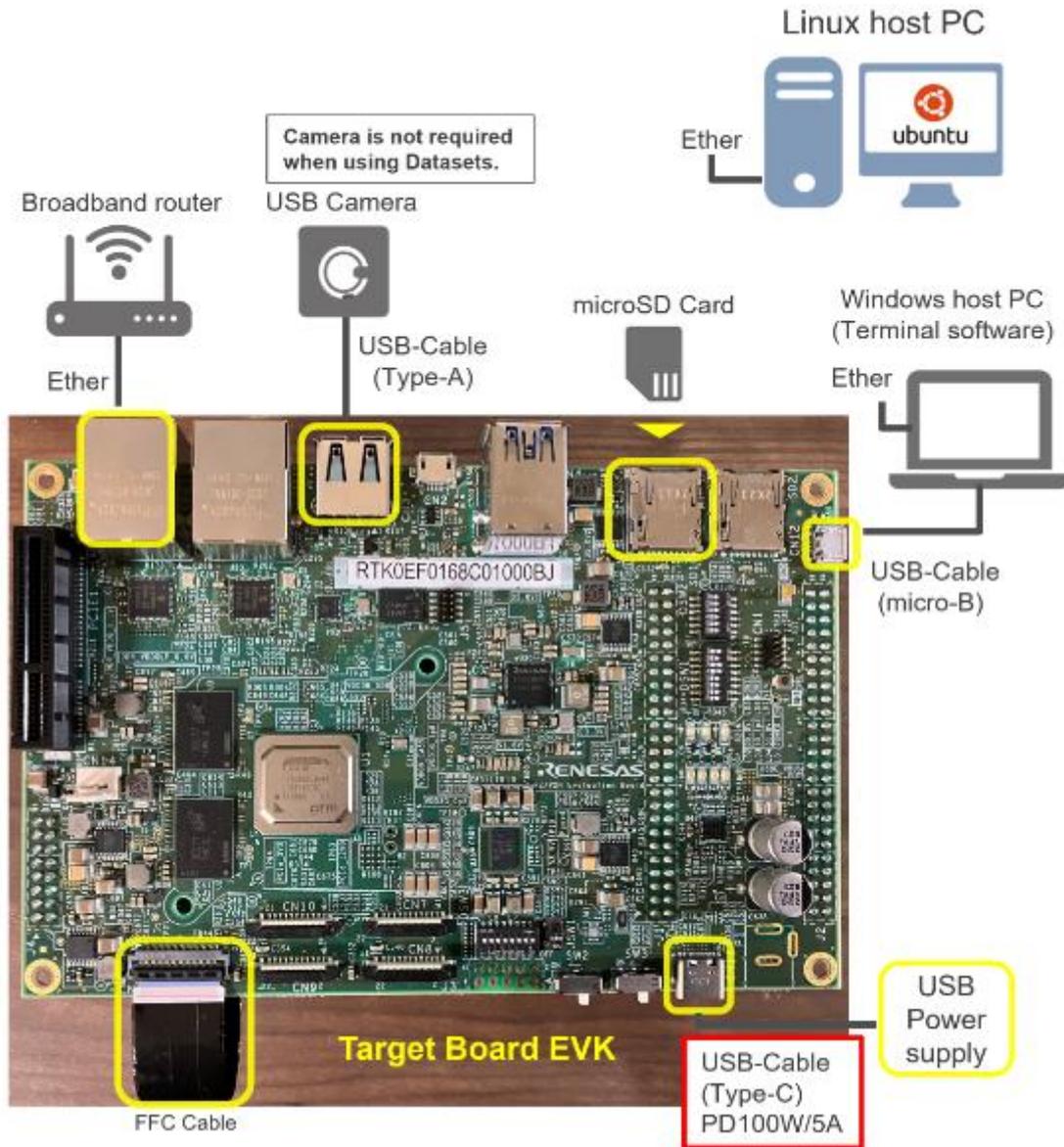


Figure 3-1 Connection diagram

### 4. Implementation of Visual AI SLAM solution

Implementation flowchart of the Visual AI SLAM solution is shown below. For detailed instructions and operations, please refer to the Visual AI SLAM GitHub below.

Visual AI SLAM GitHub :

[yolo-planar-slam-drp/installguide.md at main · ComputermindCorp/yolo-planar-slam-drp · GitHub](https://github.com/ComputermindCorp/yolo-planar-slam-drp/blob/main/yolo-planar-slam-drp/installguide.md)

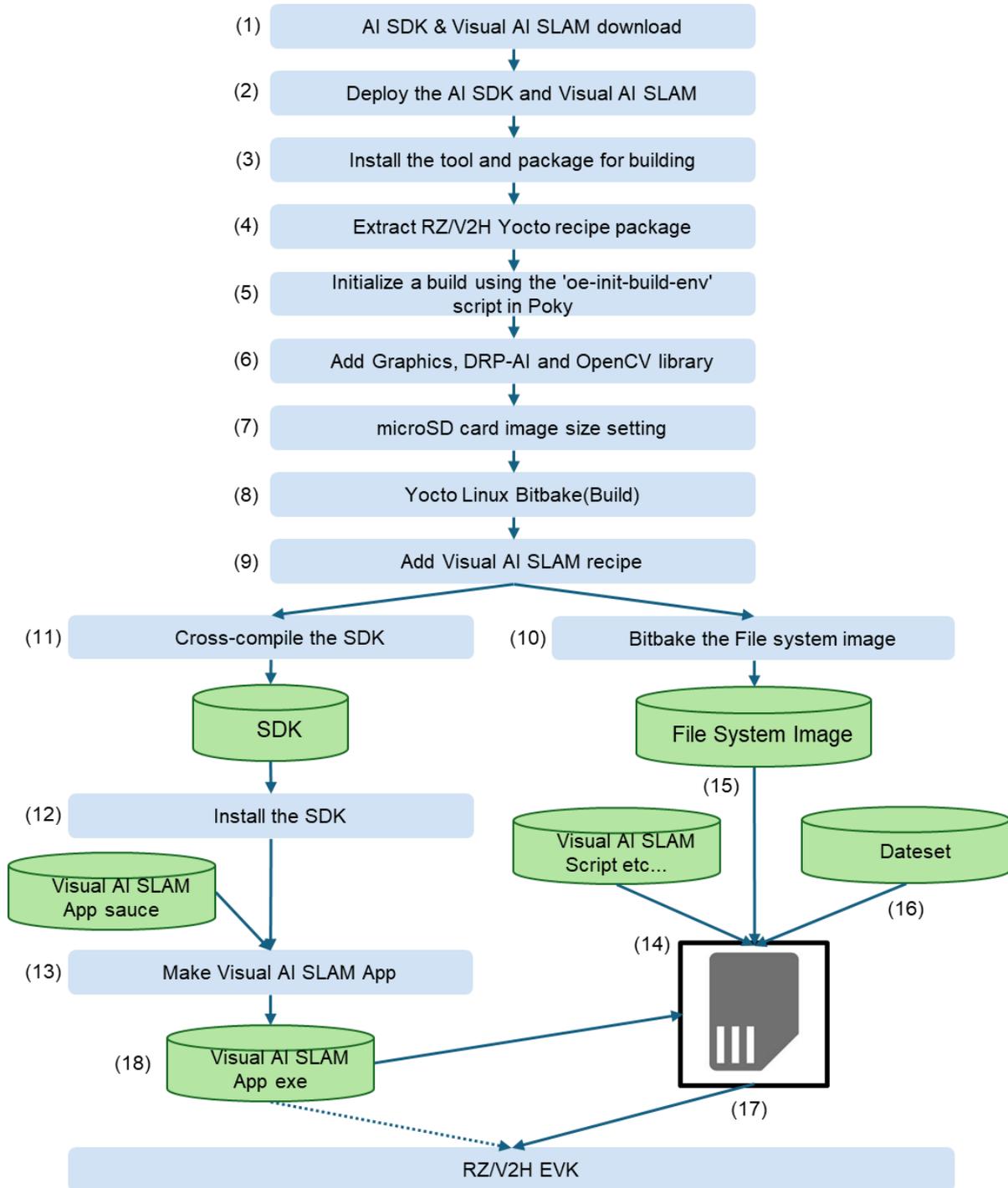


Figure 4-1 Implementation flowchart

## 5. Glossary

The terms within this application node are listed in the table below.

Item	Description
SLAM	Technology for generating self-position and driving maps
YoloPlanarSLAM	Technology that combines SLAM with an object detection AI model: YOLO to improve the accuracy of self-position and driving map generation
DRP-AI	Renesas Electronics' original hardware AI accelerator
DRP	Renesas Electronics' original dynamic reconstruction processor
AI SDK	Renesas Electronics AI development environment

**Revision History**

Rev.	Date	Description	
		Page	Summary
1.00	Sep.27.24	-	First release

## General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

### 1. Precaution against Electrostatic Discharge (ESD)

A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity.

Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

### 2. Processing at power-on

The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

### 3. Input of signal during power-off state

Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

### 4. Handling of unused pins

Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

### 5. Clock signals

After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

### 6. Voltage application waveform at input pin

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between  $V_{IL}$  (Max.) and  $V_{IH}$  (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between  $V_{IL}$  (Max.) and  $V_{IH}$  (Min.).

### 7. Prohibition of access to reserved addresses

Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

### 8. Differences between products

Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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