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SH7764 Group

Video Display Controller TFT-LCD Interfacing Example 1

Introduction

This application note shows the TFT-LCD interfacing example using the SH7764 Microcontrollers (MCUs) on-chip Video Display Controller (VDC2).

Target Device

SH7764 (R0K507764E001BR from Renesas Technology Corp.)

Contents

1. Preface

1.1 Specifications

The SH7764 MCU on-chip video display controller (VDC2) is connected with a TFT-LCD panel to display the graphic image.

1.2 Module Used

- Video display controller (VDC2)
- General-purpose I/O ports (GPIO)

1.3 Applicable Conditions

- MCU: SH7764
- Operating frequency:
  - CPU clock: 324 MHz
  - SuperHyway clock: 108 MHz
  - Peripheral clock: 54 MHz
  - Bus clock: 108 MHz
- Integrated development environment
  from Renesas Technology Corp.
- C compiler: SuperH RISC Engine Family C/C++ Compiler Package Ver.9.03 Release00
  from Renesas Technology Corp.
- Compiler options: Default settings of the High-performance Embedded Workshop
  -cpu=sh4a -endian=little -include="$(WORKSPDIR)\inc"
  -object="$(CONFIGDIR)\$(FILELEAF).obj" -debug -optimize=0
  -gbr=auto -chgincpath -errorpath
  -global_volatile=0 -opt_range=all -infinite_loop=0
  -del_vacant_loop=0 -struct_alloc=1 –nologo

1.4 Related Application Note

Refer to the related application notes as follows:

- SH7764 Group Application Note: SH7764 Example of Initialization (REJ06B0919)
- SH7764 Group Application Note: Video Display Controller TFT-LCD Interfacing Example 2 (REJ06B0921)

2. Description of the Sample Application

This application note shows the pin connection example and configuration example to display the graphic image by the VDC2. The specifications of the TFT-LCD panel used in this application note are shown in 2.2.

2.1 VDC2 Operation

2.1.1 Overview

The video display controller (VDC2) provides functions for reading four planes of graphic images (layers 1 to 4) stored in the external memory and overlaying them. It outputs 18-bit RGB video (each color is represented by six bits) and digital video data conforming to BTA T-1004.

2.1.2 Features

Table 1 lists the VDC2 features.

Table 1 VDC2 Features

Item	Function
Operating frequency	6.0 MHz to 36.0 MHz (depends on the display panel size)
Input image format	16-bit RGB565 progressive
Display size	18-bit progressive RGB output 720 × 480 (NTSC) 720 × 576 (PAL) 320 × 240 (QVGA) 640 × 480 (VGA) 800 × 480 (WVGA)
Display planes	Up to four planes (layers 1 to 4)
α blending	Mixes layers 1 to 4 according to the transparency
Chroma-keying	Applies chroma-key processing to the specified RGB color
Output video format	RGB666 progressive video output
Sync signal output	Either a combination of Vsync, Hsync, data enable, and COM/CDE signals
External sync mode	The VDC2 can operate with external sync signals (EX-VSYNC and EX-HSYNC) and the panel clock

2.1.3 I/O Pins

Table 2 lists the VDC2 I/O pins.

Table 2 VDC2 I/O Pins

Symbol	I/O	Pin Name	Function
DR[5:0]	Output	Digital red data	Video data output pins
DG[5:0]	Output	Digital green data	Video data output pins
DB[5:0]	Output	Digital blue data	Video data output pins
VSYNC	Output	Vertical sync signal	Vertical sync signal
HSYNC	Output	Horizontal sync signal	Horizontal sync signal
DE_V	Output	Vertical data enable signal	Vertical data enable signal
DE_H/DE_C	Output	Horizontal data enable signal/display enable signal	Horizontal data enable signal/display enable signal
COM/CDE	Output	Gate control signal/chroma data enable signal	Gate control signal/display enable signal (asserted when the data matches the chroma-key color specified in the register).
BT_DATA[7:0]	Output	BTA-T1004 display data	BTA-T1004 display data output pins
BT_VSYNC	Output	BTA-T1004 vertical sync	BTA-T1004 vertical sync signal
BT_DE_C	Output	BTA-T1004 display enable	BTA-T1004 display enable signal
EX_VSYNC	Input	VSYNC input	VSYNC input pin used in external sync mode
EX_HSYNC	Input	HSYNC input	HSYNC input pin used in external sync mode
DCLKIN	Input	Panel source clock input	Display source clock input pin. Input an appropriate frequency depending on the display panel.
DCLKOUT	Output	Panel clock output	Panel clock output pin

2.1.4 VDC2 Configuration

Table 3 lists the each functional block. Figure 1 shows the VDC2 block diagram.

Table 3 VDC2 Functional Blocks

Block Name	Overview of Functions
Graphics block 1	Reads a graphic image (RGB565: layer 1) stored in the external memory through the pixel bus and outputs it to graphics block 2.
Graphics block 2	Reads a graphic image (RGB565: layer 2) stored in the external memory through the pixel bus, overlays it on the output from graphics block 1, and outputs the result to graphics block 3.
Graphics block 3	Reads a graphic image (RGB565: layer 3) stored in the external memory through the pixel bus, overlays it on the output from graphics block 2, and outputs the result to graphics block 4.
Graphics block 4	Reads a graphic image (RGB565: layer 4) stored in the external memory through the pixel bus, overlays it on the output from graphics block 3, and outputs the resultant image data.
Display control block	Converts the output (RGB) from graphics block 4 into the YCbCr (4:2:2) format and outputs the data in the 8:4:4 parallel format conforming to the BTA T-1004 standard. It also outputs the control signals for the TFT-LCD panel.
Input timing control block	Selects the timing of the external sync signal input with respect to the clock rising or falling edge and selects the sync signal polarity.
Output timing control block	Controls the timing of the sync signal output with respect to the clock rising or falling edge and controls the sync signal polarity. It also controls the timing of the RGB666 video output signals with respect to the clock rising or falling edge.

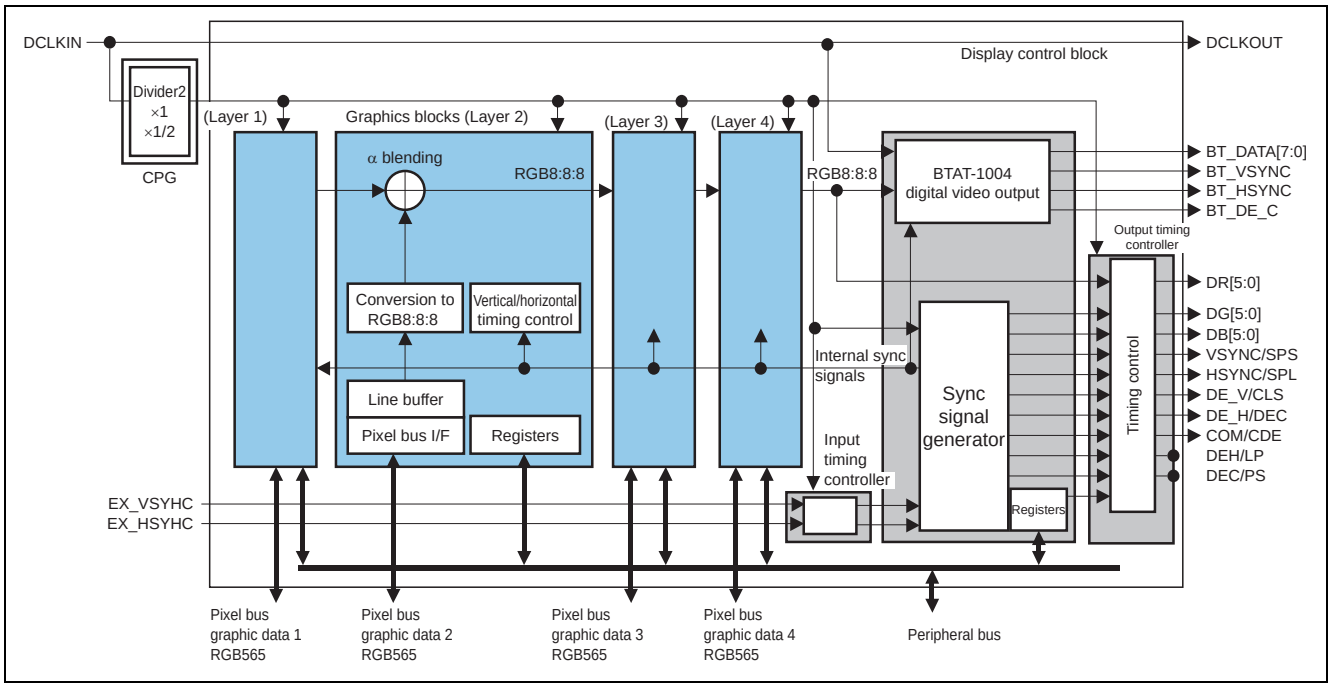


Figure 1 VDC2 Block Diagram

2.1.5 VDC2 Functions

The graphics blocks display in the RGB565 (16-bit) format the image data stored in the memory area. The graphics blocks control display by using the external input sync signals or internally generated sync signals. A single plane of an image can be displayed, and two to four planes of images can also be displayed through overlay processing. In overlaid display, the lower-layer images can be displayed through the current image (current layer) by specifying the α control area for the current layer (transparent processing). The transparency can be specified in 1/256 × 100% units. Transparent processing for the lower-layer images is also available through chroma-keying, which specifies the transparency of the specified target color.

Figure 2 shows the graphics image display example. To simplify the configuration, the video display, α control and the chroma-keying are not allowed in the following example.

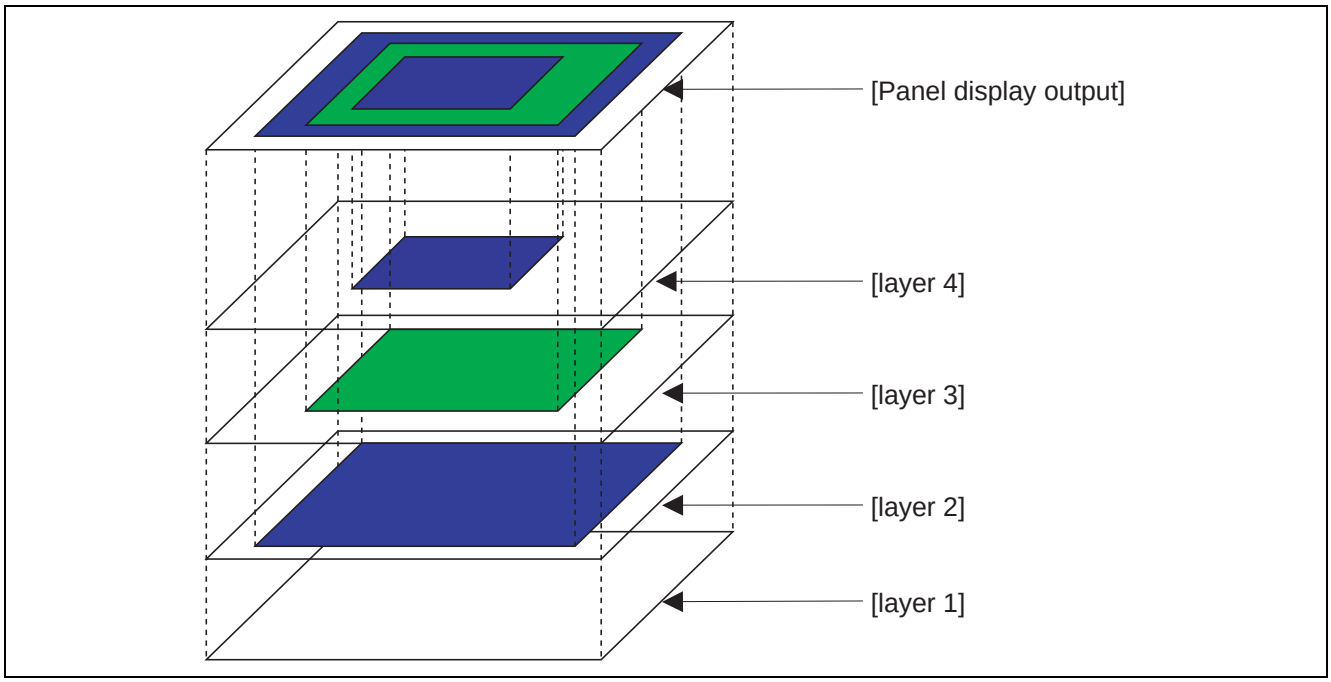


Figure 2 Graphics Image Display Example

2.1.6 Sync Signal Output Format

Figure 3 shows an example of the format for the output of synchronizing signals to the TFT-LCD panel. The figure illustrates the timing of synchronizing signals that are set in the display control and graphics blocks and the relationship among the synchronous signal area including the blanking interval, the data enable area, and the graphic image area. Make settings that suit the TFT-LCD panel you will be using.

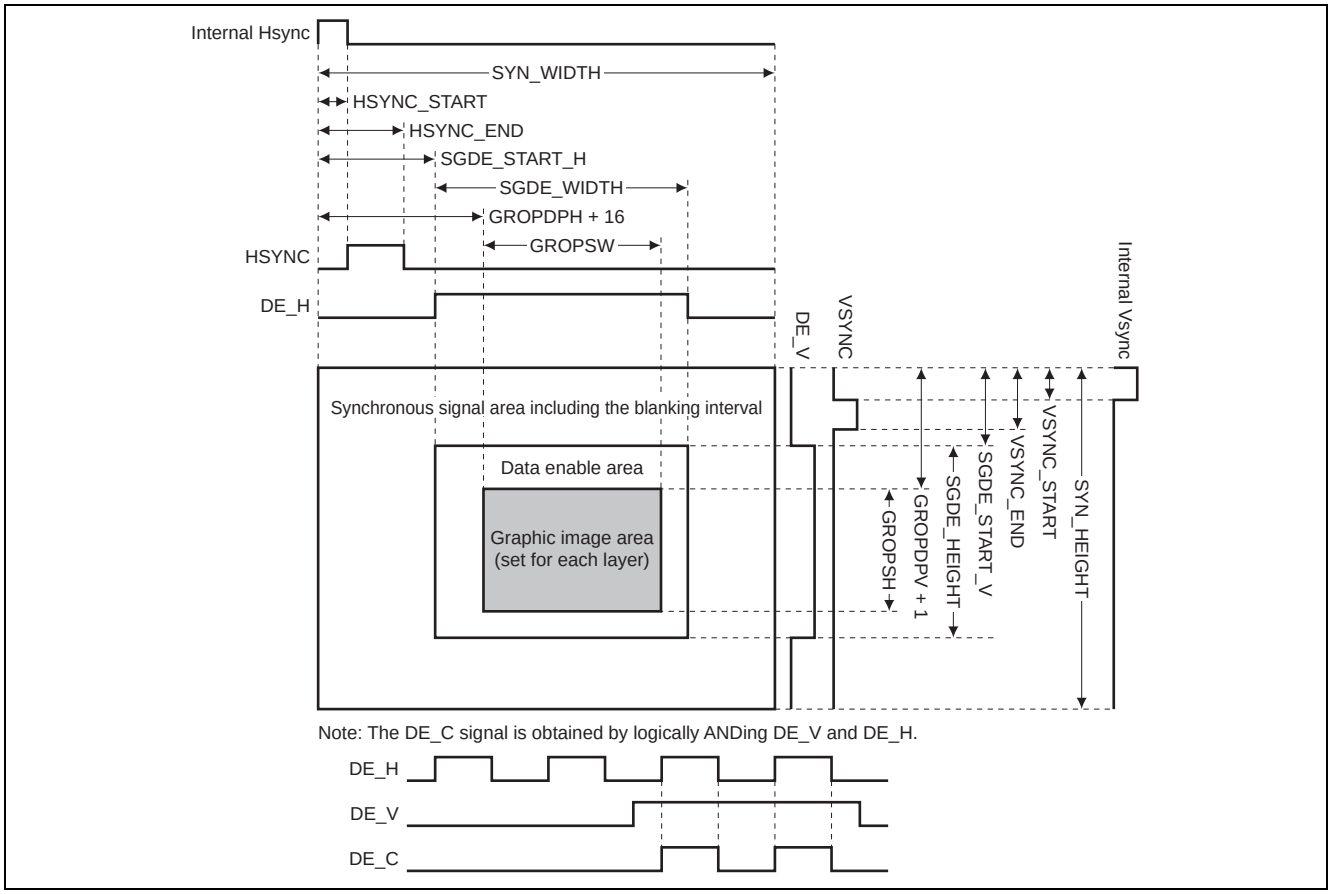


Figure 3 Screen Format

2.2 TFT-LCD Panel Specifications

Table 4 lists the specification of the TFT-LCD panel to use in this application. The specifications of the TFT-LCD panel used for this application note (TX18D55VM1CAA, manufactured by Hitachi Displays, Ltd.) are listed in the table below. As detailed specifications differ with the TFT-LCD panel, be sure to check the data sheet for the product you will be using.

2.2.1 General Specifications

Table 4 lists the general specifications of the TFT-LCD panel used in this application.

Table 4 TFT-LCD Panel General Specifications (Excerpt from Datasheet)

Item	Specifications
Resolution	Wide-VGA
Number of pixels	H 800 × V 480 (Number of dots: H (800 × 3) × V 480)
Pixel configuration	R, G, B vertical stripes
Number of colors	260,000 colors
Input signal	CMOS RGB (6 bits each digital)

2.2.2 Pin Functions

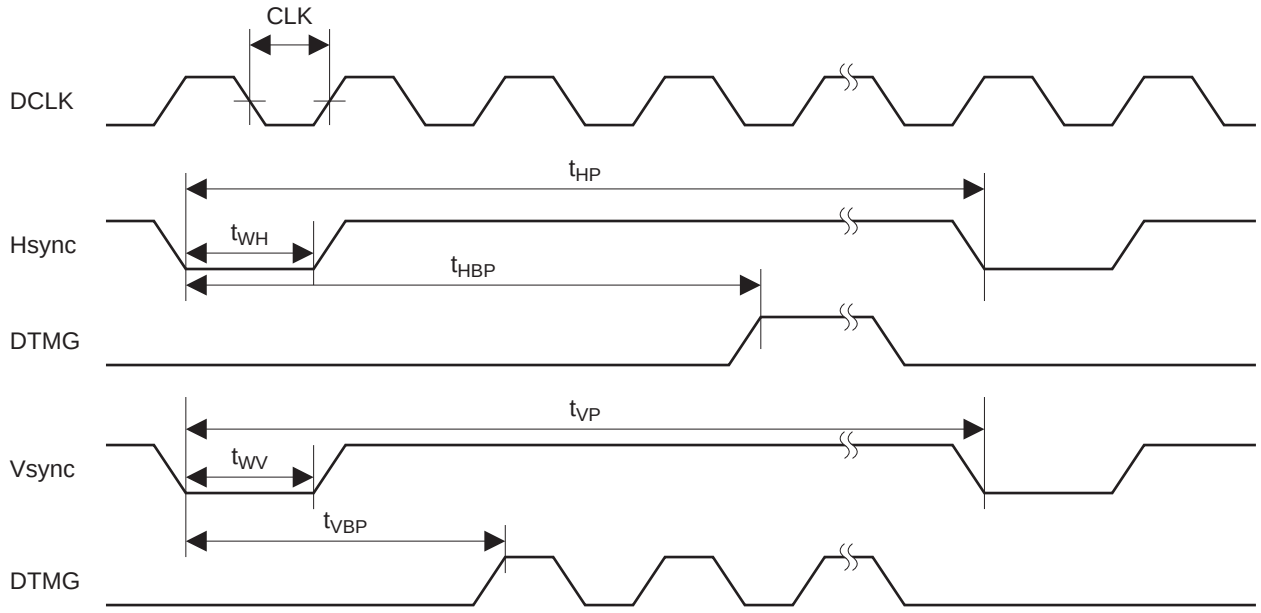
Table 5 lists the pin functions of the TFT-LCD panel used in this application.

Table 5 TFT-LCD Panel Pin Functions (Excerpt from Datasheet)

Symbol	Description
DCLK	Dot clock
DTMG	Display timing signal
R5-0	Red data signal (MSB: R5)
G5-0	Green data signal (MSB: G5)
B5-0	Blue data signal (MSB: B5)

2.2.3 Interface Timing

Figure 4 shows the interface timing of the TFT-LCD panel used in this application. Table 6 lists the timing characteristics.



Note: Data are latched on falling edges of DCLK.
Operation is with synchronization obtained by using the DTMG signal only.
While no valid data are being input, the DTMG signal must be at the low level.

Figure 4 TFT-LCD Panel Interface Timing Example (Excerpt from Datasheet)

Table 6 TFT-LCD Panel Timing Characteristics (Excerpt from Datasheet)

Item		Symbol	Min	Typ	Max	Unit
DCLK	Cycle time	t_{CLK}	25	30	33	ns
Hsync	Cycle time	t_{HP}	944	1056	1088	t_{CLK}
	Valid width	t_{WH}	4	128	—	
Vsync	Cycle time	t_{VP}	515	525	610	t_{HP}
	Valid width	t_{WV}	1	2	—	
DTMG	Horizontal back porch time	t_{HBP}	7	88	—	t_{CLK}
	Vertical back porch time	t_{VBP}	4	32	—	t_{HP}

2.3 TFT-LCD Panel Circuit Example

2.3.1 Pin Connection Example

Figure 5 shows the TFT-LCD panel hardware connection in this application.

Operation of the TX18D55VM1CAA is with synchronization obtained by using the display-timing signal (DTMG) only, so the HSYNC and VSYNC signals need not be connected. The display-enable signal (DE_C) is connected to the DTMG input. The source clock signal for the panel (input to DCLKIN) is output through DCLKOUT with no frequency multiplication.

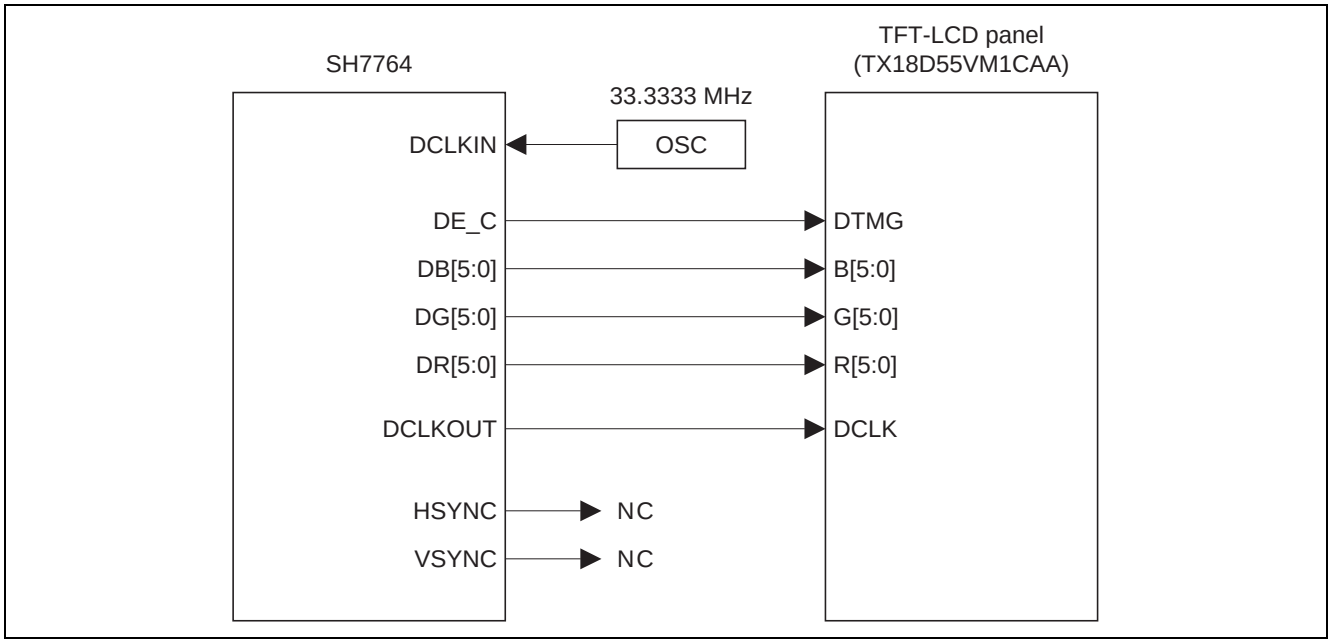


Figure 5 TFT-LCD Panel Hardware Connection

2.4 Sample Program Specifications

This section describes the specifications of the sample program and shows the flow chart of each processing.

2.4.1 Specifications

- Outputs the graphic image to the WVGA size (V 800 × H 480) TFT-LCD panel.
- Displays two planes in which all dots are displayed either in green or in blue. Displays are switched alternately.

2.4.2 Main Flow Chart of the Sample Program

Figure 6 shows the main flow chart of the sample program. The sample program initializes the VDC2 as shown in figure 7 to figure 9 to display the still image in the TFT-LCD panel. Then, the sample program repeatedly executes the processing shown in figure 10 and switches between two graphic images.

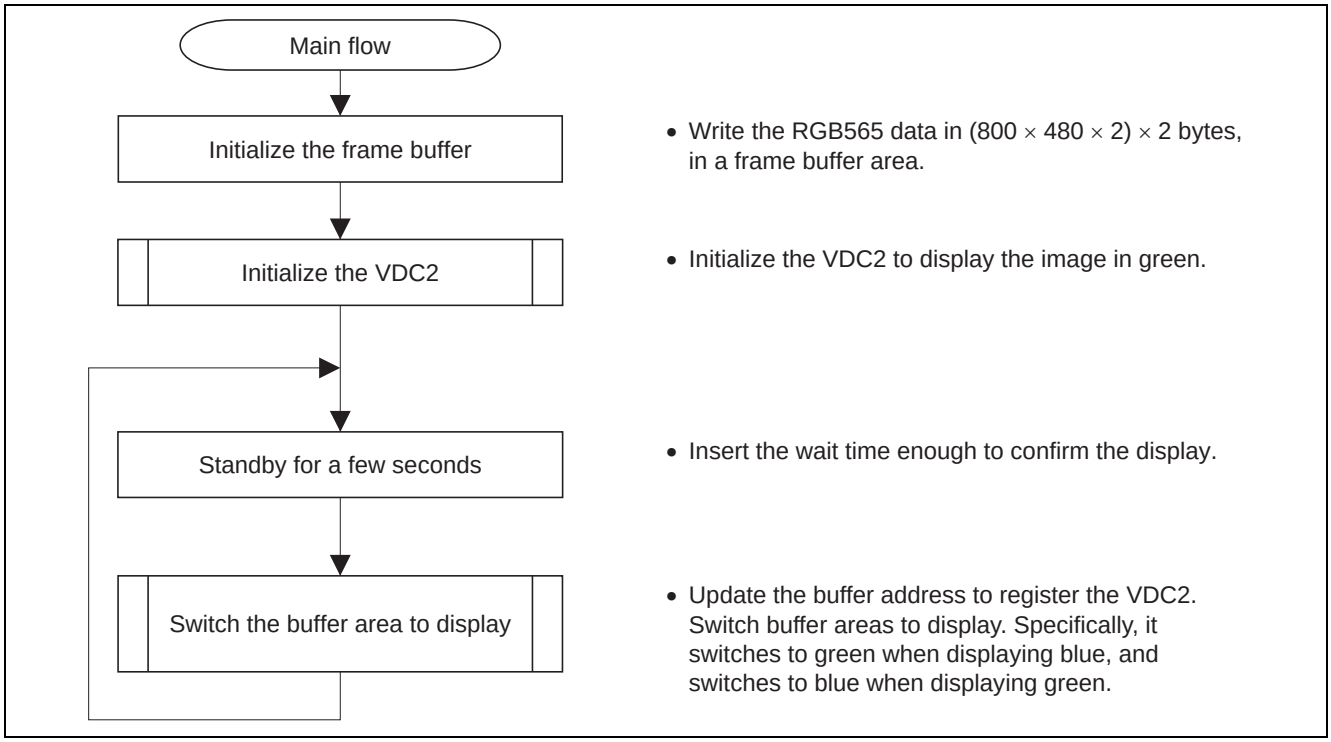


Figure 6 Sample Program Main Flow

2.4.3 Initialization of the VDC2

Figure 7 shows the flow for initialization of the VDC2.

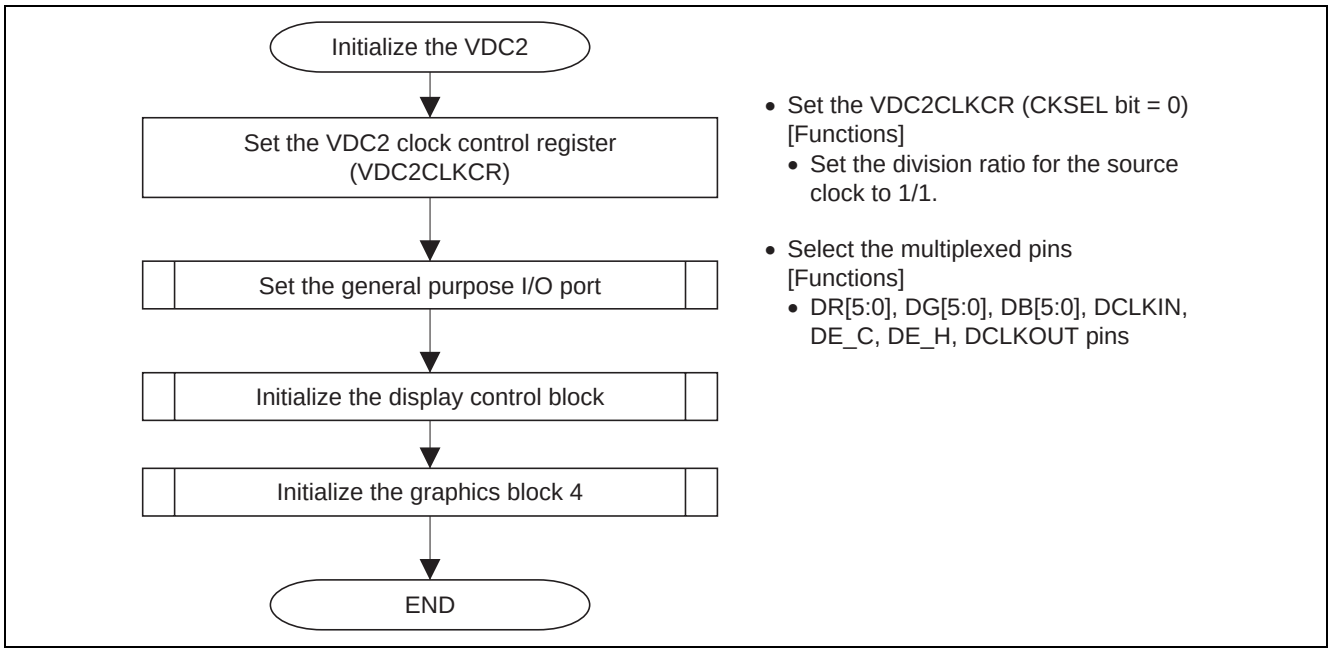


Figure 7 Flow for Initialization of the VDC2

2.4.4 Setting the Display Control Block

Figure 8 shows the setting examples of the display control block. Follow section 2.4.5 and this procedure to set the control signal output for the TFT-LCD panel. Values listed in figure 8 are set according to the TFT-LCD panel specifications described in section 2.2.

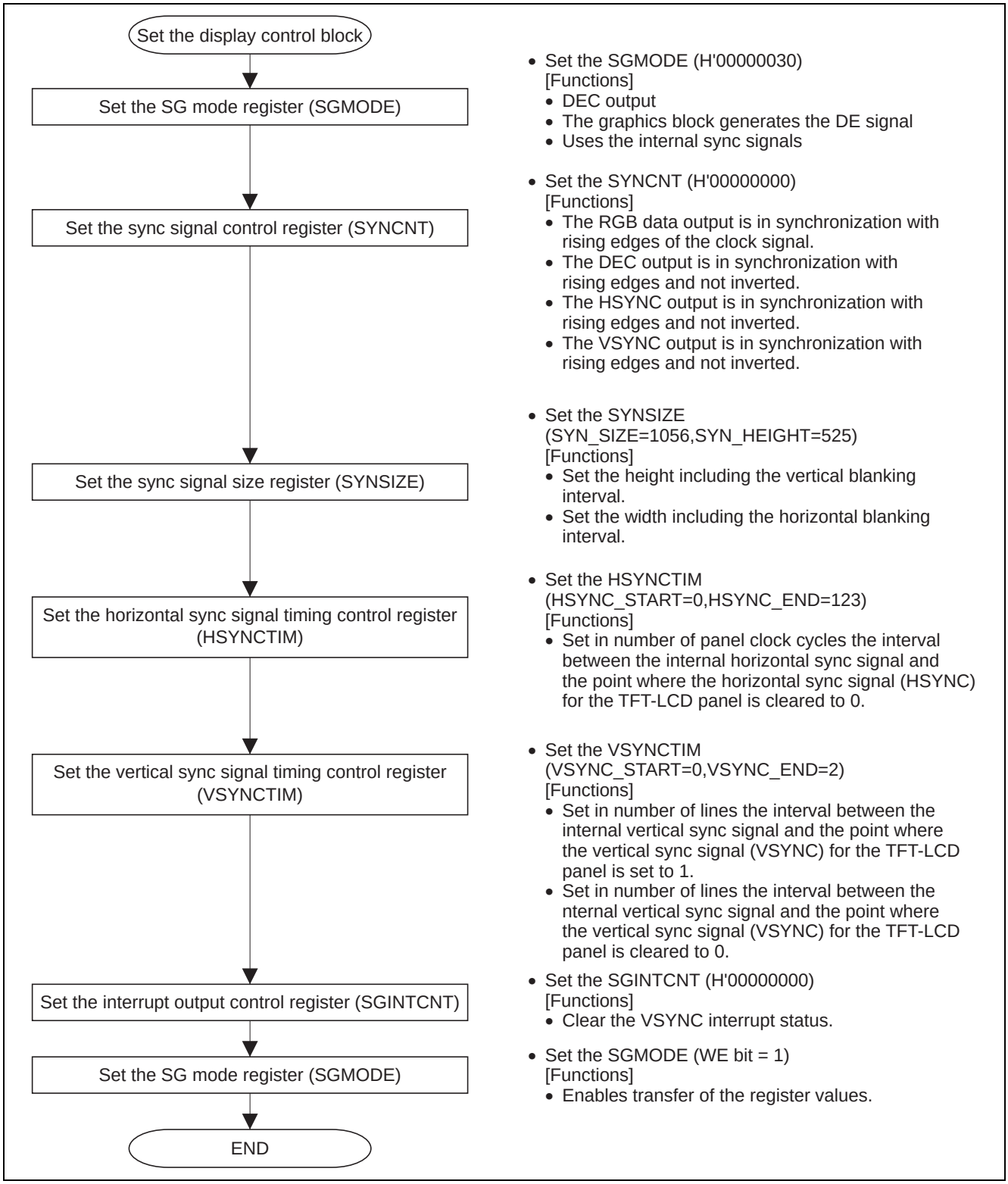


Figure 8 Setting Examples of the Graphics Control Block

2.4.5 Setting the Graphics Blocks

Figure 9 shows the setting example of the graphics block. Follow section 2.4.4 and this procedure to display the graphics image data in a specified area of the panel.

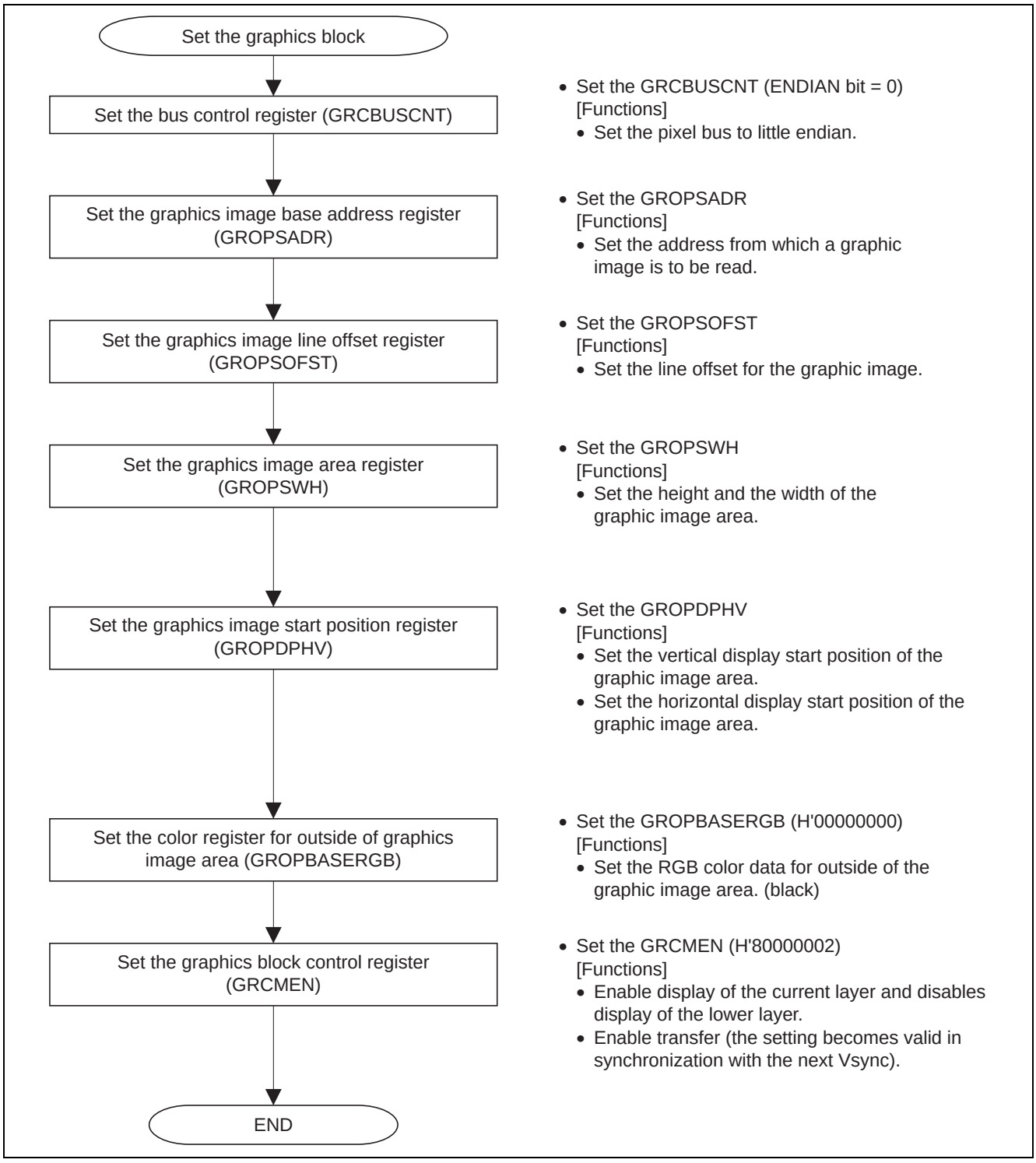


Figure 9 Setting Examples of the Graphics Block

2.4.6 Updating the Graphics Image Data

Figure 10 shows the flow chart of updating the graphics image data.

To avoid the images distorted on the panel, the graphics image data area is configured with more than two planes. After updating the data area, update the Graphics image base address register of the VDC2 to switch the read address to show the image data. Then, use the GRCMEN register to transfer the value in the graphics image base address register for the change to effect.

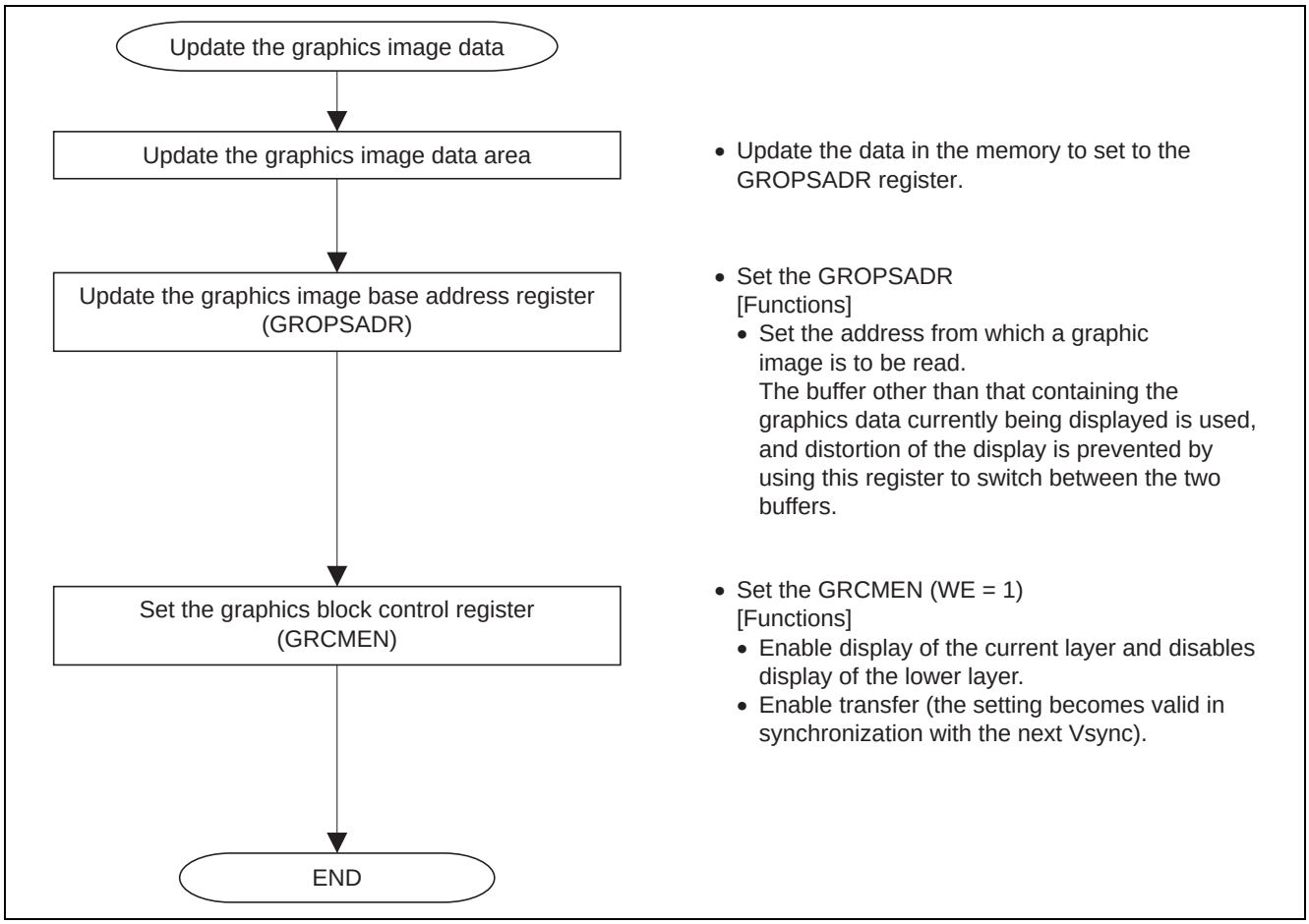


Figure 10 Graphics Image Data Update Example

3. Sample Program "vdc2.c"

3.1 Listings of Sample Program "Macro definition"

```
1     /*""FILE COMMENT""************ Technical reference data ************************
2     *
3     *       System Name : SH7764 Sample Program
4     *       File Name   : vdc2.c
5     *       Abstract    : VDC2 TFT-LCD Panel Display Example
6     *       Version     : 1.00.00
7     *       Device      : SH7764
8     *       Tool-Chain  : High-performance Embedded Workshop (Ver.4.05.01).
9     *                   : C/C++ compiler package for the SuperH RISC engine family
10    *                   :                              (Ver.9.03 Release00).
11    *       OS          : none
12    *       H/W Platform: R0K507764E001BR
13    *       Disclaimer  :
14    *                     <Note>
15    *                     This sample program is provided simply as a reference and
16    *                     its operation is not guaranteed.
17    *                     Use this sample program as a technical reference when
18    *                     developing software.
19    *
20    *       The information described here may contain technical inaccuracies or
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23    *       from these inaccuracies or errors.
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25    *       Copyright (C) 2009 Renesas Technology Corp. All Rights Reserved
26    *       AND Renesas Solutions Corp. All Rights Reserved
27    *
28    *       History     : June.01,2009 Ver.1.00.00
29    *""FILE COMMENT END""*************************************************************/
30    #include "iodefine.h"
31
32    /* ==== Macro definition ==== */
33    /* ---- TFT panel display module ---- */
34    #define TFT_TOTAL_CLOCK          1056   /* Width including the blanking interval    */
35    #define TFT_TOTAL_LINE           525    /* Height including the blanking interval   */
36    #define TFT_PANEL_CLOCK          800    /* Number of pixels in horizontal direction */
37    #define TFT_PANEL_LINE           480    /* Number of pixels in vertical direction   */
38    #define TFT_DTMG_START_H         88     /* Horizontal display start position */
39    #define TFT_DTMG_START_V         32     /* Vertical display start position   */
40    #define TFT_HSYNC_START          0      /* Hsync pulse width start position  */
41    #define TFT_HSYNC_END            123    /* Hsync pulse width end position    */
42    #define TFT_VSYNC_START          0      /* Vsync pulse width start position  */
43    #define TFT_VSYNC_END            2      /* Vsync pulse width end position    */
44    /* ---- Graphics block parameter ---- */
45    #define GRAPHICS4_Y_SIZE         TFT_PANEL_LINE
46              /* Height of graphics block 4 */
47    #define GRAPHICS4_X_SIZE         TFT_PANEL_CLOCK
48              /* Width of graphics block 4 */
49    #define GRAPHICS4_LINE_OFFSET    TFT_PANEL_CLOCK
50              /* Line offset of graphics block 4 */
51    #define GRAPHICS4_POS_Y          0
52              /* Display start position in vertical direction (0: Top of the panel) */
53    #define GRAPHICS4_POS_X          0
54              /* Display start position in horizontal direction (0: Leftmost of the panel) */
55    #define GRAPHICS4_BG_COLOR       0x0000
56              /* Color of graphics block 4: Black */
```

3.2 Listings of Sample Program "Function prototype declaration, Variable definition"

```
57    /* ==== Function prototype declaration ==== */
58    void vdc_main(void);
59    void vdc2_initial(void);
60    void vdc2_port_set(void);
61    void vdc2_display_control_initial(void);
62    void vdc2_graphic_layer4_initial(void);
63    void change_graphic(int idx);
64    void fill_rect(unsigned int x, unsigned int y,
65        unsigned int w, unsigned int h, unsigned short color,
66        unsigned int base_address, unsigned int line_offset);
67    void delay(void);
68
69    /* ==== Variable definition ==== */
70    #pragma section _VDC2_FRAME_BUFFER /* Places on a 16-byte boundary in the cache disabled area
71    */
72    unsigned short frame_buffer[2][TFT_PANEL_LINE][TFT_PANEL_CLOCK];
73    #pragma section
```

3.3 Listings of Sample Program "Display main"

```
/*""FUNC COMMENT""*************************************************************
 * ID          :
 * Outline     : Display main
 *-----------------------------------------------------------------------------
 * Include     :
 *-----------------------------------------------------------------------------
 * Declaration : void main(void);
 *-----------------------------------------------------------------------------
 * Function    : Switches frame buffers in a certain period of time to display
 *             : graphics images on the TFT-LCD panel.
 *-----------------------------------------------------------------------------
 * Argument    : void
 *-----------------------------------------------------------------------------
 * Return Value: void
 *""FUNC COMMENT END""*************************************************************/
void vdc_main(void)
{
    int idx = 0;

    /* ---- Initializes the frame buffer ---- */
    fill_rect(0,0,GRAPHICS4_X_SIZE,GRAPHICS4_Y_SIZE,0x07E0,
     (unsigned int)frame_buffer[0],GRAPHICS4_LINE_OFFSET);
      /* Fills the frame buffer 1 plane with green */

    fill_rect(0,0,GRAPHICS4_X_SIZE,GRAPHICS4_Y_SIZE,0x001f,
     (unsigned int)frame_buffer[1],GRAPHICS4_LINE_OFFSET);
      /* Fills the frame buffer 2 plane with blue */

    /* ---- Initializes the VDC2 module ---- */
    vdc2_initial();

    /* ==== Updates the graphics image data ==== */
    while(1){
        delay();

        /* ---- Switches the buffers ---- */
        idx ^= 1;
        change_graphic(idx);
    }
}
```

3.4 Listings of Sample Program "VDC2 initialization"

```
114   *""FUNC COMMENT""*****************************************************************
115    * ID          :
116    * Outline     : VDC2 initialization
117    *-------------------------------------------------------------------------------
118    * Include     :
119    *-------------------------------------------------------------------------------
120    * Declaration : void vdc2_initial(void);
121    *-------------------------------------------------------------------------------
122    * Function    : Initializes the VDC2 for displaying. Layer 4 is used.
123    *             : TFT-LCD panel TX09D55VM1CDA (Hitachi Displays) is used in this
124    *             : application.
125    *-------------------------------------------------------------------------------
126    * Argument    : void
127    *-------------------------------------------------------------------------------
128    * Return Value: void
129    *""FUNC COMMENT END""*************************************************************/
130   void vdc2_initial(void)
131   {
132       CPG.VDC2CLKCR.BIT._CKSEL = 0;   /* Clock divider 1/1 */
133       vdc2_port_set();            /* I/O pin setting */
134       vdc2_display_control_initial(); /* Display control block setting */
135       vdc2_graphic_layer4_initial();  /* Layer 4 setting */
136   }
```

3.5 Listings of Sample Program "I/O pin settings"

```
/*""FUNC COMMENT""*****************************************************************
 * ID          :
 * Outline     : I/O pin settings
 *-----------------------------------------------------------------------------
 * Include     :
 *-----------------------------------------------------------------------------
 * Declaration : void vdc2_port_set(void);
 *-----------------------------------------------------------------------------
 * Function    : Sets I/O pins for the VDC2.
 *-----------------------------------------------------------------------------
 * Argument    : void
 *-----------------------------------------------------------------------------
 * Return Value: void
 *""FUNC COMMENT END""*************************************************************/
void vdc2_port_set(void)
{
    /* ---- DR3, DR2, DR1, DR0, DG5, DG4, DG3, DG2 ---- */
    GPIO.PTSEL_G.BIT._PTSEL_G7=GPIO.PTSEL_G.BIT._PTSEL_G6=
    GPIO.PTSEL_G.BIT._PTSEL_G5=GPIO.PTSEL_G.BIT._PTSEL_G4=
    GPIO.PTSEL_G.BIT._PTSEL_G3=GPIO.PTSEL_G.BIT._PTSEL_G2=
    GPIO.PTSEL_G.BIT._PTSEL_G1=GPIO.PTSEL_G.BIT._PTSEL_G0=1;
    /* ---- DB3, DB2, DB1, DG1, DG0, DB5, DB4, ---- */
    GPIO.PTSEL_I.BIT._PTSEL_I7=GPIO.PTSEL_I.BIT._PTSEL_I6=
    GPIO.PTSEL_I.BIT._PTSEL_I5=GPIO.PTSEL_I.BIT._PTSEL_I4=
    GPIO.PTSEL_I.BIT._PTSEL_I3=GPIO.PTSEL_I.BIT._PTSEL_I2=
    GPIO.PTSEL_I.BIT._PTSEL_I1 = 1;
    /* ---- DB0, DCLKIN, DE_C/DE_H ---- */
    GPIO.PTSEL_K.BIT._PTSEL_K4=GPIO.PTSEL_K.BIT._PTSEL_K2=
    GPIO.PTSEL_K.BIT._PTSEL_K0=1;
    /* ---- DCLKOUT, DR4, DR5 ---- */
    GPIO.PTSEL_H.BIT._PTSEL_H2=GPIO.PTSEL_H.BIT._PTSEL_H1=
    GPIO.PTSEL_H.BIT._PTSEL_H0=1;
    GPIO.PTIO_H.BIT._PTIO_H2=GPIO.PTIO_H.BIT._PTIO_H1=
    GPIO.PTIO_H.BIT._PTIO_H0=0;
}
```

3.6 Listings of Sample Program "Display control block initialization"

```
/*""FUNC COMMENT""*****************************************************************
 * ID          :
 * Outline     : Display control block initialization
 *-----------------------------------------------------------------------------
 * Include     :
 *-----------------------------------------------------------------------------
 * Declaration : void vdc2_display_control_initial(void);
 *-----------------------------------------------------------------------------
 * Function    : Initializes the display control block.
 *-----------------------------------------------------------------------------
 * Argument    : void
 *-----------------------------------------------------------------------------
 * Return Value: void
 *""FUNC COMMENT END""*************************************************************/
void vdc2_display_control_initial(void)
{
    /* ---- Selects the sync signal and outputs DE_C ---- */
    VDC2.SGMODE.LONG = 0x00000030;
        /* bit5 (DE_SEL)=1 outputs DE_C                       */
        /* bit4 (DEC_MODE)=1 generates the DE signal in the graphics block */
        /* bit1 (SYNC_SEL)=0 uses the internal sync signal          */

    /* ---- Sync signal timing setting ---- */
    VDC2.SYNCNT.LONG = 0x00000000;
        /* RGB data output is synchronized with the rising edge of the clock     */
        /* DE_C output is synchronized with the rising edge of the clock without inversion  */
        /* HSYNC output is synchronized with the rising edge of the clock without inversion */
        /* VSYNC output is synchronized with the rising edge of the clock without inversion */

    /* ---- Specifies the size of the sync signal (including the blanking interval) ---- */
    /* Number of pixels including the horizontal blanking interval and number of lines
including

the vertical blanking interval */
    VDC2.SYNSIZE.BIT._SYN_WIDTH = TFT_TOTAL_CLOCK;
    VDC2.SYNSIZE.BIT._SYN_HEIGHT = TFT_TOTAL_LINE;

    /* ---- HSYNC pulse width ---- */
    VDC2.HSYNCTIM.BIT._HSYNC_START = TFT_HSYNC_START;
    VDC2.HSYNCTIM.BIT._HSYNC_END = TFT_HSYNC_END;

    /* ---- VSYNC pulse width ---- */
    VDC2.VSYNCTIM.BIT._VSYNC_START = TFT_VSYNC_START;
    VDC2.VSYNCTIM.BIT._VSYNC_END = TFT_VSYNC_END;

    /* ---- Clears the VSYNC interrupt status ---- */
    VDC2.SGINTCNT.LONG = 0x00000010;
    VDC2.SGMODE.BIT._WE = 1; /* Enables to transfer register values */
}
```

3.7 Listings of Sample Program "Graphics block 4 initialization"

```
/*""FUNC COMMENT""*****************************************************************
 * ID          :
 * Outline     : Graphics block 4 initialization
 *-----------------------------------------------------------------------------
 * Include     :
 *-----------------------------------------------------------------------------
 * Declaration : void vdc2_graphic_layer4_initial(void);
 *-----------------------------------------------------------------------------
 * Function    : Initializes graphics block 4.
 *-----------------------------------------------------------------------------
 * Argument    : void
 *-----------------------------------------------------------------------------
 * Return Value: void
 *""FUNC COMMENT END""*************************************************************/
void vdc2_graphic_layer4_initial(void)
{
    /* ---- Disables to display (lower layer) ---- */
    VDC2_GR4.GRCMEN.LONG = 0x00000002;
        /* bit31 (WE)=0 disables transfer to register             */
        /* bit1 (DEN)=1 enables to display graphics     */
        /* bit0 (VEN)=0 disables to display lower-layer graphics */

    /* ---- Bus endianness ---- */
    VDC2_GR4.GRCBUSCNT.BIT._ENDIAN = 0; /* Little endian */

    /* ---- Setting for reading images from external memory ---- */
    VDC2_GR4.GROPSADR = (unsigned int *)frame_buffer[0];

    /* ---- Line offset setting ---- */
    VDC2_GR4.GROPSOFST = GRAPHICS4_LINE_OFFSET * sizeof(short);

    /* ---- Sets the output image area (LCD panel size) ---- */
    /* Width and height of the graphics image area */
    VDC2_GR4.GROPSWH.BIT._GROPSH = GRAPHICS4_Y_SIZE;
    VDC2_GR4.GROPSWH.BIT._GROPSW = GRAPHICS4_X_SIZE;

    /* ---- Vertical and horizontal display start positions of the image area ---- */
    VDC2_GR4.GROPDPHV.BIT._GROPDPV = TFT_DTMG_START_V - 1 + GRAPHICS4_POS_Y;
    VDC2_GR4.GROPDPHV.BIT._GROPDPH = TFT_DTMG_START_H - 16 + GRAPHICS4_POS_X;

    /* ---- Color for outside of the graphics image area ---- */
    VDC2_GR4.GROPBASERGB.LONG = GRAPHICS4_BG_COLOR;

    /* ---- Graphics output setting transfer ---- */
    VDC2_GR4.GRCMEN.BIT._WE = 1; /* Enables to transfer register values */
}
```

3.8 Listings of Sample Program "Update the graphics image data"

```
/*""FUNC COMMENT""*****************************************************************
 * ID          :
 * Outline     : Update the graphics image data
 *-------------------------------------------------------------------------------
 * Include     :
 *-------------------------------------------------------------------------------
 * Declaration : void change_graphic(void);
 *-------------------------------------------------------------------------------
 * Function    : Switches to another buffer specified by an argument to read the
 *             : graphics image data. Update the image data before executing this function.
 *             : Transfer the value by the GRCMEN4 register to enable the update.
 *-------------------------------------------------------------------------------
 * Argument    : int idex : Index number of the buffer to display
 *-------------------------------------------------------------------------------
 * Return Value: void
 *""FUNC COMMENT END""*************************************************************/
void change_graphic(int idx)
{
    /* ---- Updates the graphics image data area ---- */
    VDC2_GR4.GROPSADR = (unsigned int *)frame_buffer[idx];
    VDC2_GR4.GRCMEN.BIT._WE = 1; /* Enables to transfer the register value */
}
```

4. Documents for Reference

- Hardware Manual
  SH7764 Group Hardware Manual (REJ09B0360)
  The most up-to-date version of this document is available on the Renesas Technology Website.

- Software Manual (REJ09B0003)
  SH-4A Software Manual
  The most up-to-date version of this document is available on the Renesas Technology Website.

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