V_{GS} Transient Tolerance of Renesas GaN FETs

This document provides a guideline for allowable transient voltages between gate and source pins.

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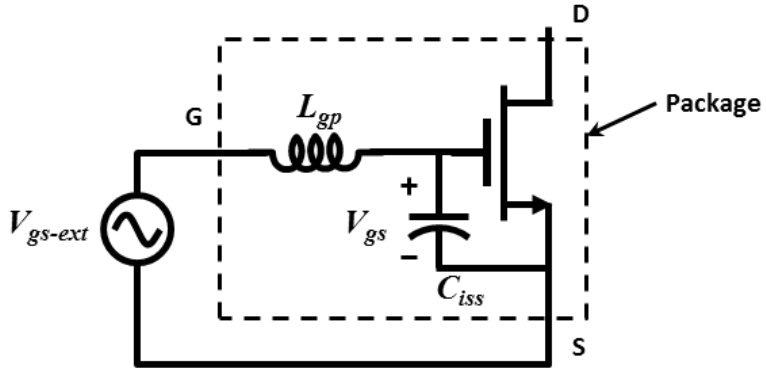
1. Introduction

The absolute maximum rating provided in Renesas data sheets for V_{GSS} is ±18V. This is the maximum voltage which the device is guaranteed to sustain between gate and source without failure. Because the package adds inductance in series with the gate; however, transient voltages may appear on the gate pin which exceed V_{GSS}, but cause no damage because the voltage actually present on the die does not exceed V_{GSS}. This Application Note provides a guideline for allowable transient voltages between gate and source pins.

2. Simple analysis

A very simple analysis of the input loop is shown in Figure 1. The package inductance in series with the gate, L_{GP}, has a value of about 3nH for the TO-220 package. From the data sheets, C_{iss} has a minimum value of 710pF. Using these values, the frequency at which $V_{GS}/V_{GS\text{-}EXT}$ = 0.5 is ~190MHz. Therefore, for frequencies above 200MHz, the amplitude of the actual internal voltage on V_{GS} is less than 50% of the voltage measured on the package pins. By this analysis, any ringing or transient voltage with a period of less than 5ns can have an amplitude as high as 36V without causing more than 18V on the internal gate.



$$\frac{Vgs}{Vgsext} \approx \frac{1}{\sqrt{1 + (2\pi f)^2 LgpCiss}}$$

Figure 1. Simple analysis of the input loop showing parasitic inductance internal to the transistor package

A more accurate analysis can be made, but requires an understanding of the origin of transient signals on the gate pin.

3. Origin of V_{GS} transients

In circuits with GaN power FETs, inductance in the input, or gate-drive loop is critical. Particularly important is the source inductance (L_{S2} in Figure 2, for example), which is common to both input and output loops. Any voltage developed across this inductance due to a change in the output current, di_D/dt, will appear in the input loop. A low impedance layout will minimize this inductance. However, the TO-220 package unavoidably adds inductance in the source lead, L_{SP2} as shown in Figure 2. This inductance cannot be further reduced.

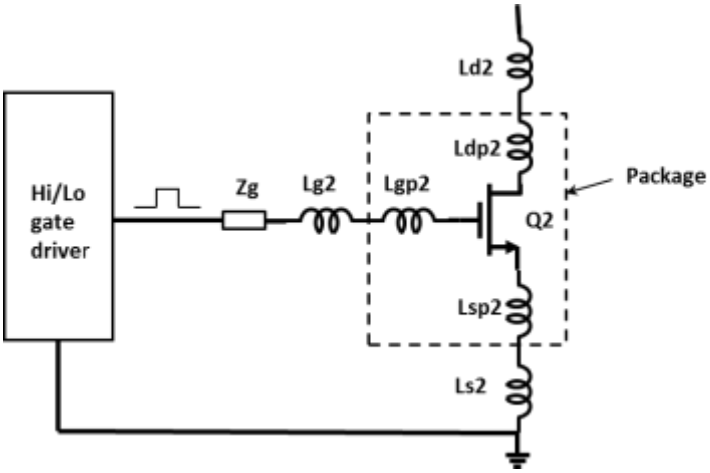
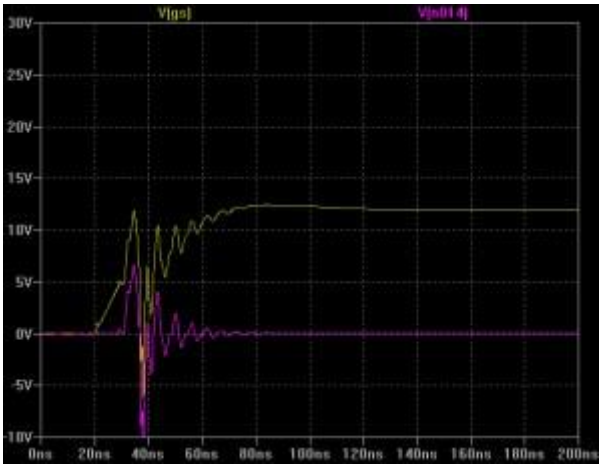


Figure 2. input loop showing parasitic inductances internal and external to the transistor package

Figure 3 shows simulated voltages on the internal source node and external gate pin, with respect to circuit ground. It is seen that high-frequency ringing on the gate pin is identical to the ringing voltage on the source inductance. The input capacitance, C_{ISS}, is sufficiently large that the actual gate-to-source voltage on the FET die is relatively unchanged by this signal. Figure 4 compares the external V_{GS} waveform to this actual internal gate-to-source voltage. The ringing on the gate pin has a frequency of about 150MHz, similar to the frequency found in the previous simple analysis. In this more realistic case; however, the internal gate voltage is much less than 50% of the external gate voltage, so the guideline given is seen to be quite conservative.



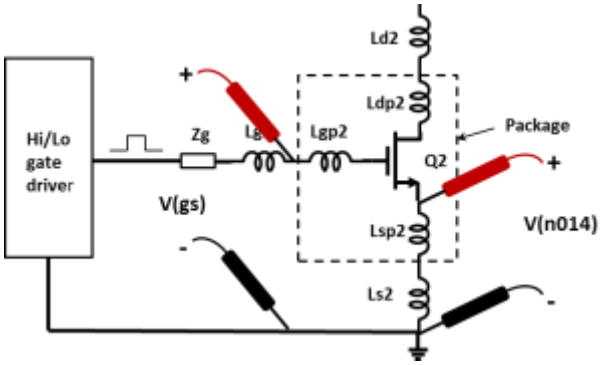


Figure 3. Simulation showing voltage on the internal source node

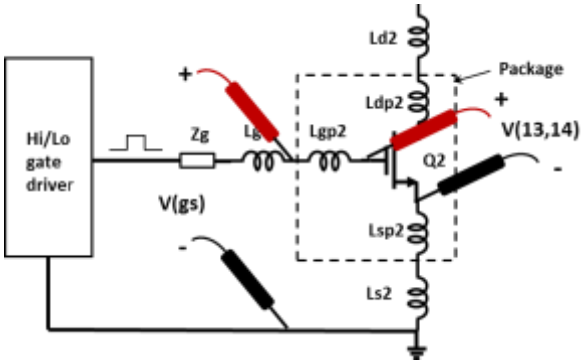


Figure 4. Simulation showing voltage on the internal gate node

4. Packages with internal ferrite beads

GaN FETs in the TO-247 package, such as the TPH3205WSB and TPH3207WS, have an internal ferrite bead in series with the gate. The impedance of the bead adds to L_{GP} in the simple analysis of Figure 1 and further attenuates transients of external origin.

The externally measured typical V_{GS} waveform is markedly different for these devices, as seen in Figure 5.

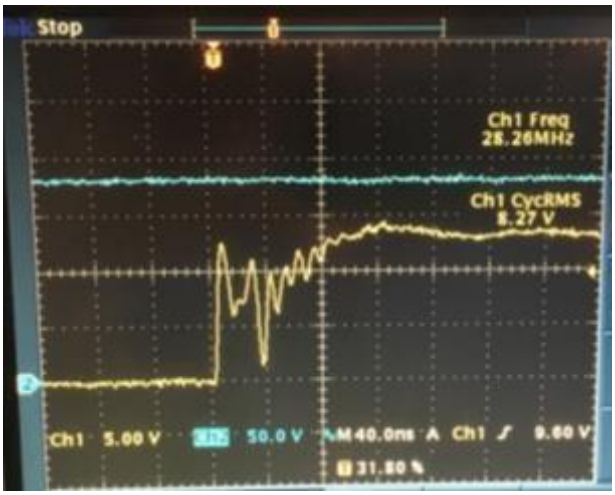
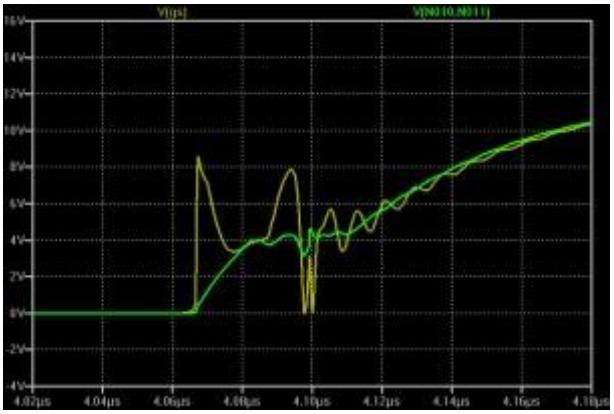


Figure 5. Externally measured V_{GS} waveform for a TPH3205WSB

The voltage which is actually present internally between the gate and source is similar to the previous case, as seen in the simulation of Figure 6.



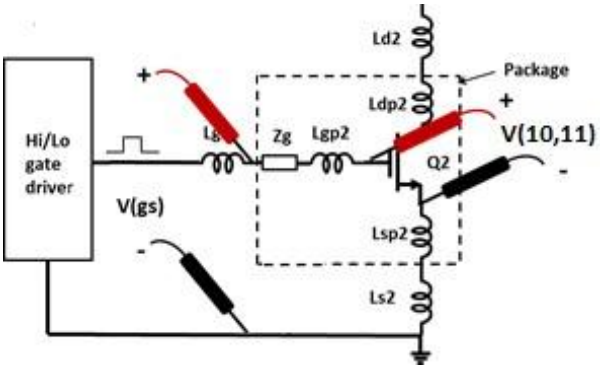


Figure 6. Simulation showing voltage on the internal gate node of a TO-247 with internal ferrite bead

5. Avoiding problems through careful PCB layout

The parasitic inductances of the input (gate) and output (drain) loops contribute significantly to overshoot, ringing, and stability in general. Renesas Application Notes AN0003: Printed Circuit Board Layout and Probing for GaN Power Switches and AN0004: Designing Hard-switched Bridges with GaN provide analysis and recommendations for designs that minimize PCB inductance and associated problems.