VersaClock 3S – 32.768kHz Output Configuration and Performance

Introduction

VersaClock 3S (VC3S) is programmable clock generator that is designed for low-power, consumer, and high-performance PCI Express applications. VersaClock 3S features a built-in Extreme Low-Power DCO and supports a low-power operation 32.768kHz RTC clock with only a coin cell battery supply. With less than 2µA low-power DCO operation mode, it supports applications with up to a few years clock source for date/time keeping circuit (RTC).

When the main power VDD33 is greater than 2.5V, the VC3S device will switch the DCO power source to main power to save battery power.

VC3S also supports a 32.786kHz output with a full-power divider mode, providing an option of better cycle-to-cycle jitter performance. The register bit 0x2A[3] switches on the low-power DCO Mode or full-power divider mode.

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1. Two Different Modes for Achieving 32k

Figure 1 shows a typical block diagram as displayed in the VC3S 5P35023 Datasheet. The 32.768kHz clock is supported for all SE1 – SE3.

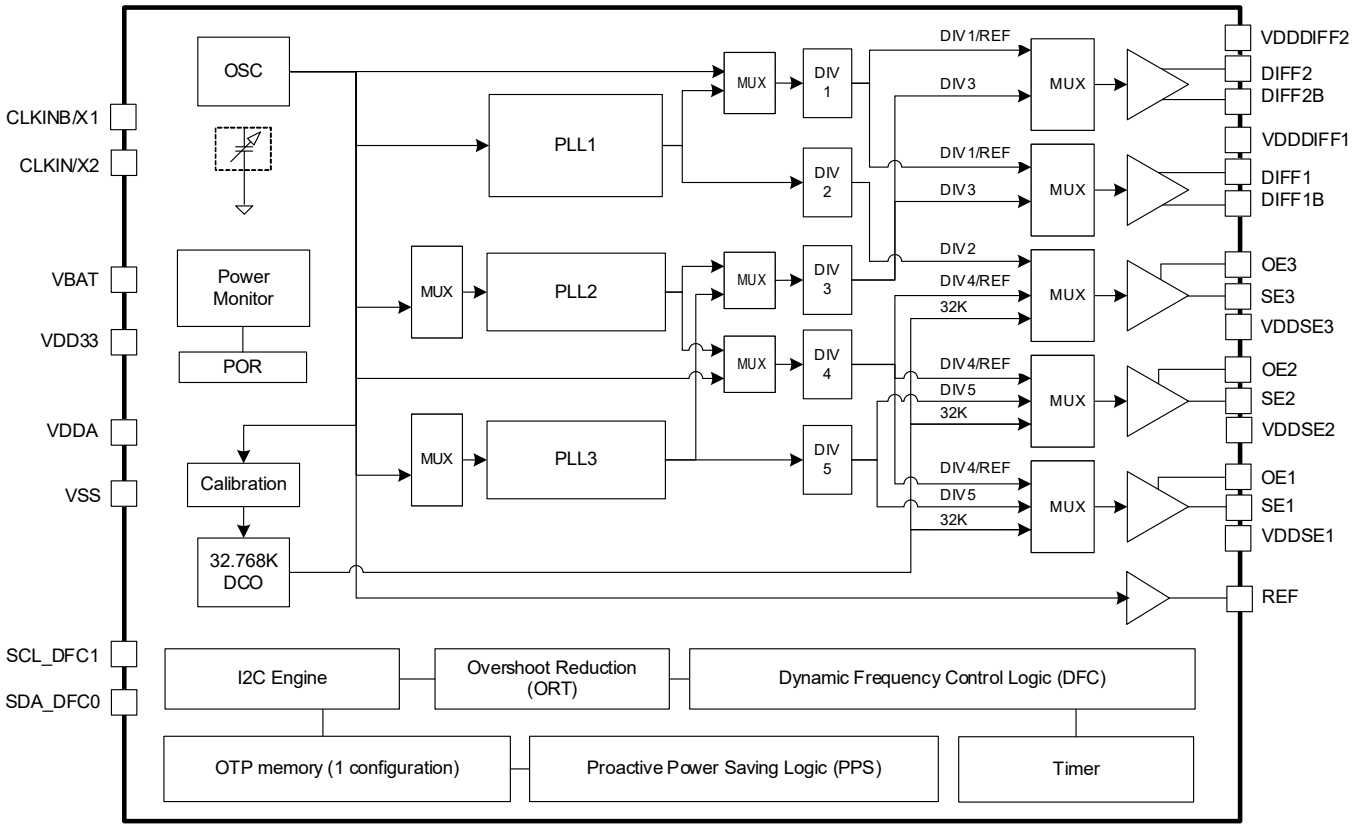

Figure 1. VersaClock 3S (5P35023) Block Diagram

When register 0x24[4] = 0, SE1 outputs a free-running frequency of 32.768kHz. When this bitset is 0x24[4] = 1, the frequency is controlled by SE1_CLKSEL. Register 0x1F[7] = 0 is to select output SE2 running at 32.768kHz. Register 0x21[7] = 0 is for output SE3 running at 32.768kHz.

0x2A[3] is a full-power direct divider switch bit and selects either to use low-power DCO Mode or full-power divider mode to generate 32.768kHz for SE1 – SE3.

For other VC3S parts, different settings are required to select the different modes (see Table 1).

Table 1. 32k Mode Selection

VC3S Device	Low Power DCO Mode	Full Power Divider Mode
5L35021B/5L35023B	0x2A[3] = 0	0x2A[3] = 1
5P35021B/5P35023B	0x2A[3] = 1	0x2A[3] = 0

2. DCO Mode

DCO mode is low-power consumption. The 32kHz clock only consumes less than 2µA current for the system's RTC reference clock. The system could save power when the device goes into power-down or sleep mode.

V_{BAT} is the power supply for low-power DCO mode and is typically connected to a 3.0V–3.3V coin cell battery. V_{DDSEx} (for non-32k outputs) should be off when VDDAs/VDDs turns off; V_{BAT} mode only supports 32.768kHz for SE1 – SE3. OE1 controls chip global power-down (PD#) except when 32.768kHz is enabled on SE1. When the PD# pin is active low, the chip goes to the lowest power-down mode and all outputs are disabled, with the exception of the 32kHz output (only keep 32k/Xtal calibration).

When using DCO mode, the external reference input should be in the range of 12MHz – 38MHz.

When the input frequency is out of the range, 32.768kHz needs to be acquired through divider mode.

Example: For 5P35021B/5P35023B, 0x2A[3] = 1, select DCO mode (see Figure 2).

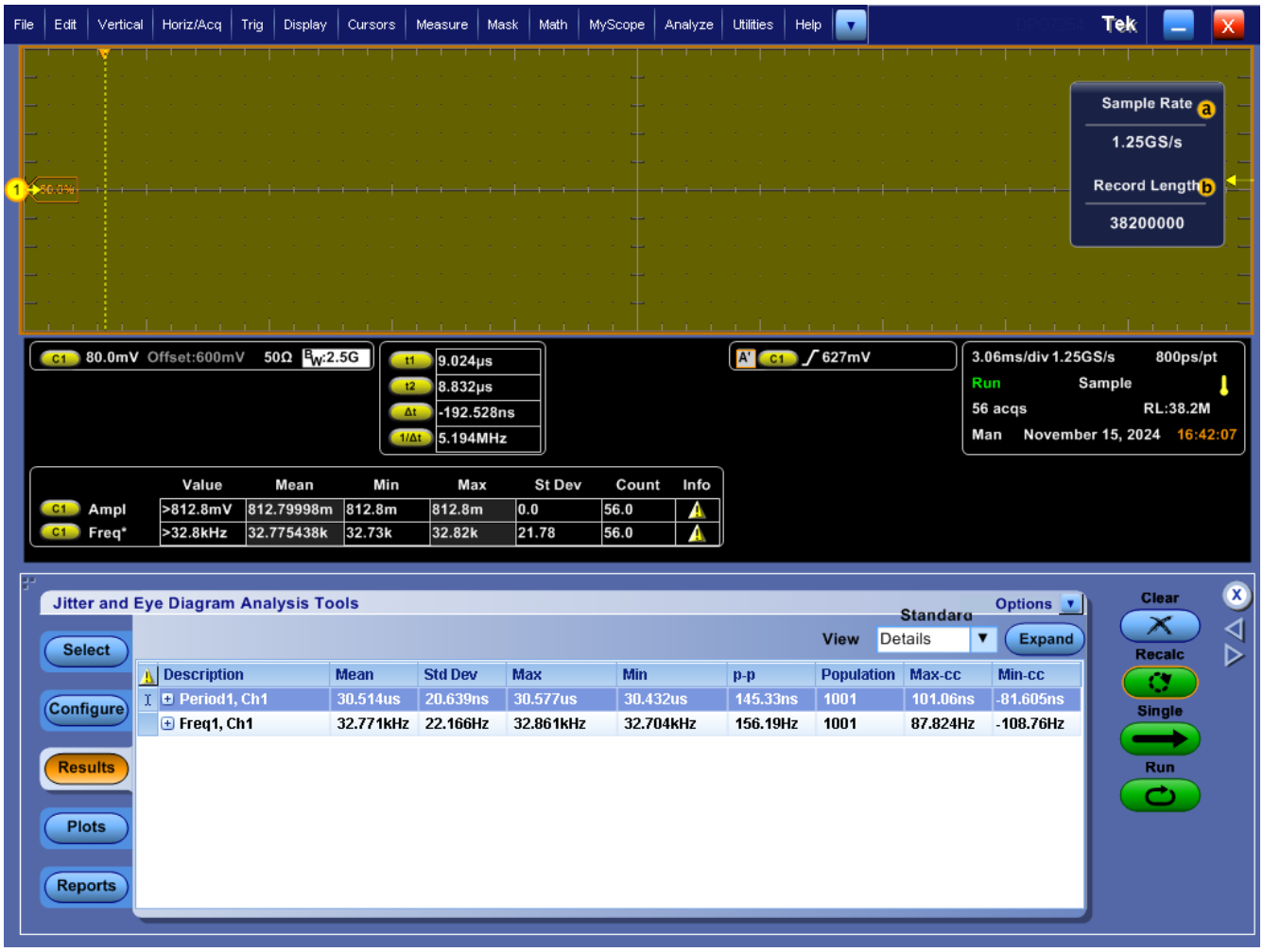

Figure 2. 32.768kHz with Low-Power DCO Mode

3. Full-Power Divider Mode – Divide from Reference Input

32kHz can also be divided from a reference input under full-power divider mode using the following equations.

$$32k\ Divider = 32k\ Integer\ Divider + \frac{32k\ Fractional\ Divider}{2^{10}}$$

$$32.768kHz = \frac{Reference\ Input\ Frequency}{32k\ Divider/2}$$

The integer divider and fractional divider are both limited to 10 bits, thus the maximum 32k divider is 2^10+2^10/2^10 = 1025. The total divider value needs to fit in the 10 bits integer divider and the 10 bits fractional divider when using full-power divider mode.

3.1 Registers

32k integer divider – 10 bits total

0x26[7:6]: 32k div int [9:8]

0x25[7:0]: 32k div int [7:0]

32k fractional divider – 10 bits total

0x26[1:0]: 32k div frac [9:8]

0x27[7:0]: 32k div frac [7:0]

3.2 Using 32k Integer Divider and Fractional Divider

Example: For 5P35021B/5P35023B, 0x2A[3] = 1, select Divider mode (see Figure 3).

With a 25MHz reference input:

- The integer divider value is 381. 0x25 = 0x7D, 0x26[9:8] = 0x01
- Fractional divider value is 481. 0x26[1:0] = 0x01, 0x27 = 0xE1

Total divider value is 381 + 481/2^10 = 381.4697266.

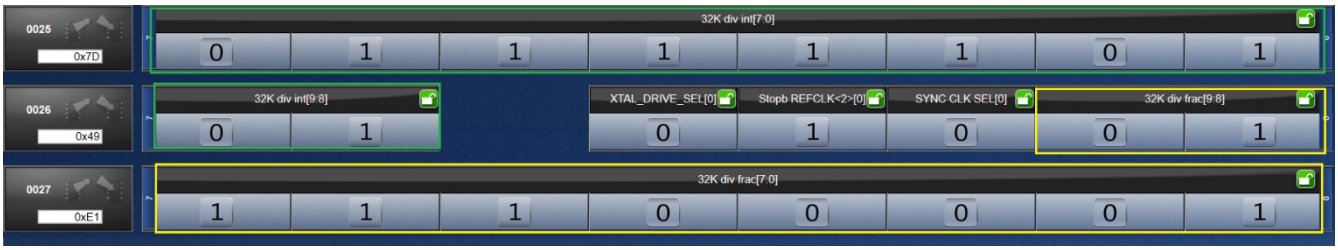

Figure 3. 25MHz Reference Input Divider Mode Register Setting from Timing Commander

Cycle-to-cycle jitter is 80.5ns (see Figure 4)

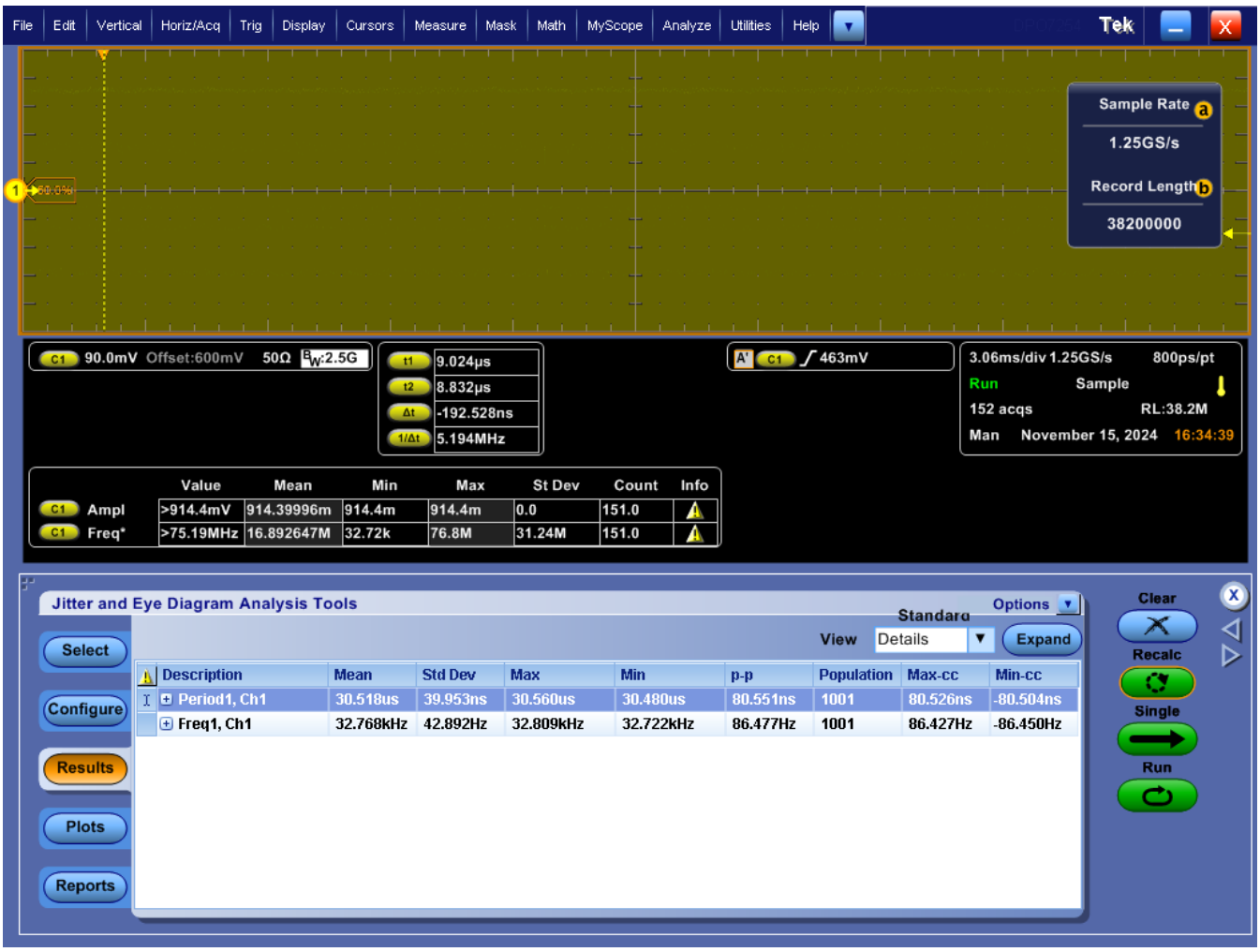

Figure 4. 32k Divider Mode with 25MHz Input Reference

3.3 Using 32k Integer Divider Only

To further improve the cycle-to-cycle jitter performance, use only an integer divider rather than both an integer divider and a fractional divider.

To achieve 32.768kHz with only the integer divider, consider using a 24.576MHz reference input.

With a 24.576MHz reference input:

- The integer divider value is 375. 0x26[9:8] = 0x01, 0x25 = 0x77
- Fractional divider value is 0. 0x26[1:0] = 0x00, 0x27 = 0x00

Total divider value is 375 (see Figure 5).

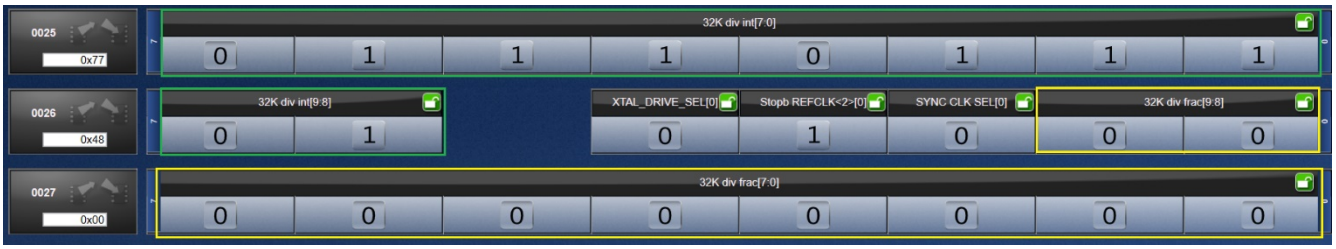

Figure 5. 24.576MHz Reference Input Divider Mode Register Setting from Timing Commander

Cycle-to-cycle jitter is 732.7ps (see Figure 6).

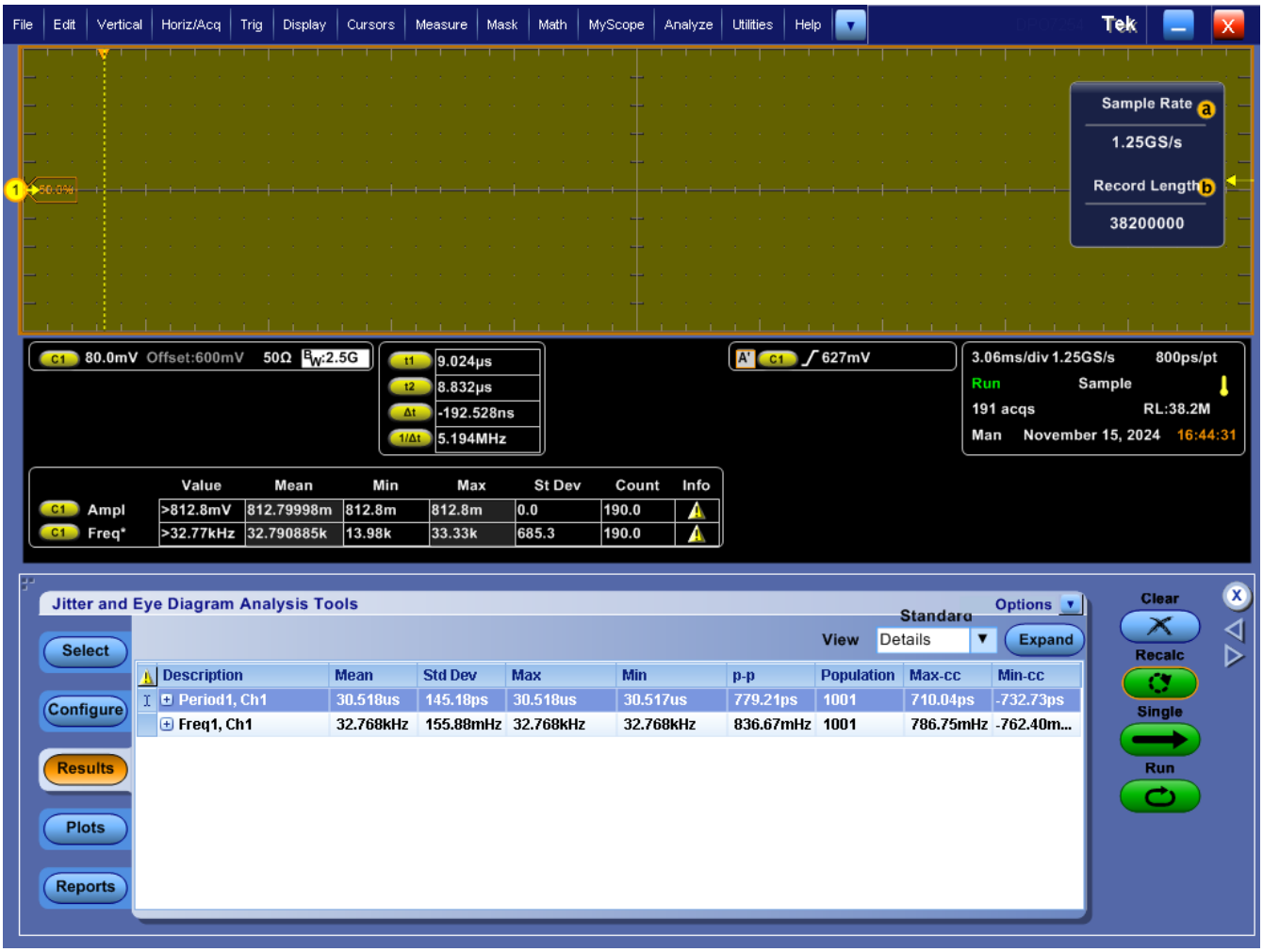

Figure 6. 32k Divider Mode with 24.576MHz Input Reference

4. Revision History

Revision	Date	Description
1.00	Dec 19, 2024	Initial release.

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