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M16C/64 Group

Variable-period variable-duty PWM output

1. Abstract

In this process, Timer A0 and Timer A1 are used to generate variable-period, variable-duty PWM output. Use the following peripheral function:

- Timer mode of timer A
- One-shot timer mode of timer A

2. Introduction

This application note is applied to the M16C/64 group microcomputers.

This program can be operated under the condition of M16C family products with the same SFR (Special Function Register) as M16C/64 Group products. Because some functions may be modified of the M16C family products, see the user's manual. When using the functions shown in this application note, evaluate them carefully for an operation.

3. Specification

(1) Set timer A0 in timer mode, and set timer A1 in one-shot timer mode with pulse-output function.

(2) Set 1 ms, the PWM period, to timer A0. Set 500 µs, the width of PWM "H" pulse, to timer A1. Both timer A0 and timer A1 use f_{1TIMAB} for the count source.

(3) Connect a 16-MHz oscillator to X_{IN}.

(4) Using POFSi bit in TAPOFS register, the output polarity of the TAi_{OUT} pin is not inverted (the TAi bit is set to 0 (stop counting)), the pin outputs "L". (i = 0, 1)

4. Operation

(1) Setting the count start flag to "1" causes the counter of timer A0 to begin counting. The counter of timer A0 performs a down count on count source f_{1TIMAB}.

(2) If the counter of timer A0 underflows, the counter reloads the content of the reload register and continues counting. At this time, the timer A0 interrupt request bit goes to "1".

(3) An underflow in timer A0 triggers the counter of timer A1 and causes it to begin counting. When the counter of timer A1 begins counting, the output level of the $TA1_{OUT}$ pin goes to "H".

(4) As soon as the count of the counter of timer A1 becomes "0000h", the output level of $TA1_{OUT}$ pin goes to "L", and the counter reloads the content of the reload register and stops counting. At the same time, the timer A1 interrupt request bit goes to "1".

Figure 1 shows the operation timing.

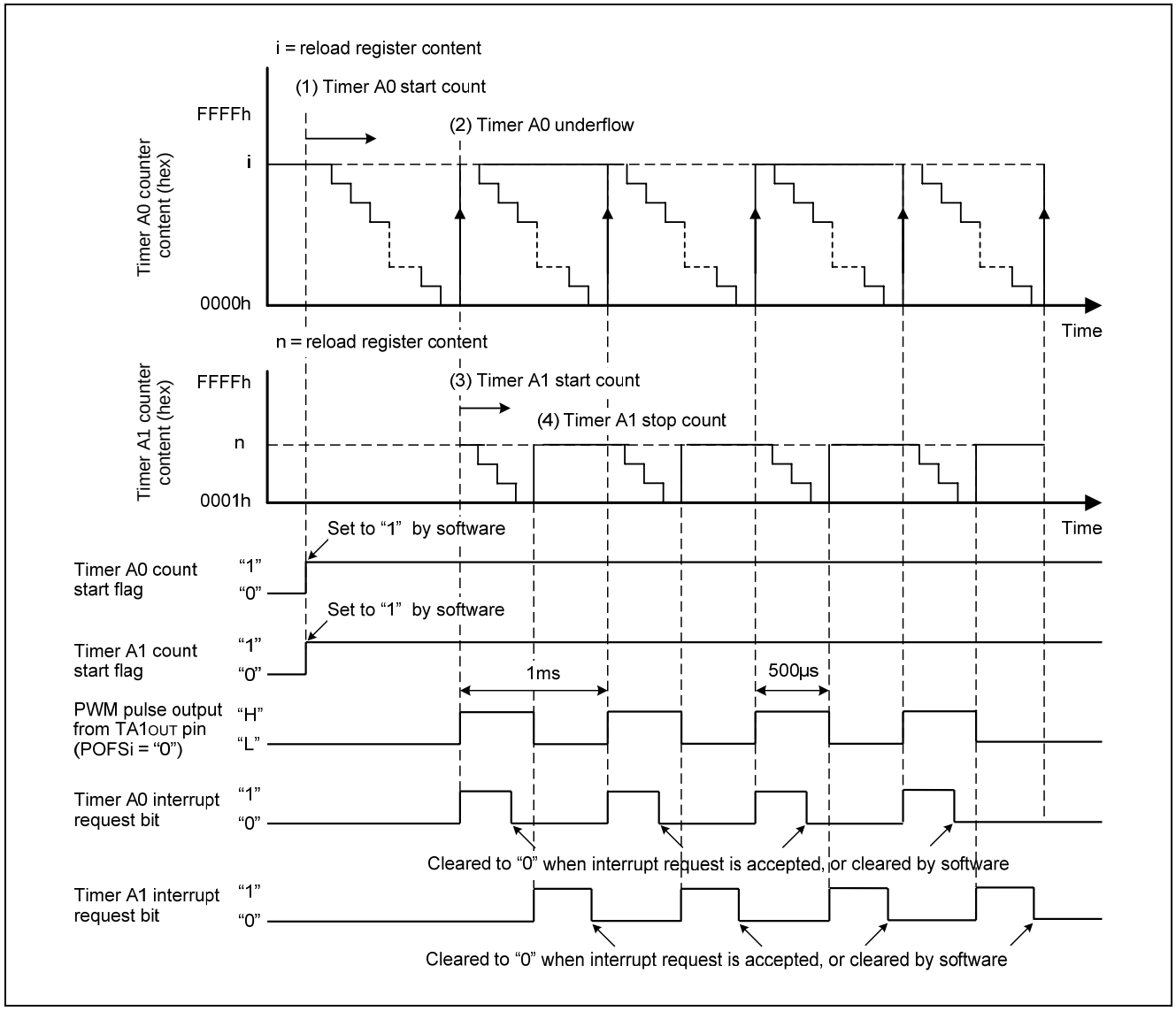


Figure 1. Operation timing of variable-period variable-duty PWM output

Figure 2 shows the connection diagram.

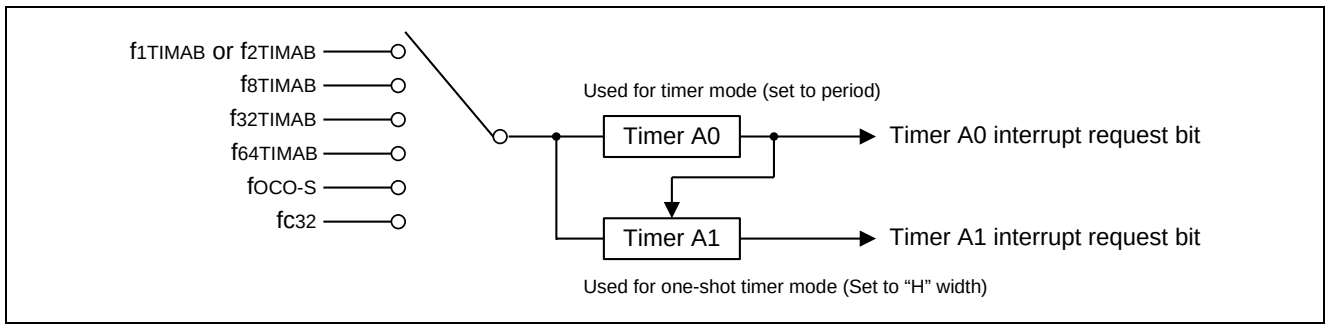


Figure 2. Connection diagram of variable-period variable-duty PWM output

5. Set-up procedure

Table 1 shows Timer A count source, Figure 3 shows block diagram of Timer A count source in timer mode.

Table 1. Count Source Selection of Timer A

TACSj register (Note 1)				TAiMR register		Count source	Count source period
TCS3/ TCS7	TCS2/ TCS6	TCS1/ TCS5	TCS0/ TCS4	TCK1	TCK0		f(PLL):24MHz f(XCIN):32.768kHz
0	-	-	-	0	0	f1TIMAB/f2TIMAB (Note 2)	41.7ns or 83.3ns
0	-	-	-	0	1	f8TIMAB	333.3ns
0	-	-	-	1	0	f32TIMAB	1333.3ns
0	-	-	-	1	1	fc32	976.56µs
1	0	0	0	-	-	f1TIMAB/f2TIMAB (Note 2)	41.7ns or 83.3ns
1	0	0	1	-	-	f8TIMAB	333.3ns
1	0	1	0	-	-	f32TIMAB	1333.3ns
1	0	1	1	-	-	f64TIMAB	2666.7ns
1	1	0	1	-	-	foco-s	About 8µs
1	1	1	0	-	-	fc32	976.56µs

Note 1: TCS3~TCS0 bits of TACS0 register correspond to Timer A0 count source selection, TCS7~TCS4 bits of TACS0 register correspond to Timer A1 count source selection, TCS3~TCS0 bits of TACS1 register correspond to Timer A2 count source selection, TCS7~TCS4 bits of TACS1 register correspond to Timer A3 count source selection, and TCS3~TCS0 bits of TACS2 register correspond to Timer A4 count source selection.
Note 2: When the PCLK0 bit in the PCLKR register is "1", the selected clock source is f1TIMAB. When the PCLK0 bit is "0", the selected clock source is f2TIMAB.

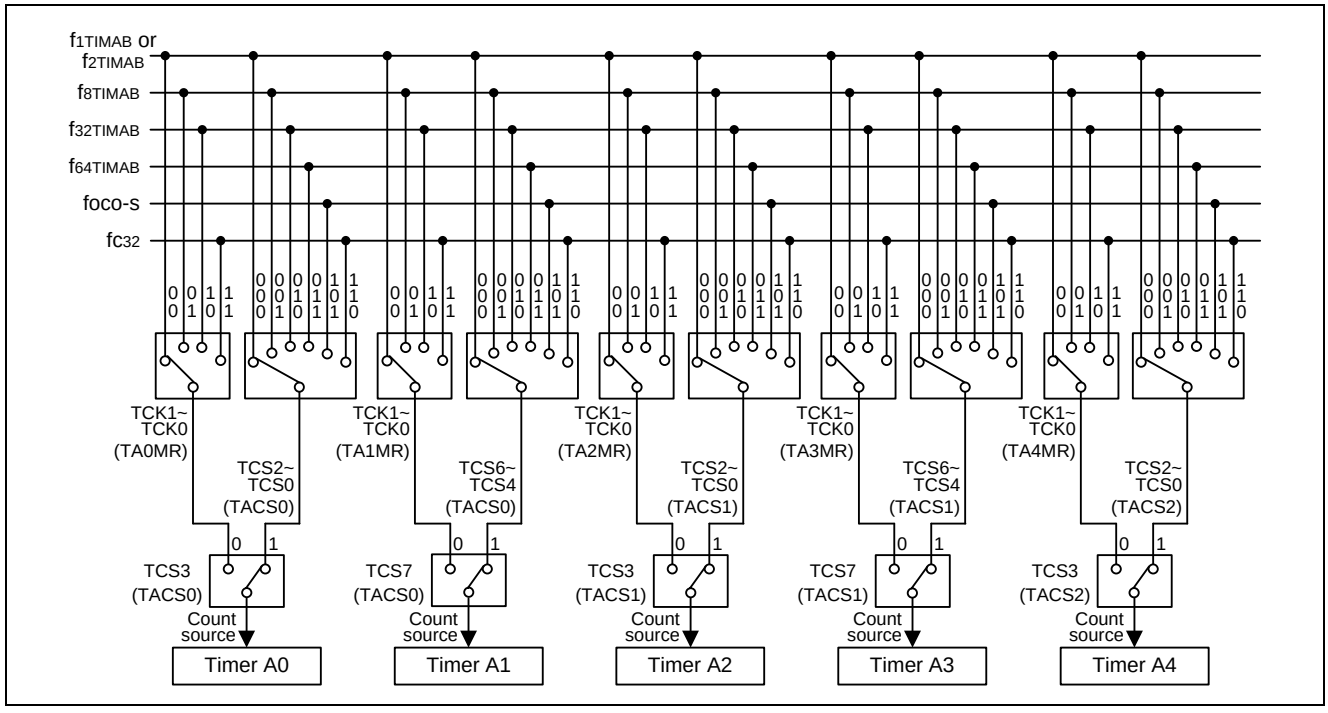
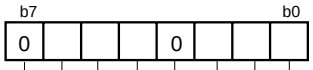


Figure 3. Count source of Timer A

Selecting timer count source



Timer A count source select register 0 [Address 01D0h] TACS0

TA0 count source select bit (Note1)
b2 b1 b0
0 0 0 : f_{1TIMAB} or f_{2TIMAB} (Note2)
0 0 1 : f_{8TIMAB}
0 1 0 : $f_{32TIMAB}$
0 1 1 : $f_{64TIMSB}$
1 0 0 : Do not set
1 0 1 : foco-s
1 1 0 : f_{C32}
1 1 1 : Do not set

TA0 count source option specified bit (Note1)
0 : TCK0, TCK1 enabled, TCS0 to TCS2 disabled

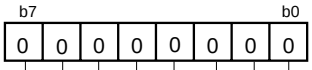
TA1 count source select bit (Note1)
b2 b1 b0
0 0 0 : f_{1TIMAB} or f_{2TIMAB} (Note2)
0 0 1 : f_{8TIMAB}
0 1 0 : $f_{32TIMAB}$
0 1 1 : $f_{64TIMSB}$
1 0 0 : Do not set
1 0 1 : foco-s
1 1 0 : f_{C32}
1 1 1 : Do not set

TA1 count source option specified bit (Note1)
0 : TCK0, TCK1 enabled, TCS4 to TCS6 disabled

Note 1: About the count source period, please refer to Table 2.
Note 2: When the PCLK0 bit in the PCLKR register is “1”, the selected clock source is f_{1TIMAB}. When the PCLK0 bit is “0”, the selected clock source is f_{2TIMAB}.

Setting timer A0

Selecting timer mode and functions



Timer A0 mode register [Address 0336h]
TA0MR

Selection of timer mode

Pulse output function select bit
0 : Pulse is not output ($TA0_{OUT}$ pin is normal port pin)

Gate function select bit
b4 b3
0 0 :Gate function not available ($TA0_{IN}$ pin is a normal port pin)

0 (Must always be “0” in timer mode)

Count source select bit (Note1)
b7 b6
0 0 : f_{1TIMAB} or f_{2TIMAB} (Note2)
0 1 : f_{8TIMAB}
1 0 : $f_{32TIMAB}$
1 1 : f_{C32}

Note 1: Valid when the TCS3 bit or TCS7 bit in registers TACS0 to TACS2 is set to 0 (TCK0, TCK1 enabled). About the count source period, please refer to Table 2.
Note 2: When the PCLK0 bit in the PCLKR register is “1”, the selected clock source is f_{1TIMAB}. When the PCLK0 bit is “0”, the selected clock source is f_{2TIMAB}.

Setting counter value

(b15) b7 (b8) b0 b7 b0

3Eh	7Fh

Timer A0 register [Address 0327h, 0326h]
TA0

Setting timer A1

Selecting one-shot timer mode and functions

b7 b0

0	0	0	1	0	1	1	0

Timer A1 mode register [Address 0337h]
TA1MR

Selection of one-shot timer mode

Pulse output function select bit
1 : Pulse is output (TA1OUT pin is pulse output pin)

External trigger select bit
Invalid when choosing timer's overflow

Trigger select bit
1 : Selected by event/trigger select register

0 (Must always be "0" in one-shot timer mode)

Count source select bit (Note1)
b7 b6
0 0 : f1TIMAB or f2TIMAB (Note2)
0 1 : f8TIMAB
1 0 : f32TIMAB
1 1 : fc32

Note 1: Valid when the TCS3 bit or TCS7 bit in registers TACS0 to TACS2 is set to 0 (TCK0, TCK1 enabled). About the count source period, please refer to Table 2.
Note 2: When the PCLK0 bit in the PCLKR register is "1", the selected clock source is f1TIMAB. When the PCLK0 bit is "0", the selected clock source is f2TIMAB.

Setting event/trigger select bit
(Set timer A0 to trigger timer A1)

b7 b0

						1	0

Trigger select register [Address 0323h]
TRGSR

Timer A1 event/trigger select bit
b1 b0
1 0 : TA0 overflow or underflow is selected

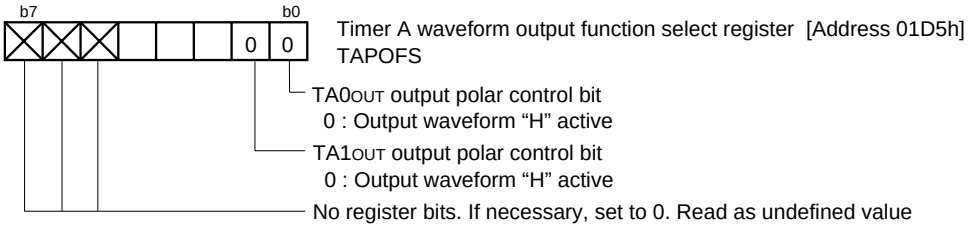
Setting one-shot timer's time

(b15) b7 (b8) b0 b7 b0

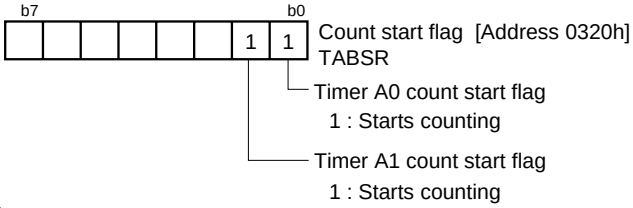
1Fh	40h

Timer A1 register [Address 0329h, 0328h]
TA1

Selecting waveform output function



Setting count start flag



Start counting

6. Reference

Hardware manual

M16C/64 Group Hardware Manual

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