To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

Send any inquiries to http://www.renesas.com/inquiry.

Notice

1. All information included in this document is current as of the date this document is issued. Such information, however, is subject to change without any prior notice. Before purchasing or using any Renesas Electronics products listed herein, please confirm the latest product information with a Renesas Electronics sales office. Also, please pay regular and careful attention to additional and different information to be disclosed by Renesas Electronics such as that disclosed through our website.
2. Renesas Electronics does not assume any liability for infringement of patents, copyrights, or other intellectual property rights of third parties by or arising from the use of Renesas Electronics products or technical information described in this document. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
3. You should not alter, modify, copy, or otherwise misappropriate any Renesas Electronics product, whether in whole or in part.
4. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation of these circuits, software, and information in the design of your equipment. Renesas Electronics assumes no responsibility for any losses incurred by you or third parties arising from the use of these circuits, software, or information.
5. When exporting the products or technology described in this document, you should comply with the applicable export control laws and regulations and follow the procedures required by such laws and regulations. You should not use Renesas Electronics products or the technology described in this document for any purpose relating to military applications or use by the military, including but not limited to the development of weapons of mass destruction. Renesas Electronics products and technology may not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations.
6. Renesas Electronics has used reasonable care in preparing the information included in this document, but Renesas Electronics does not warrant that such information is error free. Renesas Electronics assumes no liability whatsoever for any damages incurred by you resulting from errors in or omissions from the information included herein.
7. Renesas Electronics products are classified according to the following three quality grades: “Standard”, “High Quality”, and “Specific”. The recommended applications for each Renesas Electronics product depends on the product’s quality grade, as indicated below. You must check the quality grade of each Renesas Electronics product before using it in a particular application. You may not use any Renesas Electronics product for any application categorized as “Specific” without the prior written consent of Renesas Electronics. Further, you may not use any Renesas Electronics product for any application for which it is not intended without the prior written consent of Renesas Electronics. Renesas Electronics shall not be in any way liable for any damages or losses incurred by you or third parties arising from the use of any Renesas Electronics product for an application categorized as “Specific” or for which the product is not intended where you have failed to obtain the prior written consent of Renesas Electronics. The quality grade of each Renesas Electronics product is “Standard” unless otherwise expressly specified in a Renesas Electronics data sheets or data books, etc.

   “Standard”: Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; and industrial robots.

   “High Quality”: Transportation equipment (automobiles, trains, ships, etc.); traffic control systems; anti-disaster systems; anti-crime systems; safety equipment; and medical equipment not specifically designed for life support.

   “Specific”: Aircraft; aerospace equipment; submersible repeaters; nuclear reactor control systems; medical equipment or systems for life support (e.g. artificial life support devices or systems), surgical implantations, or healthcare intervention (e.g. excision, etc.), and any other applications or purposes that pose a direct threat to human life.
8. You should use the Renesas Electronics products described in this document within the range specified by Renesas Electronics, especially with respect to the maximum rating, operating supply voltage range, movement power voltage range, heat radiation characteristics, installation and other product characteristics. Renesas Electronics shall have no liability for malfunctions or damages arising out of the use of Renesas Electronics products beyond such specified ranges.
9. Although Renesas Electronics endeavors to improve the quality and reliability of its products, semiconductor products have specific characteristics such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Further, Renesas Electronics products are not subject to radiation resistance design. Please be sure to implement safety measures to guard them against the possibility of physical injury, and injury or damage caused by fire in the event of the failure of a Renesas Electronics product, such as safety design for hardware and software including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult, please evaluate the safety of the final products or system manufactured by you.
10. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. Please use Renesas Electronics products in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. Renesas Electronics assumes no liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
11. This document may not be reproduced or duplicated, in any form, in whole or in part, without prior written consent of Renesas Electronics.
12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products, or if you have any other inquiries.

(Note 1) “Renesas Electronics” as used in this document means Renesas Electronics Corporation and also includes its majority-owned subsidiaries.

(Note 2) “Renesas Electronics product(s)” means any product developed or manufactured by or for Renesas Electronics.

Preliminary Application Note

V850E/MS1™

32-/16-Bit Single-Chip Microcontrollers

Hardware

μPD703100
μPD703101
μPD703102
μPD70F3102

Document No. U14214EJ1V0ANJ1 (1st edition)
Date Published August 2000 N CP(K)

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

The export of these products from Japan is regulated by the Japanese government. The export of some or all of these products may be prohibited without governmental license. To export or re-export some or all of these products from a country other than Japan may also be prohibited without a license from that country. Please call an NEC sales representative.

- **The information contained in this document is being issued in advance of the production cycle for the device. The parameters for the device may change before final production or NEC Corporation, at its own discretion, may withdraw the device prior to its production.**
- No part of this document may be copied or reproduced in any form or by any means without the prior written consent of NEC Corporation. NEC Corporation assumes no responsibility for any errors which may appear in this document.
- NEC Corporation does not assume any liability for infringement of patents, copyrights or other intellectual property rights of third parties by or arising from use of a device described herein or any other liability arising from use of such device. No license, either express, implied or otherwise, is granted under any patents, copyrights or other intellectual property rights of NEC Corporation or others.
- Descriptions of circuits, software, and other related information in this document are provided for illustrative purposes in semiconductor product operation and application examples. The incorporation of these circuits, software, and information in the design of the customer's equipment shall be done under the full responsibility of the customer. NEC Corporation assumes no responsibility for any losses incurred by the customer or third parties arising from the use of these circuits, software, and information.
- While NEC Corporation has been making continuous effort to enhance the reliability of its semiconductor devices, the possibility of defects cannot be eliminated entirely. To minimize risks of damage or injury to persons or property arising from a defect in an NEC semiconductor device, customers must incorporate sufficient safety measures in its design, such as redundancy, fire-containment, and anti-failure features.
- NEC devices are classified into the following three quality grades:
  "Standard", "Special", and "Specific". The Specific quality grade applies only to devices developed based on a customer designated "quality assurance program" for a specific application. The recommended applications of a device depend on its quality grade, as indicated below. Customers must check the quality grade of each device before using it in a particular application.
  - Standard: Computers, office equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment and industrial robots
  - Special: Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)
  - Specific: Aircraft, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems or medical equipment for life support, etc.

  The quality grade of NEC devices is "Standard" unless otherwise specified in NEC's Data Sheets or Data Books. If customers intend to use NEC devices for applications other than those specified for Standard quality grade, they should contact an NEC sales representative in advance.

M5 98. 8

Regional Information

Some information contained in this document may vary from country to country. Before using any NEC product in your application, please contact the NEC office in your country to obtain a list of authorized representatives and distributors. They will verify:

- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

In addition, trademarks, registered trademarks, export restrictions, and other legal issues may also vary from country to country.

NEC Electronics Inc. (U.S.)
Santa Clara, California
Tel: 408-588-6000
800-366-9782
Fax: 408-588-6130
800-729-9288

NEC Electronics (Germany) GmbH
Duesseldorf, Germany
Tel: 0211-65 03 02
Fax: 0211-65 03 490

NEC Electronics (UK) Ltd.
Milton Keynes, UK
Tel: 01908-691-133
Fax: 01908-670-290

NEC Electronics Italiana s.r.l.
Milano, Italy
Tel: 02-66 75 41
Fax: 02-66 75 42 99

NEC Electronics (Germany) GmbH
Benelux Office
Eindhoven, The Netherlands
Tel: 040-2445845
Fax: 040-2444580

NEC Electronics (France) S.A.
Velizy-Villacoublay, France
Tel: 01-30-67 58 00
Fax: 01-30-67 58 99

NEC Electronics (France) S.A.
Madrid Office
Madrid, Spain
Tel: 91-504-2787
Fax: 91-504-2860

NEC Electronics (Germany) GmbH
Scandinavia Office
Taeby, Sweden
Tel: 08-63 80 820
Fax: 08-63 80 388

NEC Electronics Hong Kong Ltd.
Hong Kong
Tel: 2886-9318
Fax: 2886-9022/9044

NEC Electronics Hong Kong Ltd.
Seoul Branch
Seoul, Korea
Tel: 02-528-0303
Fax: 02-528-4411

NEC Electronics Singapore Pte. Ltd.
United Square, Singapore
Tel: 65-253-8311
Fax: 65-250-3583

NEC Electronics Taiwan Ltd.
Taipei, Taiwan
Tel: 02-2719-2377
Fax: 02-2719-5951

NEC do Brasil S.A.
Electron Devices Division
Guarulhos-SP Brasil
Tel: 55-11-6462-6810
Fax: 55-11-6462-6829

J00.7

[MEMO]

INTRODUCTION

Target Readers

This manual is intended for users who wish to understand the function of the V850E/MS1 (μPD703100, 703101, 703102, 70F3102) and to design application systems using these microcontrollers.

Purpose

The purpose of these application notes is to help the user understand the composition of the V850E training board (TB-V850E), an example of a system that uses the V850E/MS1.

Organization

These application notes are broadly divided into the following sections.

- General description of V850E/MS1
- Bus interface-connected circuit examples - 1 (Connection examples of directly connectable memory devices)
  - SRAM-connected circuit
  - PROM-connected circuit
  - DRAM-connected circuit
- Bus interface-connected circuit examples - 2 (Connection examples of added circuits)
  - SRAM-connected circuit
  - PROM-connected circuit
  - SIMM-connected circuit
  - DIMM-connected circuit
  - I/O device-connected circuit
- Application examples

How to Use This Manual

In these application notes, it is assumed that the reader has general knowledge in the fields of electrical engineering, logic circuits, and microcontrollers.

For details of V850E/MS1 electrical characteristics
→ See the corresponding (separate) data sheet.

For details of V850E/MS1 hardware functions
→ See the corresponding (separate) **V850E/MS1 User's Manual Hardware**.

For details of V850E/MS1 instruction functions
→ See the **V850E/MS1 User's Manual Architecture**.

Conventions

Data significance:	Higher digits on the left and lower digits on the right.
Active low representation:	$\overline{xxx}$ (overscore over pin or signal name) or /xxx (slash "/" is entered before the signal name)
Memory map address:	Higher address on the top and lower address on the bottom
Note:	Footnote for item marked with **Note** in the text
Caution:	Information requiring particular attention
Remark:	Supplementary information

Numeral representation: Binary ... xxxx or xxxxB
Decimal ... xxxx
Hexadecimal ... xxxxH

Prefix indicating the power of 2 (address space, memory capacity)
K (Kilo): $2^{10} = 1024$
M (Mega): $2^{20} = 1024^2$
G (Giga): $2^{30} = 1024^3$

Related Documents

The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

○ Documents Related to Devices

Document Name	Document No.
μPD703100-33, 703100-40, 703101-33, 703102-33 Data Sheet	U13995E
μPD703100-A33, 703100-A40, 703101-A33, 703102-A33 Data Sheet	U14168E
μPD70F3102-33 Data Sheet	U13844E
μPD70F3102-A33 Data Sheet	U13845E
V850E/MS1 User's Manual Hardware	U12688E
V850E/MS1 User's Manual Architecture	U12197E
V850E/MS1 Application Notes Hardware	This manual

○ Documents Related to Development tools (User's Manuals)

Document Name		Document No.
IE-703102-MC (In-circuit Emulator)		U13875E
IE-703102-MC-EM1, IE-703102-MC-EM1-A (In-circuit Emulator Option Board)		U13876E
CA850 (C Compiler Package)	Operation (UNIX™ Based)	U12839E
	Operation (Windows™ Based)	U12827E
	C Language	U12840E
	Assembly Language	U10543E
	Project Manager (Windows Based)	U11991E
RX850 (Real-time OS)	Basics	U13430E
	Technical	U13431E
	Installation	U13410E
RX850 Pro (Real-time OS)	Basics	U13773E
	Technical	U13772E
	Installation	U13774E
ID850 (Ver. 1.31) (Integrated Debugger) Operation (Windows Based)		U13716E
RD850[Note] (Task Debugger) (Windows Based)		U11158E
RD850 (Ver. 3.0) (Task Debugger) (Windows Based)		U13737E
RD850 Pro (Ver. 3.0) (Task Debugger) (Windows Based)		U13916E
AZ850 (System Performance Analyzer) Operation		U11181E

Note Corresponds to ID850 (Ver. 1.32)

CONTENTS

LIST OF FIGURES (1/2)

LIST OF FIGURES (2/2)

LIST OF TABLES

OTHER

[MEMO]

CHAPTER 1 GENERAL DESCRIPTION OF V850E/MS1

The V850E/MS1 uses a "V850E" CPU core of NEC's V850 Family™, and it includes ROM, RAM, various memory controllers, DMA controllers, and peripheral functions such as a real-time pulse unit, serial interface, and an A/D converter. In addition, this 16-bit single-chip microcontroller has an internal 32-bit data bus and an external 16-bit data bus for high-capacity data processing and high-speed real-time control.

Memory devices such as PROMs, SRAMs, and DRAMs can be directly connected.

1.1 Features

○ Number of instructions	81
○ Minimum instruction execution time	25 ns (ROMless version: during internal 40-MHz operation) 30 ns (mask ROM version or flash memory version: during internal 33-MHz operation)
○ General-purpose registers	32 bits × 32 registers
○ Instruction set	Upwardly compatible with V850 CPU Signed multiplication (16 bits × 16 bits R 32 bits) or (32 bits × 32 bits → 64 bits): 1 or 2 clocks Saturated arithmetic instructions (overflow and underflow detection functions are included) 32-bit shift instruction: 1-clock cycle Bit manipulation instructions Load and store instructions with long/short format Signed load instruction
○ Memory space	32 Mbytes of linear address space (shared program/data) Chip select output function: 8 areas Memory block allocation function: 2, 4, or 8 Mbytes per block Programmable wait function Idle state insertion function
○ External bus interface	16-bit data bus (separate address/data bus) 16-/8-bit bus sizing function Bus hold function External wait function

○ Internal memory

Product Name	Internal ROM	Internal RAM
μPD703100	None	4 Kbytes
μPD703101	96 Kbytes (Mask ROM)	4 Kbytes
μPD703102	128 Kbytes (Mask ROM)	4 Kbytes
μPD70F3102	128 Kbytes (Flash memory)	4 Kbytes

○ Interrupts and exceptions

External interrupts: 25 (including NMIs)
Internal interrupts: 47 sources
Exceptions: 1 source
Eight programmable priority levels can be specified.

○ Memory access controllers

DRAM controller (for EDO DRAM, fast page DRAM)
Page ROM controller

○ DMA controllers

4-channel configuration
Transfer unit: 8 bits, 16 bits
Maximum number of transfers: 65536 (2^{16}) transfers
Transfer types: Fly-by (1 cycle) transfer, 2-cycle transfer
Transfer modes: Single transfer, single-step transfer, block transfer
DMA transfer termination (terminal count) output signal

○ I/O lines

Input ports: 9
I/O ports: 114

○ Real-time pulse unit

16-bit timer/event counter: 6 channels
16-bit timers: 6
16-bit capture/compare registers: 24
16-bit interval timer: 2 channels

○ Serial interface

Asynchronous serial interface (UART)
Clocked Serial Interface (CSI)
UART/CSI: 2 channels
CSI: 2 channels
Dedicated baud rate generator: 3 channels

○ A/D converter

10-bit resolution A/D converter: 8 channels

○ Clock generator	5 multiplication functions using PLL clock synthesizer 2 division functions using external clock
○ Power-saving functions	HALT/IDLE/Software STOP modes Clock output stop function
○ Package	144-pin plastic LQFP (fine pitch) (20 × 20 mm): Pin pitch = 0.5 mm 157-pin plastic FBGA (14 × 14 mm)
○ CMOS structure	All static circuits

[MEMO]

CHAPTER 2 BUS INTERFACE-CONNECTED CIRCUIT EXAMPLES - 1

This chapter describes the memory that can be connected directly to the V850E/MS1. The approach behind the configuration of these circuit examples is as follows.

<1> V850E/MS1's internal system clock speed is 33 MHz

Remark Wait settings and idle settings for speeds other than 33 MHz are described in **2.1.2 Wait/idle setting and system clock list for SRAM connection**.

<2> Programmable wait is used for wait control
($\overline{\text{WAIT}}$ signal is pulled up)

<3> External pins operate using +5-V power when HV_{DD} is connected to a +5-V power supply
External pins operate using +3.3-V power when HV_{DD} is connected to a +3.3-V power supply

Caution Since the V850E/MS1 uses different products depending on whether the external pin interface is a 5-V interface or a 3.3-V interface, the electrical characteristics are also different.

<4> External bus master is not connected
($\overline{\text{HLDRQ}}$ signal is pulled up)

Note that it may be necessary to add a margin of several ns to actual circuits since the delay time from the PCB wiring has not been included.

2.1 Connection with SRAM

2.1.1 Connection with μPD431008-20

In this circuit example, the V850E/MS1 uses two μPD431008LE-20 × 128 K (8 bits, 5 V) SRAM devices or two μPD431008LLE-A20 (128 K × 8 bits, 3 V) devices and is connected to a 256-Kbyte external memory space.

[Circuit configuration]

- V850E/MS1's internal system clock : 33 MHz
- Connected devices: μPD431008LE-20 (or μPD431008LLE-A20) × 2
- Memory usage: Memory block 1
  Assigned to address range 0200000H to 023FFFFH in external memory space (256-Kbyte space starting at address 0200000H)

[Connection approach and caution points]

The SRAM's $\overline{\text{WE}}$ pin is connected to the V850E/MS1's $\overline{\text{LWR}}$ pin if the SRAM has been connected to D0 to D7 in the V850E/MS1, or it is connected to the $\overline{\text{UWR}}$ pin if the SRAM has been connected to D8 to D15 in the V850E/MS1.

If the connected SRAM is the μPD431008LE-20, +5-V power is supplied to the SRAM's HV_{DD}, and if the connected SRAM is the μPD431008LLE-A20, +3.3-V power is supplied to the SRAM's HV_{DD}.

[Register settings]

- Memory block 1: SRAM, external ROM, external I/O mode
- Wait setting: 1 wait cycle
- Idle state: Insert

(1) Settings in BCT

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BCT	BT	BT	BT	BT	BT	BT	BT	BT	BT	BT	BT	BT	BT	BT	BT	BT
[FFFFF064H]	71	70	61	60	51	50	41	40	31	30	21	20	11	10	01	00
Memory block	7		6		5		4		3		2		1		0	

"SRAM, external ROM, external I/O" is specified in memory block 1
BCT's setting: xxxxxxxxxxxx00xxB

(2) Settings in BSC

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BSC	BS	BS	BS	BS	BS	BS	BS	BS	BS	BS	BS	BS	BS	BS	BS	BS
[FFFFF066H]	71	70	61	60	51	50	41	40	31	30	21	20	11	10	01	00
Memory block	7		6		5		4		3		2		1		0	

"16 bits" is specified in memory block 1
BSC's setting: xxxxxxxxxxxx01xxB

(3) Settings in DWC1 and DWC2

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DWC1	DW	DW	DW	DW	DW	DW	DW	DW	DW	DW	DW	DW	DW	DW	DW	DW
[FFFFF060H]	71	70	61	60	51	50	41	40	31	30	21	20	11	10	01	00
Memory block	7		6		5		4		3		2		1		0	

Bit	7	6	5	4	3	2	1	0
DWC2	DW	DW	DW	DW	DW	DW	DW	DW
[FFFFF06AH]	72	62	52	42	32	22	12	02
Memory block	7	6	5	4	3	2	1	0

"1 wait" is specified in memory block 1
DWC1's setting: xxxxxxxxxxxx01xxB
DWC2's setting: xxxxxx0xB

(4) Settings in BCC

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BCC	BC	BC	BC	BC	BC	BC	BC	BC	BC	BC	BC	BC	BC	BC	BC	BC
[FFFFF062H]	71	70	61	60	51	50	41	40	31	30	21	20	11	10	01	00
Memory block	7		6		5		4		3		2		1		0	

"Insert" is specified in memory block 1's idle state
BCC's setting: xxxxxxxxxxxx01xxB

Figure 2-1. Circuit Example (Connection with μPD431008-20)

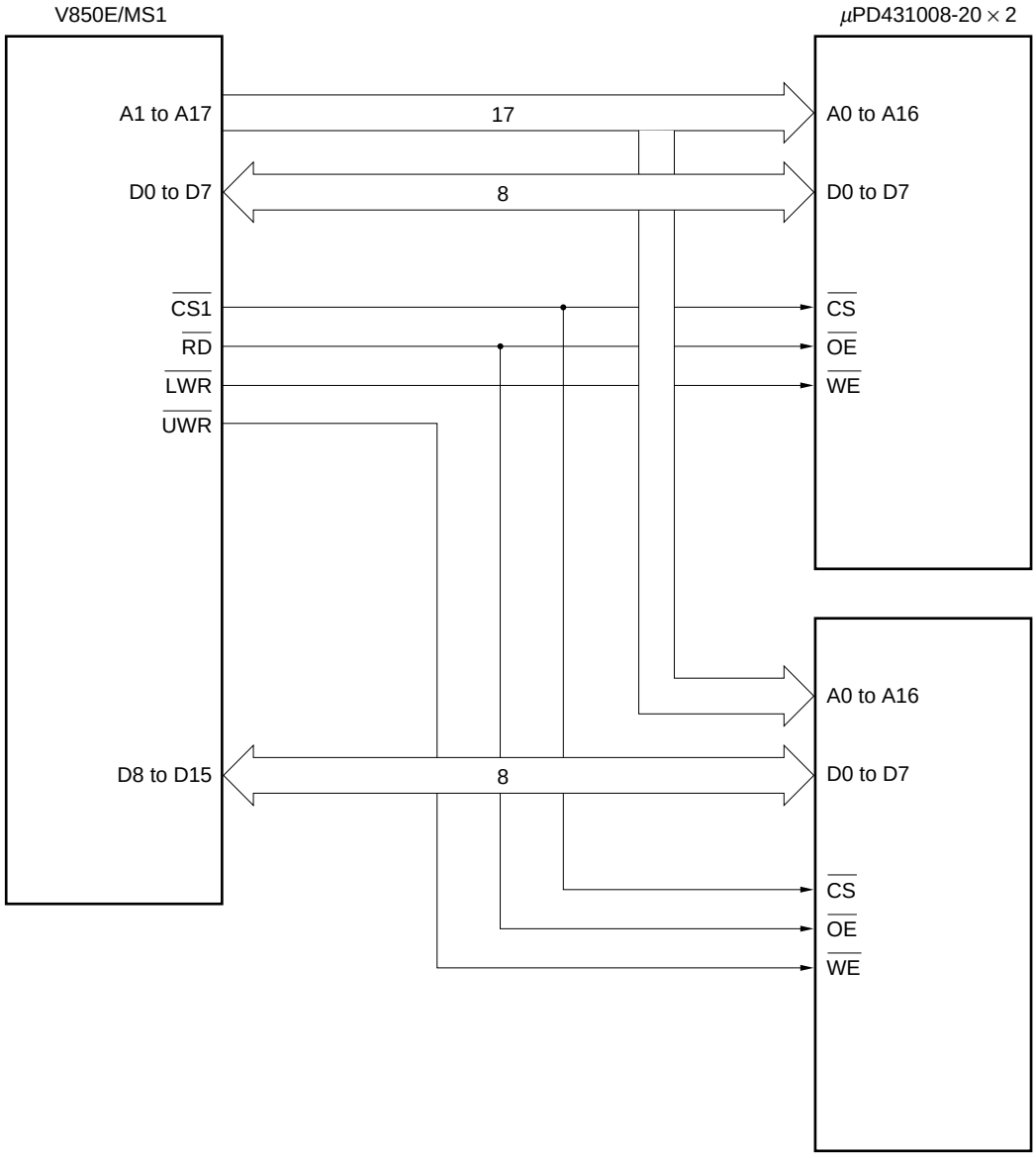
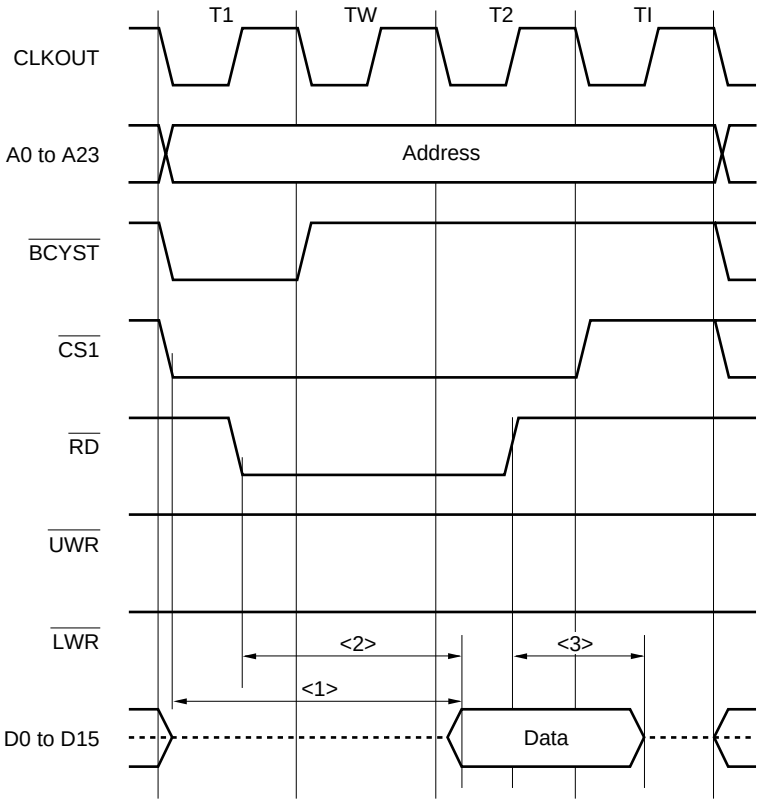


Figure 2-2. Read Operation in μPD431008-20



When connected to μPD431008LE-20

<1> Output delay time following active state transition of address and $\overline{CS}$ signals from μPD431008LE-20: 20 ns (Max.)
Maximum value for data input setup time (to address), based on the V850E/MS1's electrical characteristics (HV_{DD} = +5 V).

t_{SAID} (ns) = (1.5 + WD + W) T − 28
= 2.5 × 30 − 28; WD = 1, W = 0, T = 30 ns
= 47 ns (> 20 ns)

<2> Output delay time following active state transition of $\overline{OE}$ signal from μPD431008LE-20: 10 ns (Max.)
Maximum value for data input setup time (to $\overline{RD}$), based on the V850E/MS1's electrical characteristics (HV_{DD} = +5 V).

t_{SRDID} (ns) = (1 + WD + W) T − 32
= 2 × 30 − 32; WD = 1, W = 0, T = 30 ns
= 28 ns (> 10 ns)

<3> Output floating delay time following inactive state transition of $\overline{OE}$ signal from μPD431008LE-20: 7 ns (Max.)
Minimum value for data output delay time (from $\overline{RD}\uparrow$), based on the V850E/MS1's electrical characteristics (HV_{DD} = +5 V).

t_{DRDOD} (ns) = (0.5 + i) T − 10
= 1.5 × 30 − 10; i = 1, T = 30 ns
= 35 ns (> 7 ns)

Remark WD: Number of waits set by DWC
W: Number of waits due to $\overline{WAIT}$ signal
i: Idle state

When connected to μPD431008LLE-A20

<1> Output delay time following active state transition of address and $\overline{CS}$ signals from μPD431008LLE-A20: 20 ns (Max.)
Maximum value for data input setup time (to address), based on the V850E/MS1's electrical characteristics (HV_{DD} = +3.3 V).

t_{SAID} (ns) = (1.5 + WD + W) T − 28
= 2.5 × 30 − 28; WD = 1, W = 0, T = 30 ns
= 47 ns (> 20 ns)

<2> Output delay time following active state transition of $\overline{OE}$ signal from μPD431008LLE-A20: 10 ns (Max.)
Maximum value for data input setup time (to $\overline{RD}$), based on the V850E/MS1's electrical characteristics (HV_{DD} = +3.3 V).

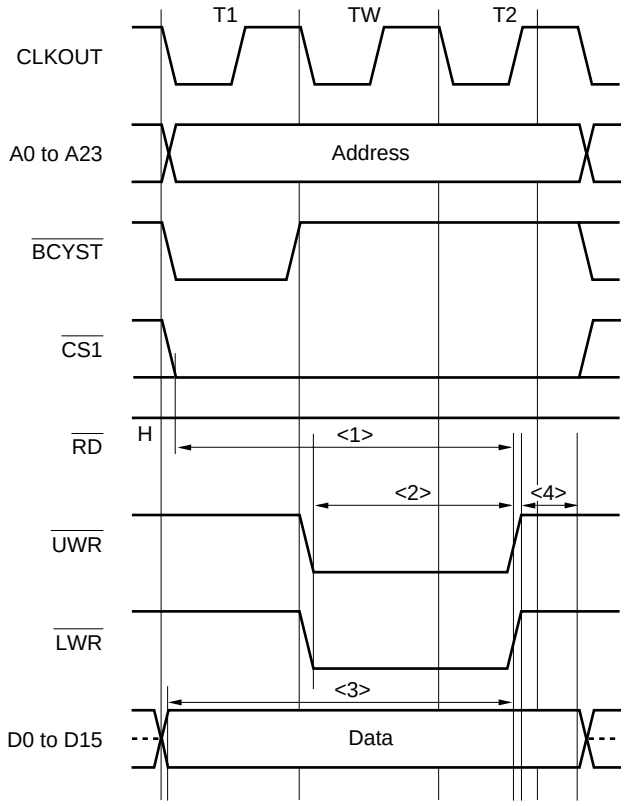
t_{SRDID} (ns) = (1 + WD + W) T − 32
= 2 × 30 − 32; WD = 1, W = 0, T = 30 ns
= 28 ns (> 10 ns)

<3> Output floating delay time following inactive state transition of $\overline{OE}$ signal from μPD431008LLE-A20: 9 ns (Max.)
Minimum value for data output delay time (from $\overline{RD}\uparrow$), based on the V850E/MS1's electrical characteristics (HV_{DD} = +3.3 V).

t_{DRDOD} (ns) = (0.5 + i) T − 10
= 1.5 × 30 − 10; i = 1, T = 30 ns
= 35 ns (> 9 ns)

Remark WD: Number of waits set by DWC
W: Number of waits due to $\overline{WAIT}$ signal
i: Idle state

Figure 2-3. Write Operation in μPD431008-20 - 1 (16-Bit Access)



When connected to μPD431008LE-20

<1> Time from active state transition of μPD431008LE-20's address and $\overline{CS}$ signals to end of write operation: 12 ns (Min.)
Minimum address setup time (to $\overline{UWR}$ and $\overline{LWR}\uparrow$), based on the V850E/MS1's electrical characteristics (HV_{DD} = +5 V).

t_{SAWR} (ns) = (1.5 + WD + W) T − 10
= 2.5 × 30 − 10; WD = 1, W = 0, T = 30 ns
= 65 ns (> 12 ns)

<2> μPD431008LE-20's $\overline{WE}$ active pulse width: 10 ns (Min.)
Minimum low-level width of $\overline{UWR}$ and $\overline{LWR}$, based on the V850E/MS1's electrical characteristics (HV_{DD} = +5 V).

t_{WWRL} (ns) = (1 + WD + W) T − 10
= 2 × 30 − 10; WD = 1, W = 0, T = 30 ns
= 50 ns (> 10 ns)

<3> Time from μPD431008LE-20's data valid recognition to end of write operation: 10 ns (Min.)

Minimum data output setup time (to $\overline{UWR}$ and $\overline{LWR}\uparrow$), based on the V850E/MS1's electrical characteristics (HV_{DD} = +5 V).

t_{SODWR} (ns) = (1.5 + WD + W) T – 10
= 2.5 × 30 – 10; WD = 1, W = 0, T = 30 ns
= 65 ns (> 10 ns)

<4> Data hold time following end of μPD431008LE-20's write operation: 0 ns (Min.)

Data output hold time (from $\overline{UWR}$ and $\overline{LWR}\uparrow$), based on the V850E/MS1's electrical characteristics (HV_{DD} = +5 V).

t_{HWROD} (ns) = 0.5T – 10
= 0.5 × 30 – 10; T = 30 ns
= 5 ns (> 0 ns)

Remark WD: Number of waits set by DWC
W: Number of waits due to $\overline{WAIT}$ signal

When connected to μPD431008LLE-A20

<1> Time from active state transition of μPD431008LLE-A20's address and $\overline{CS}$ signals to end of write operation: 12 ns (Min.)

Minimum address setup time (to $\overline{UWR}$ and $\overline{LWR}\uparrow$), based on the V850E/MS1's electrical characteristics (HV_{DD} = +3.3 V).

t_{SAWR} (ns) = (1.5 + WD + W) T – 10
= 2.5 × 30 – 10; WD = 1, W = 0, T = 30 ns
= 65 ns (> 12 ns)

<2> μPD431008LLE-A20's $\overline{WE}$ active pulse width: 10 ns (Min.)

Minimum low-level width of $\overline{UWR}$ and $\overline{LWR}$, based on the V850E/MS1's electrical characteristics (HV_{DD} = +3.3 V).

t_{WWRL} (ns) = (1 + WD + W) T – 10
= 2 × 30 – 10; WD = 1, W = 0, T = 30 ns
= 50 ns (> 10 ns)

<3> Time from μPD431008LLE-A20's data valid recognition to end of write operation: 10 ns (Min.)

Minimum data output setup time (to $\overline{UWR}$ and $\overline{LWR}\uparrow$), based on the V850E/MS1's electrical characteristics (HV_{DD} = +3.3 V).

t_{SODWR} (ns) = (1.5 + WD + W) T – 10
= 2.5 × 30 – 10; WD = 1, W = 0, T = 30 ns
= 65 ns (> 10 ns)

<4> Data hold time following end of μPD431008LLE-A20's write operation: 0 ns (Min.)

Minimum data output hold time (from $\overline{UWR}$ and $\overline{LWR}\uparrow$), based on the V850E/MS1's electrical characteristics (HV_{DD} = +3.3 V).

t_{HWROD} (ns) = 0.5T − 5

= 0.5 × 30 − 5; T = 30 ns

= 10 ns (> 0 ns)

Remark WD: Number of waits set by DWC

W: Number of waits due to $\overline{WAIT}$ signal

Figure 2-4. μPD431008-20 Write Operation - 2 (8-Bit Access to D0 to D7)

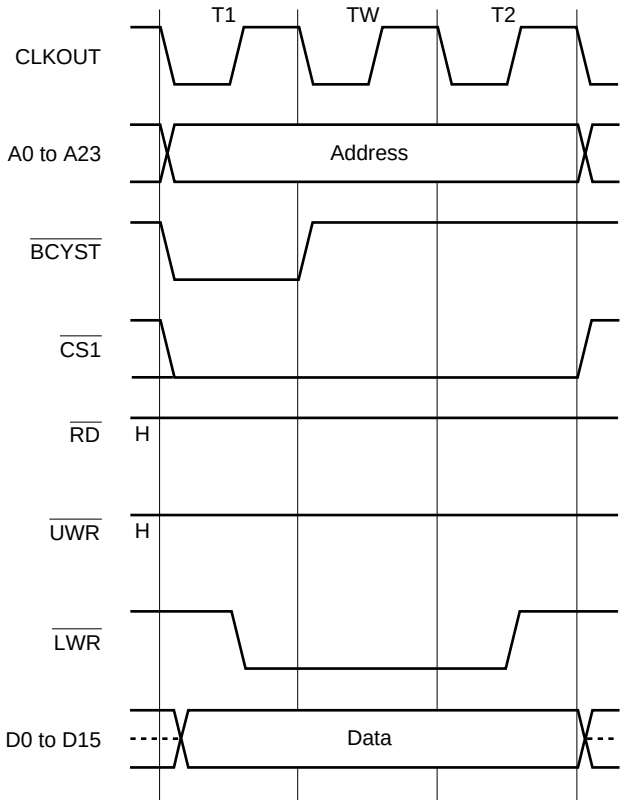
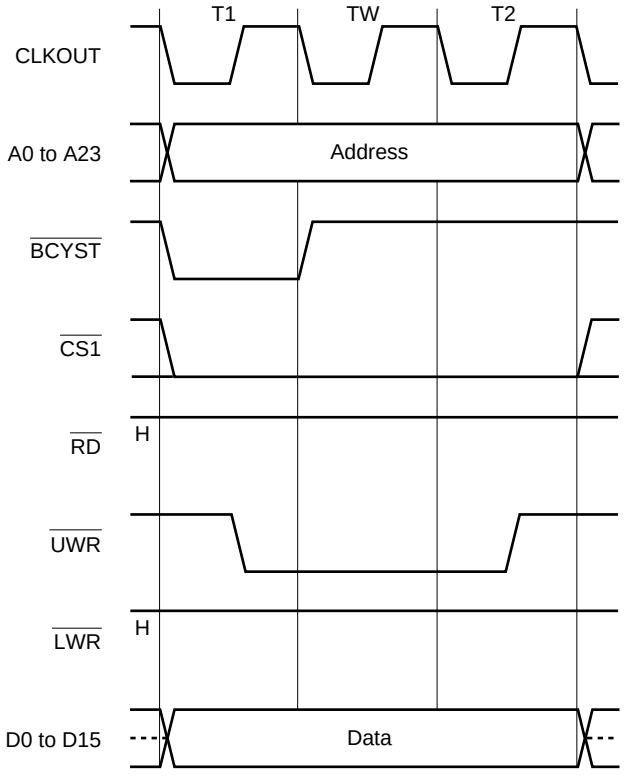


Figure 2-5. μPD431008-20 Write Operation - 3 (8-Bit Access to D8 to D15)



2.1.2 Wait/idle setting and system clock list for SRAM connection

Connection with μPD431008LE-15 (V850E/MS1's HV_{DD} = 5 V)

ϕ (System clock)	Waits	Idle insertion	Timing constrained
$\phi \leq$ 25 MHz	0	No	t_{SRDID}
25 MHz < $\phi \leq$ 26 MHz	1	No	t_{DRDOD}
26 MHz < ϕ ($\leq$ 40 MHz)	1	Yes	

Connection with μPD431008LE-20 (V850E/MS1's HV_{DD} = 5 V)

ϕ (System clock)	Waits	Idle insertion	Timing constrained
$\phi \leq$ 23 MHz	0	No	t_{SRDID}
23 MHz < $\phi \leq$ 26 MHz	1	Yes	t_{DRDOD}
26 MHz < ϕ ($\leq$ 40 MHz)	1	Yes	

Connection with μPD431000A-70 (V850E/MS1's HV_{DD} = 5 V)

ϕ (System clock)	Waits	Idle insertion	Timing constrained
$\phi \leq$ 13 MHz	0	No	t_{DRDOD}
13 MHz < $\phi \leq$ 14 MHz	0	Yes	t_{SRDID}
14 MHz < $\phi \leq$ 25 MHz	1	Yes	t_{SAID}
25 MHz < $\phi \leq$ 35 MHz	2	Yes	t_{SAID}
35 MHz < ϕ ($\leq$ 40 MHz)	3	Yes	

Connection with μPD431008LLE-A17 (V850E/MS1's HV_{DD} = 3.3 V)

ϕ (System clock)	Waits	Idle insertion	Timing constrained
$\phi \leq$ 24 MHz	0	No	t_{SRDID}
24 MHz < $\phi \leq$ 25 MHz	1	No	t_{DRDOD}
25 MHz < ϕ ($\leq$ 40 MHz)	1	Yes	

Connection with μPD431008LLE-A20 (V850E/MS1's HV_{DD} = 3.3 V)

ϕ (System clock)	Waits	Idle insertion	Timing constrained
$\phi \leq$ 23 MHz	0	No	t_{SRDID}, t_{DRDOD}
23 MHz < ϕ ($\leq$ 40 MHz)	1	Yes	

2.2 Connection with PROM

The following is an example in which one HN27C4096H PROM (256 K × 16 bits) is used to connect with a 512-Kbyte external ROM space.

[Circuit configuration]

- V850E's internal system clock: 33 MHz
- Connected device: HN27C4096H-85 × 1
- Memory usage: Memory block 0
  Assigned to address range 0000000H to 007FFFFH in external memory space (512-Kbyte space starting at address 0H)

[Connection approach and caution points]

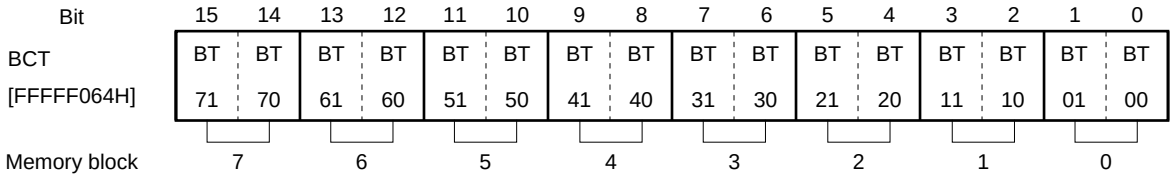
<1> Connection of the address signal from V850E/MS1 is shifted by one address (connected from A1) among the HN27C4096H-85's addresses since addresses are in byte units.

<2> Since the HN27C4096H-85's output floating delay time is 30 ns, idle insertion is required.
See **3.2 Connection with Slow PROM (27C1024-12)** for connection examples using devices that require more than a one-clock idle.

[Register settings]

- Memory block 0: SRAM, external ROM, external I/O mode
- Wait setting: 3 wait cycles
- Idle state: Insert

(1) Settings in BCT



"SRAM, external ROM, external I/O" is specified in memory block 0
BCT's setting: xxxxxxxxxxxxxx00B

(2) Settings in BSC

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BSC	BS	BS	BS	BS	BS	BS	BS	BS	BS	BS	BS	BS	BS	BS	BS	BS
[FFFFF066H]	71	70	61	60	51	50	41	40	31	30	21	20	11	10	01	00
Memory block	7		6		5		4		3		2		1		0	

"16 bits" is specified in memory block 0
BSC's setting: xxxxxxxxxxxxxx01B

(3) Settings in DWC1 and DWC2

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DWC1	DW	DW	DW	DW	DW	DW	DW	DW	DW	DW	DW	DW	DW	DW	DW	DW
[FFFFF060H]	71	70	61	60	51	50	41	40	31	30	21	20	11	10	01	00
Memory block	7		6		5		4		3		2		1		0	

Bit	7	6	5	4	3	2	1	0
DWC2	DW	DW	DW	DW	DW	DW	DW	DW
[FFFFF06AH]	72	62	52	42	32	22	12	02
Memory block	7	6	5	4	3	2	1	0

"3 waits" is specified in memory block 1
DWC1's setting: xxxxxxxxxxxxxx11B
DWC2's setting: xxxxxxx0B

(4) Settings in BCC

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BCC	BC	BC	BC	BC	BC	BC	BC	BC	BC	BC	BC	BC	BC	BC	BC	BC
[FFFFF062H]	71	70	61	60	51	50	41	40	31	30	21	20	11	10	01	00
Memory block	7		6		5		4		3		2		1		0	

"Insert" is specified in memory block 0's idle state
BCC's setting: xxxxxxxxxxxxxx01B

Figure 2-6. Circuit Example (Connection with HN27C4096H-85)

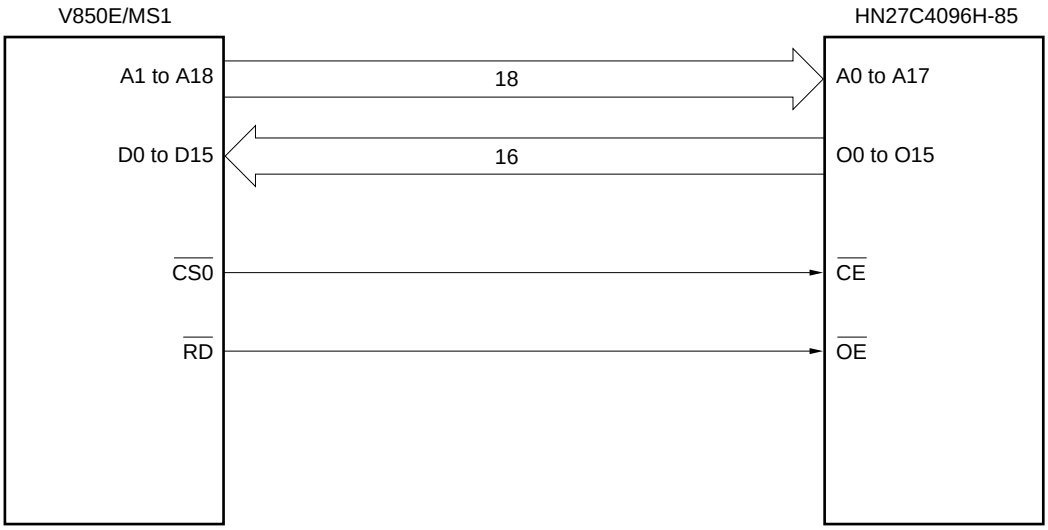
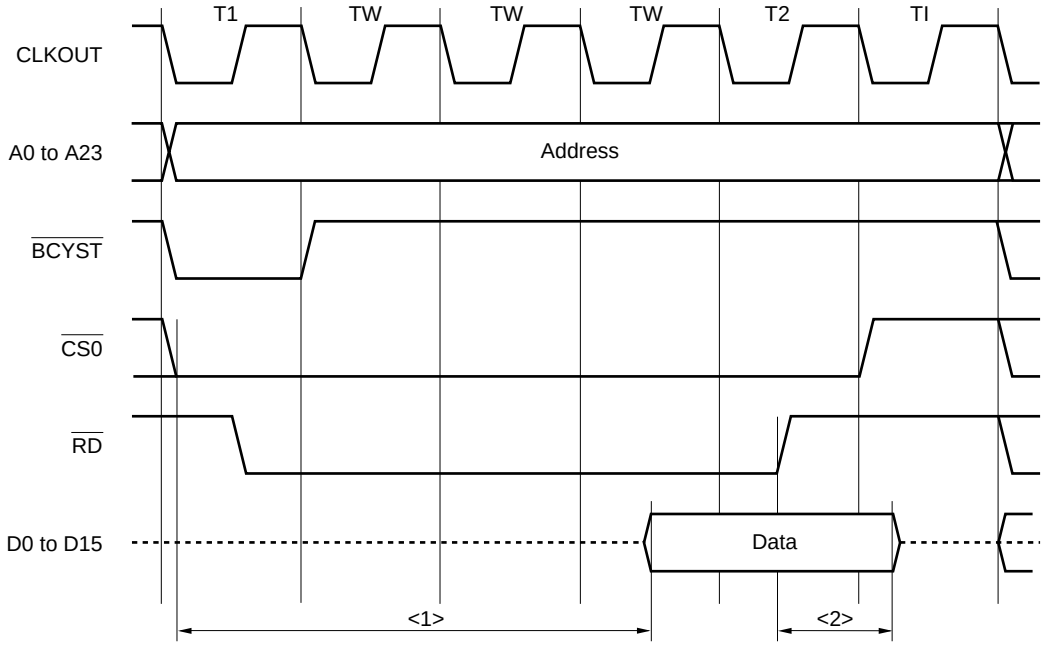


Figure 2-7. Read Operation in HN27C4096H-85



<1> Data output delay time after 27C4096H-85's $\overline{CE}$ signal is active: 85 ns (Max.)

<2> Data output floating delay time after 27C4096H-85's $\overline{OE}$ signal is inactive: 30 ns (Max.)

Remark Broken lines indicate high impedance.

2.3 Connection with Fast Page DRAM

The following is an example in which one μPD42S16160 fast page DRAM (1 M × 16 bits) is used to connect with a 2-Mbyte external memory space.

[Circuit configuration]

- V850E's internal system clock: 33 MHz
- Connected device: μPD42S16160-50 × 1
- Memory usage: Memory block 2
  Assigned to address range 0400000H to 05FFFFFH in external memory space (2-Mbyte space starting at address 04000000H)

[Connection approach and caution points]

<1> The DRAM access timing can be set via four operations, one to each of the DRAM configuration registers (DRC0 to DRC3). One configuration register is specified for each memory block to determine the particular operation. In this example, the access timing is set to the DRC0 register.

<2> The V850E/MS1's address pins A1 to A12 are connected to pins A0 to A11 in the μPD42S16160. Since the μPD42S16160 has 12 high-order bits (corresponding to the row address) and 8 low-order bits (corresponding to the column address), an address multiplex width is set as shown below for the V850E/MS1's pins A1 to A12 when outputting the row address.

	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1
Row address	a20	a19	a18	----------							a10	a9

<3> Since CBR refresh operates at the rate of 4096 cycles per 128 ms, the refresh interval is set to 31.25 μs or less.

<4> If a wait can be inserted to either setting in the DRAM configuration register, it should be inserted to the less frequently used setting.

Example[Note]: If a wait can be inserted (or added) either as a hold wait or data wait for the row address, insert (or add) the hold wait for the row address.

Reason This reduces the number of waits when on page.

Note This does not apply to the settings shown in this section.

[Register settings]

- Memory block 2: DRAM mode
- Specified DRAM configuration register: DRC0
- Type of DRAM: Fast page DRAM
- RAS hold mode: Enabled
- Idle state: Insert

(1) Settings in BCT

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BCT	BT	BT	BT	BT	BT	BT	BT	BT	BT	BT	BT	BT	BT	BT	BT	BT
[FFFFF064H]	71	70	61	60	51	50	41	40	31	30	21	20	11	10	01	00
Memory block	7		6		5		4		3		2		1		0	

"DRAM" is specified in memory block 2

BCT's setting: xxxxxxxxxx10xxxxB

(2) Settings in BSC

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BSC	BS	BS	BS	BS	BS	BS	BS	BS	BS	BS	BS	BS	BS	BS	BS	BS
[FFFFF066H]	71	70	61	60	51	50	41	40	31	30	21	20	11	10	01	00
Memory block	7		6		5		4		3		2		1		0	

"16 bits" is specified in memory block 2

BSC's setting: xxxxxxxxxx01xxxxB

(3) Settings in BCC

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BCC	BC	BC	BC	BC	BC	BC	BC	BC	BC	BC	BC	BC	BC	BC	BC	BC
[FFFFF062H]	71	70	61	60	51	50	41	40	31	30	21	20	11	10	01	00
Memory block	7		6		5		4		3		2		1		0	

"Insert" is specified in memory block 2's idle state

BCC's setting: xxxxxxxxxx01xxxxB

(4) Settings in DRC0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DRC0	PAE	PAE	RPC	RPC	RHC	RHC	DAC	DAC	CPC	CPC	0	RHD	0	0	DAW	DAW
[FFFFF200H]	10	00	10	00	10	00	10	00	10	00		0			10	00

PAE10, 00: 0, 1 ⋯ Fast page DRAM
RPC10, 00: 0, 1 ⋯ Number of row address precharge waits (RPWs) = 1
RHC10, 00: 0, 1 ⋯ Number of row address hold waits (RHWs) = 1
DAC10, 00: 0, 1 ⋯ Number of data waits (DAWs) = 1
CPC10, 00: 0, 0 ⋯ Number of column address precharge waits (CPWs) = 0
RHD0: 0 ⋯ RAS hold mode is enabled
DAW10, 00: 0, 0 ⋯ Address multiplex width: 8 bits
Setting to DRC0: 5500H

(5) Settings in DTC

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DTC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC
[FFFFF220H]	71	70	61	60	51	50	41	40	31	30	21	20	11	10	01	00
Memory block	7		6		5		4		3		2		1		0	

"DRC0" is specified in memory block 2
DTC's setting: xxxxxxxxxx00xxxxB

(6) Settings in RFC0[Note]

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RFC0	REN	0	0	0	0	0	RCC	RCC	0	0	RI	RI	RI	RI	RI	RI
[FFFFF210H]	0						01	00			05	04	03	02	01	00

REN0: 1 ⋯ Refresh enable
RCC01, 00: 0, 0 ⋯ Refresh count clock (32ϕ)
RI05 to 00: 0, 1, 1, 1, 1, 1 ⋯ Interval factor 32
Setting to RFC0: 801FH
Since ϕ = 33 MHz (0.030 μs), the refresh interval for the above setting is as follows.
Refresh interval = $32 \times 0.030 \times 32$
= 30.72 (μs)

Note Since DRC0 is used as the configuration register, RFC0 is used to specify a refresh operation.

(7) Settings in RWC

Bit	7	6	5	4	3	2	1	0
RWC [FFFFF218H]	RRW1	RRW0	RCW2	RCW1	RCW0	SRW2	SRW1	SRW0

RRW1, 0: 0, 1 ⋯ Number of refresh RAS waits (RRWs) = 1
RCW2 to 0: 0, 0, 0 ⋯ Number of refresh cycle waits (RCWs) = 0
Setting to RWC: 40H

Remark Self refresh is not used in this case. If there are other connected DRAMs, the RRW and RCW settings should be set for the slowest memory.

Figure 2-8. Circuit Example (Connection with μPD42S16160-50)

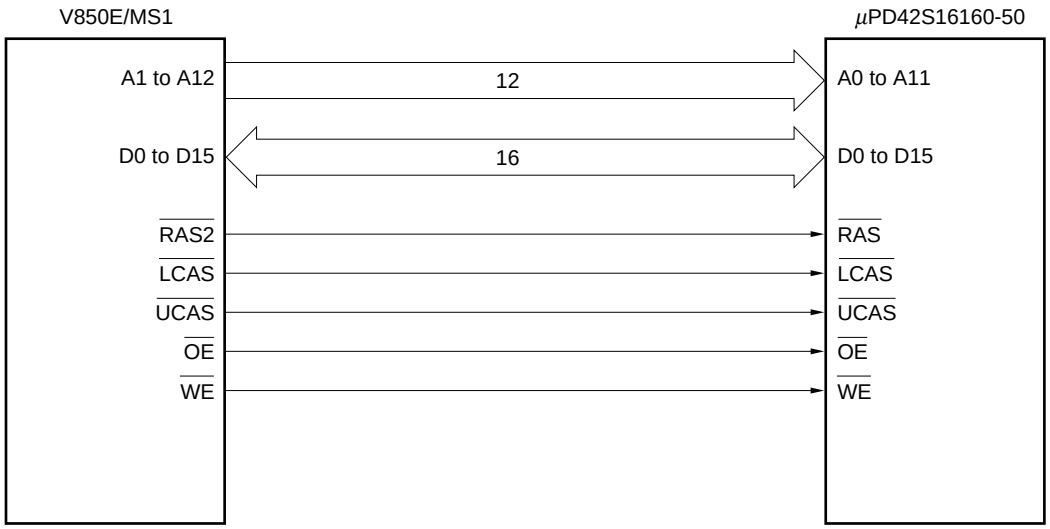
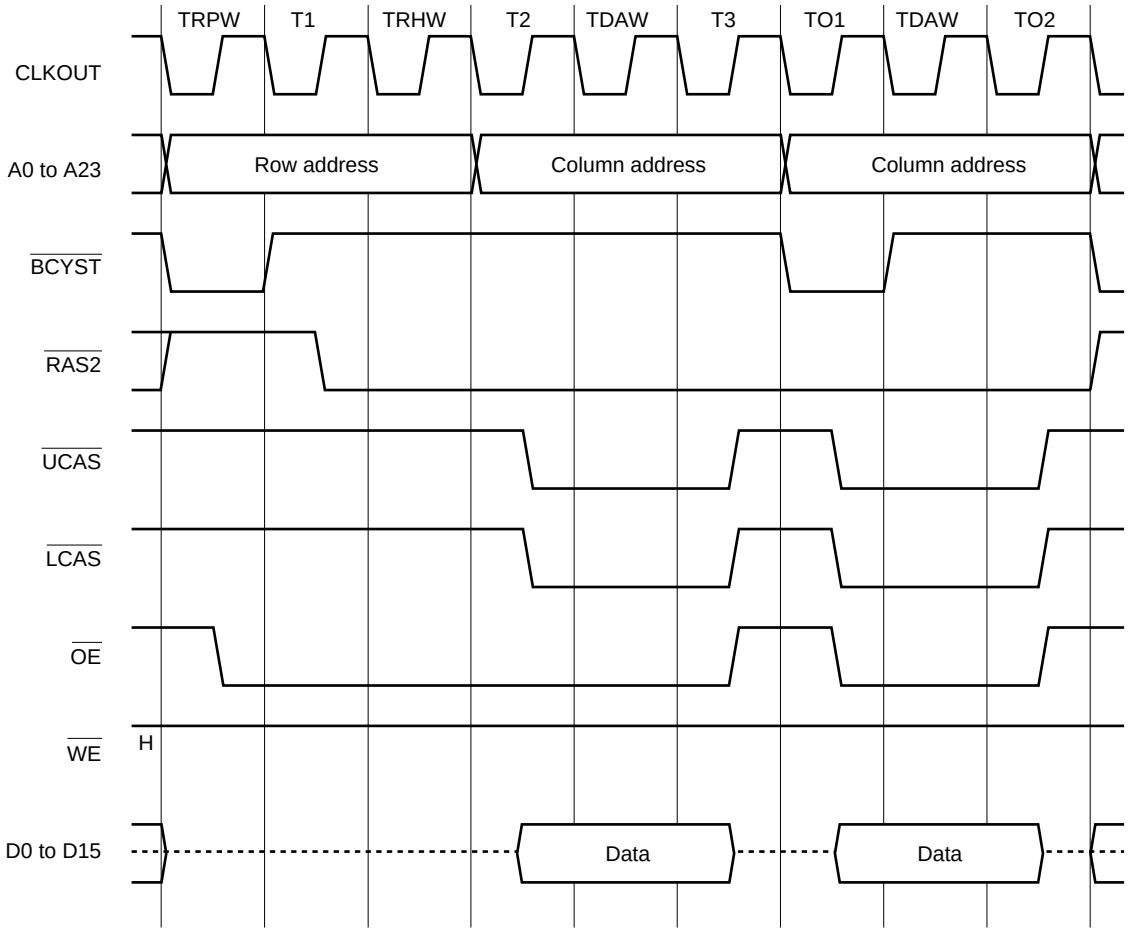
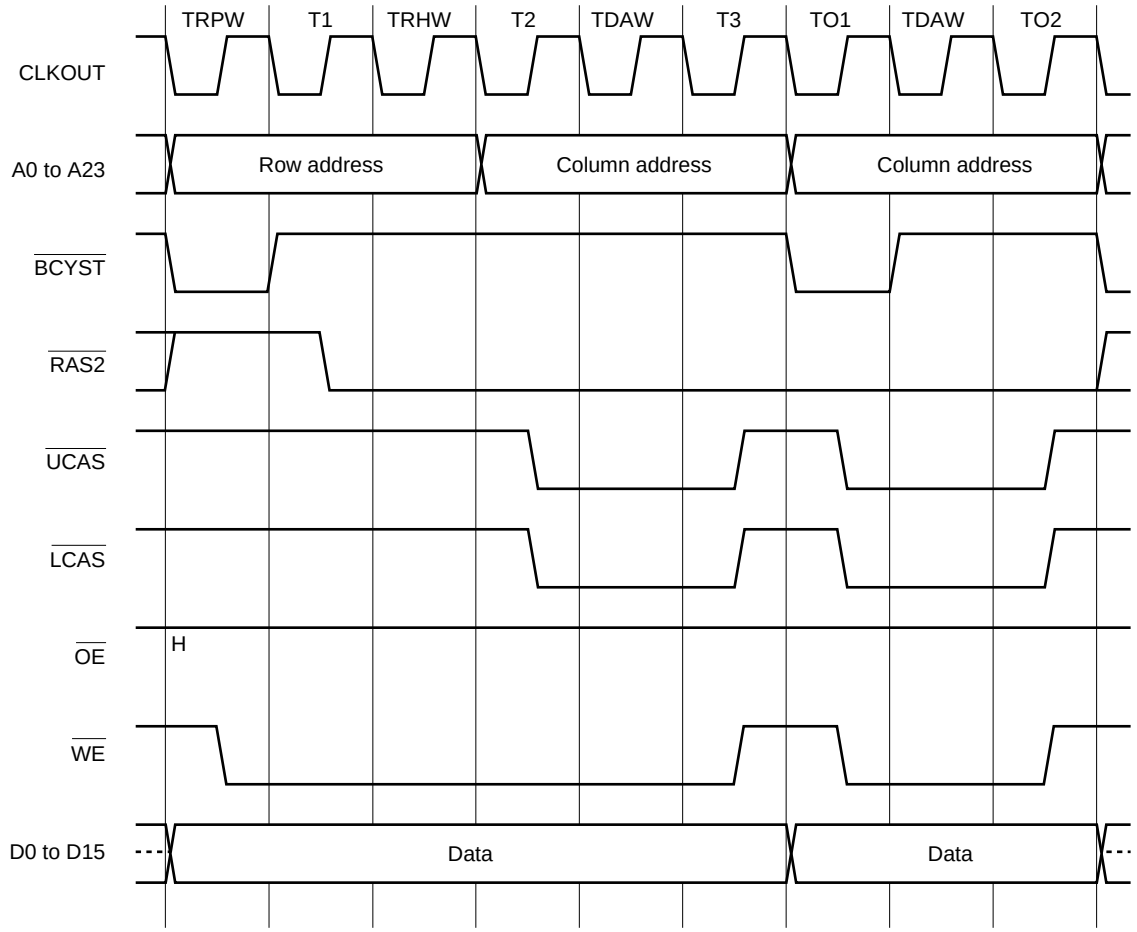


Figure 2-9. Read Operation in μPD42S16160-50



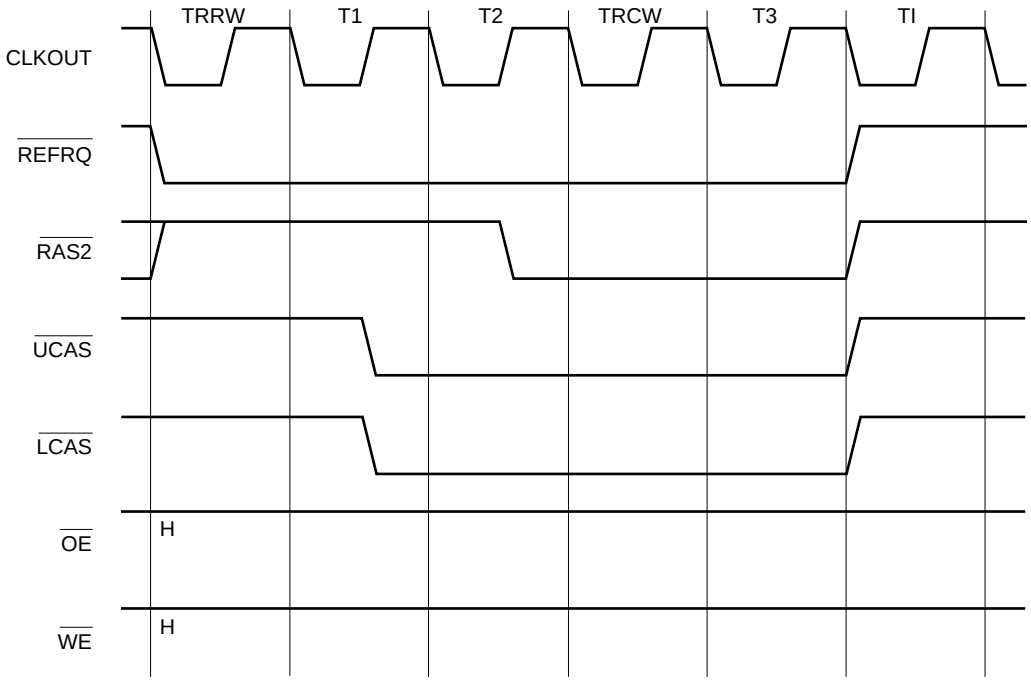
Remark Broken lines indicate high impedance.

Figure 2-10. Write Operation in μPD42S16160-50



Remark Broken lines indicate high impedance.

Figure 2-11. Refresh Operation in μPD42S16160-50



2.4 Connection with EDO DRAM

The following is an example in which one μPD42S18165 EDO DRAM (1 M × 16 bits) is used to connect with a 2-Mbyte external memory space.

[Circuit configuration]

- V850E's main system clock: 33 MHz
- Connected device: μPD42S18165-50 × 1
- Memory usage: Memory block 3
  Assigned to address range 0800000H to 09FFFFFH in external memory space (2-Mbyte space starting at address 0800000H)

[Connection approach and caution points]

<1> The DRAM access timing is set to DRC1.

<2> The V850E/MS1's address pins A1 to A10 are connected to the pins A0 to A9 in the μPD42S18165. Since the μPD42S18165 has 10 high-order bits and 10 low-order bits, an address multiplex width is set as shown below for the V850E/MS1's pins A1 to A10 when outputting the row address.

	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1
Row address	a20	----------							a12	a11

<3> Since CBR refresh operates at the rate of 1024 cycles per 128 ms, the refresh interval is set to 125 μs or less.

[Register settings]

- Memory block 3: DRAM mode
- Specified DRAM configuration register: DRC1
- Type of DRAM: EDO DRAM
- RAS hold mode: Enabled
- Idle state: Insert

(1) Settings in BCT

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BCT	BT	BT	BT	BT	BT	BT	BT	BT	BT	BT	BT	BT	BT	BT	BT	BT
[FFFFF064H]	71	70	61	60	51	50	41	40	31	30	21	20	11	10	01	00
Memory block	7		6		5		4		3		2		1		0	

"DRAM" is specified in memory block 3
BCT's setting: xxxxxxxx10xxxxxxB

(2) Settings in BSC

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BSC	BS	BS	BS	BS	BS	BS	BS	BS	BS	BS	BS	BS	BS	BS	BS	BS
[FFFFF066H]	71	70	61	60	51	50	41	40	31	30	21	20	11	10	01	00
Memory block	7		6		5		4		3		2		1		0	

"16 bits" is specified in memory block 3
BSC's setting: xxxxxxxx01xxxxxxB

(3) Settings in BCC

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BCC	BC	BC	BC	BC	BC	BC	BC	BC	BC	BC	BC	BC	BC	BC	BC	BC
[FFFFF062H]	71	70	61	60	51	50	41	40	31	30	21	20	11	10	01	00
Memory block	7		6		5		4		3		2		1		0	

"Insert" is specified in memory block 3's idle state
BCC's setting: xxxxxxxx01xxxxxxB

(4) Settings in DRC1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DRC1	PAE	PAE	RPC	RPC	RHC	RHC	DAC	DAC	CPC	CPC	0	RHD	0	0	DAW	DAW
[FFFFF202H]	11	01	11	01	11	01	11	01	11	01		1			11	01

PAE11, 01: 1, 0 EDO DRAM
RPC11, 01: 0, 1 Number of row address precharge waits (RPWs) = 1
RHC11, 01: 0, 1 Number of row address hold waits (RHWs) = 1
DAC11, 01: 0, 1 Number of data waits (DAWs) = 1
CPC11, 01: 0, 1 Number of column address precharge waits (CPWs) = 1
RHD1: 0 RAS hold mode is enabled
DAW11, 01: 1, 0 Address multiplex width: 10 bits
Setting to DRC1: 9542H

(5) Settings in DTC

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DTC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC
[FFFFF220H]	71	70	61	60	51	50	41	40	31	30	21	20	11	10	01	00
Memory block	7		6		5		4		3		2		1		0	

"DRC1" is specified in memory block 3
DTC's setting: xxxxxxxx01xxxxxxB

(6) Settings in RFC1[Note]

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RFC1	REN	0	0	0	0	0	RCC	RCC	0	0	RI	RI	RI	RI	RI	RI
[FFFFF212H]	1						11	10			15	14	13	12	11	10

REN1: 1 ⋯ Refresh enable
RCC11, 10: 0, 1 ⋯ Refresh count clock (128ϕ)
RI15 to 10: 0, 1, 1, 1, 1, 1 ⋯ Interval factor 32

Setting to RFC1: 811FH
Since ϕ = 33 MHz (0.03 μs), the refresh interval for the above setting is as follows.
Refresh interval = $128 \times 0.03 \times 32$
= 122.9 (μs)

Note Since DRC1 is used as the configuration register, RFC1 is used to specify a refresh operation.

(7) Settings in RWC

Bit	7	6	5	4	3	2	1	0
RWC	RRW1	RRW0	RCW2	RCW1	RCW0	SRW2	SRW1	SRW0
[FFFFF218H]								

RRW1, 0: 0, 1 ⋯ Number of refresh RAS waits (RRWs) = 1
RCW2 to 0: 0, 0, 0 ⋯ Number of refresh cycle waits (RCWs) = 0
Setting to RWC: 40H

Remark Self refresh is not used in this case. If there are other connected DRAMs, the RRW and RCW settings should be set for the slowest memory.

Figure 2-12. Circuit Example (Connection with μPD42S18165-50)

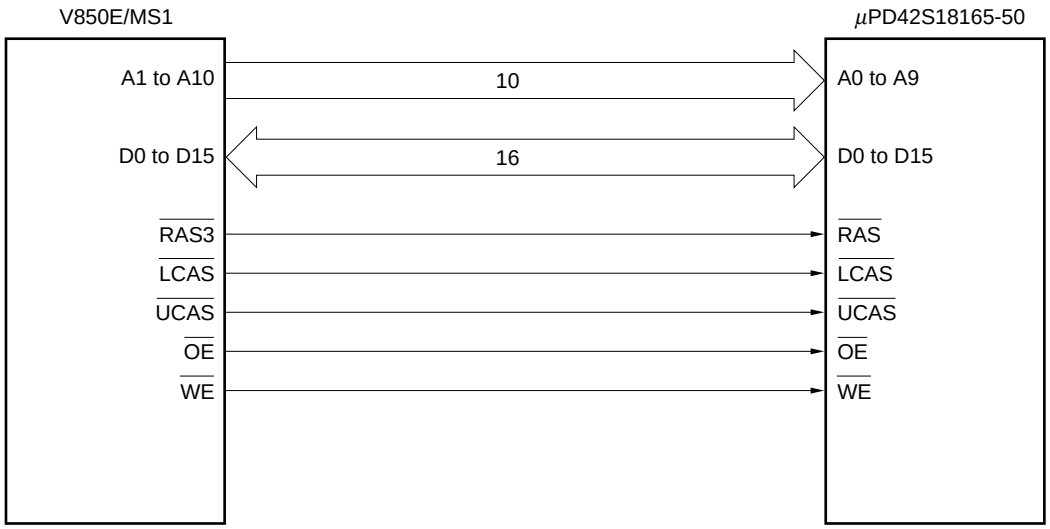
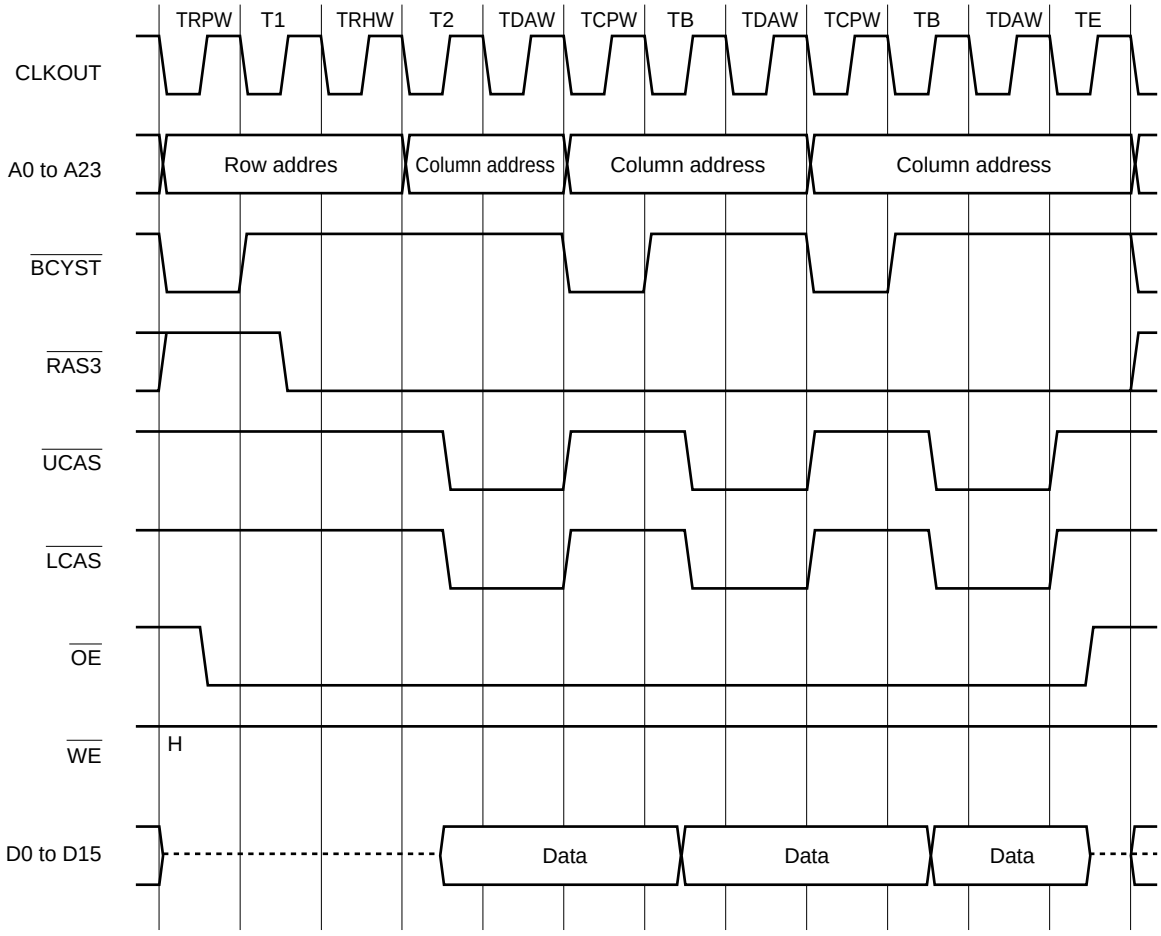
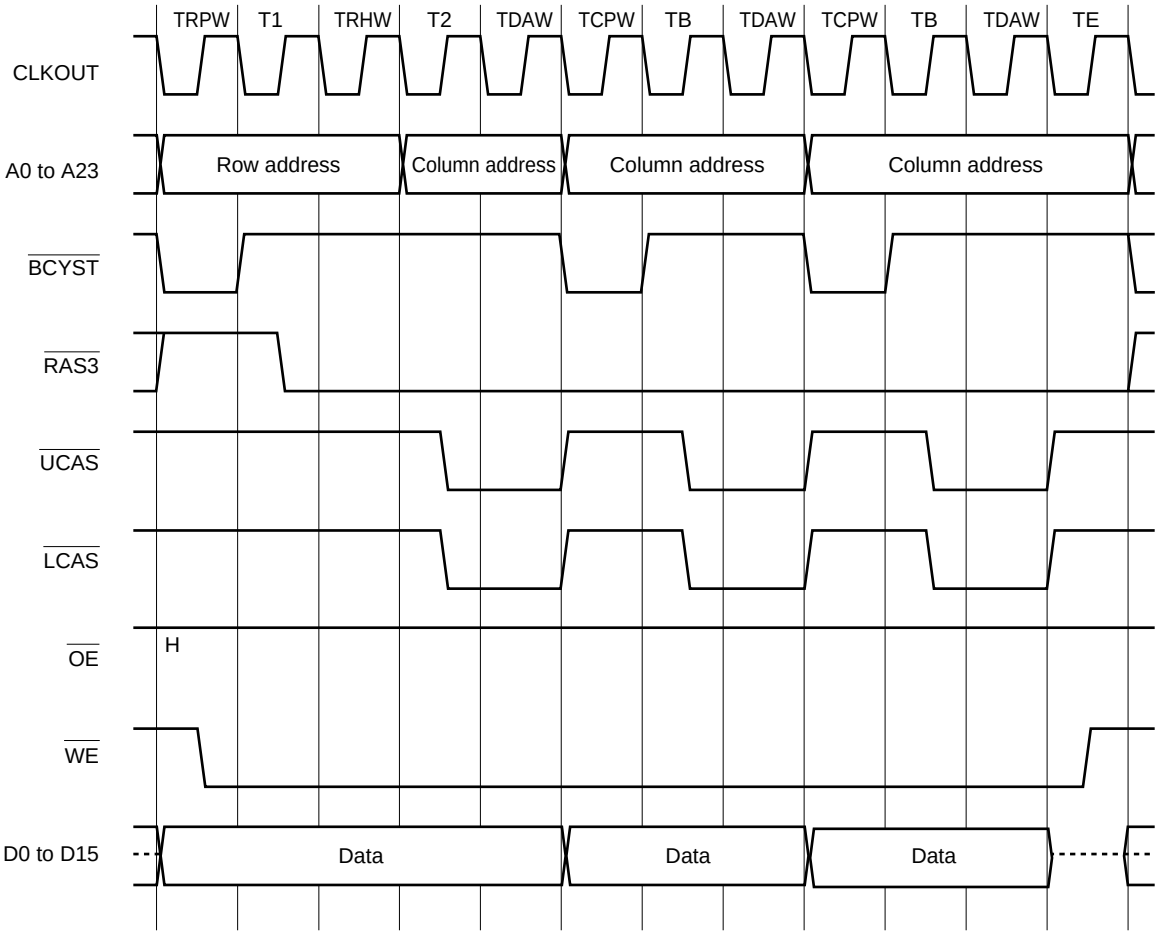


Figure 2-13. Read Operation in μPD42S18165-50



Remark Broken lines indicate high impedance.

Figure 2-14. Write Operation in μPD42S18165-50



Remark Broken lines indicate high impedance.

CHAPTER 3 BUS INTERFACE-CONNECTED CIRCUIT EXAMPLES - 2

This chapter shows examples of types of memory that cannot be directly connected to the V850E/MS1's bus interface and are therefore connected using added circuits. The approach behind the configuration of these circuit examples is as follows.

<1> Programmable wait used for wait control
($\overline{\text{WAIT}}$ signal is pulled up)

<2> External pins operate using +5-V power when HV_{DD} is connected to a +5-V power supply
External pins operate using +3.3-V power when HV_{DD} is connected to a +3.3-V power supply

Caution Since the V850E/MS1 uses different products depending on whether the external pin interface is a 5-V interface or a 3.3-V interface, the electrical characteristics are also different.

<3> External bus master is not connected except for SIMM connection
($\overline{\text{HLDRQ}}$ signal is pulled up except for SIMM connection)

The signal propagation delay time caused by the added circuit is calculated as ranging from 2 ns (minimum) to 7 ns (maximum). In an actual circuit, the specifications of used devices must also be taken into account when calculating this delay time. In this chapter, the register setting information is simplified. For more detailed register setting information, see **CHAPTER 2**.

3.1 Connection with 16-Bit SRAM

In this circuit example, the V850E/MS1 uses one μPD431016 SRAM (64 K × 16 bits) device and is connected to a 128-Kbyte memory space.

[Circuit configuration]

- V850E's internal system clock: 25 MHz
- Connected devices: μPD431016LE-20 × 1
- Memory usage: Memory block 1
  Assigned to address range 0200000H to 021FFFFH in external memory space
  (128-Kbyte space starting at address 0200000H)

[Connection approach and caution points]

Since there is no byte select signal in the V850E/MS1, the μPD431016's byte select signal, $\overline{\text{LB}}$ signal, and $\overline{\text{UB}}$ signal are generated from the V850E/MS1's $\overline{\text{RD}}$ signal, $\overline{\text{LWR}}$ signal, and $\overline{\text{UWR}}$ signal.

The μPD431016's $\overline{\text{WE}}$ signal is connected by the ORed result of the V850E/MS1's $\overline{\text{LWR}}$ and $\overline{\text{UWR}}$ signals.

[Register settings]

- Memory block 1: SRAM, external ROM, external I/O mode
- Wait setting: 1 wait cycle
- Idle state: Not inserted

Register	Setting	Function
BCT	xxxxxxxxxxxx00xxB	Block 1: SRAM, external ROM, external I/O mode
BSC	xxxxxxxxxxxx01xxB	Block 1: 16 bits
DWC1	xxxxxxxxxxxx01xxB	Block 1: 1 wait
DWC2	xxxxxx0xB	
BCC	xxxxxxxxxxxx00xxB	Block 1: Idle is not inserted

Figure 3-1. Circuit Example (Connection with μPD431016LE-20)

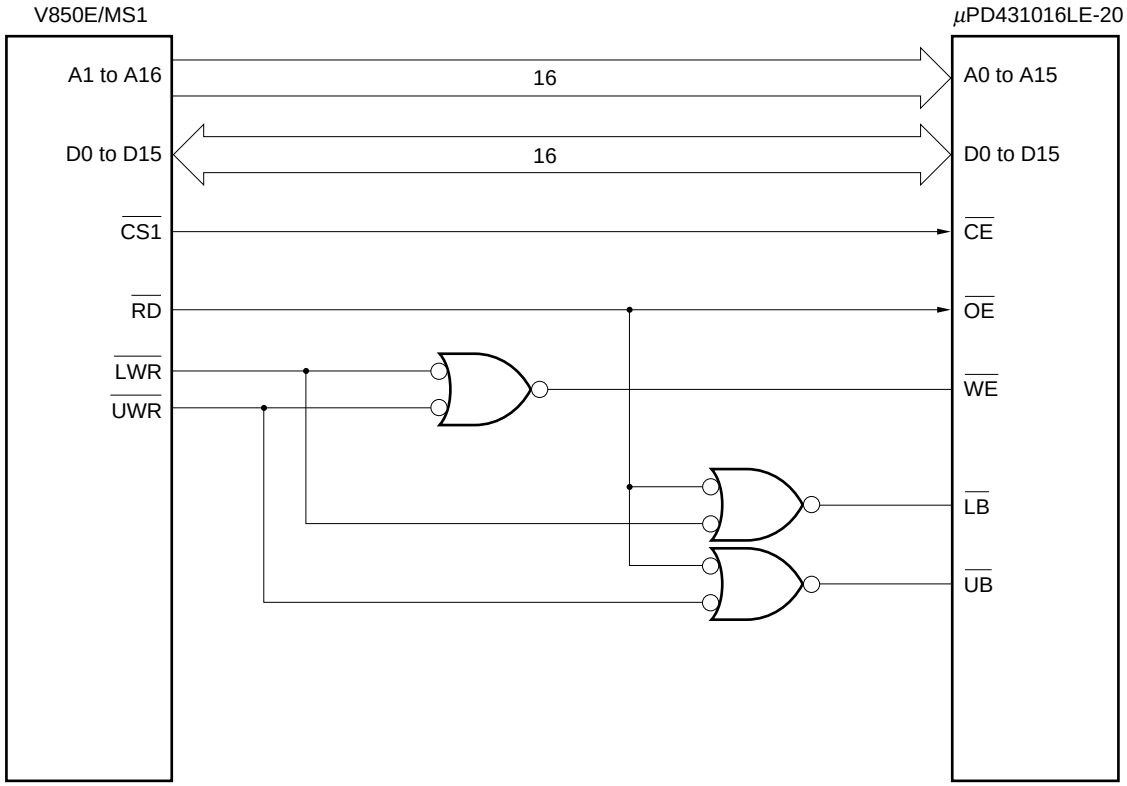
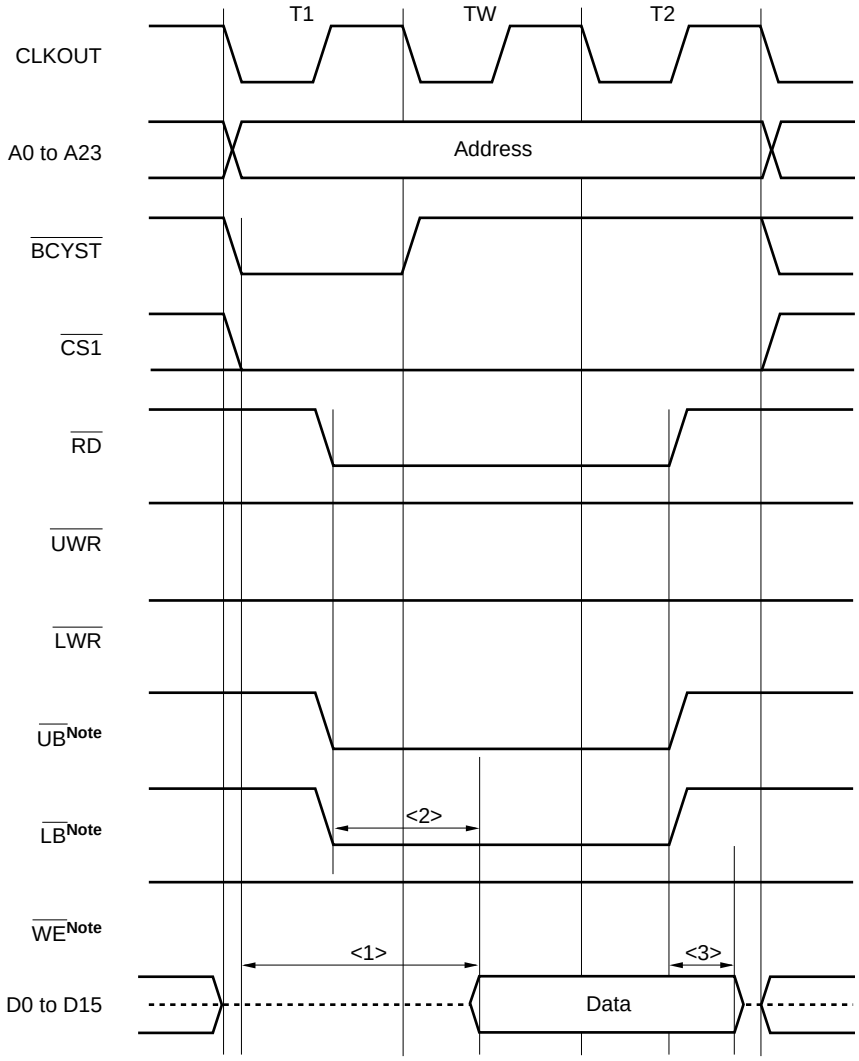


Figure 3-2. Read Operation in μPD431016LE-20 (8-Bit Access/16-Bit Access)



Note $\overline{UB}$, $\overline{LB}$, and $\overline{WE}$ are pins of the μPD431016.

Remark Broken lines indicate high impedance.

<1> Output delay time following active state transition of address and $\overline{CS}$ signals from μPD431016LE-20: 20 ns (Max.)
Maximum value for data input setup time (to address), based on the V850E/MS1's electrical characteristics (HV_{DD} = +5 V).

t_{SAID} (ns) = (1.5 + WD + W) T − 28
= 2.5 × 40 − 28; WD = 1, W = 0, T = 40 ns
= 72 ns (> 20 ns)

<2> Output delay time following active state transition of $\overline{OE}$, $\overline{LB}$, and $\overline{UB}$ signals from μPD431016LE-20: 10 ns (Max.)
Maximum value for data input setup time (to $\overline{RD}\downarrow$), based on the V850E/MS1's electrical characteristics (HV_{DD} = +5 V).

t_{SRDID} (ns) = (1 + WD + W) T − 32
= 2 × 40 − 32; WD = 1, W = 0, T = 40 ns
= 48 ns

When maximum delay time from added circuit for $\overline{LB}$ and $\overline{UB}$ is taken into account:

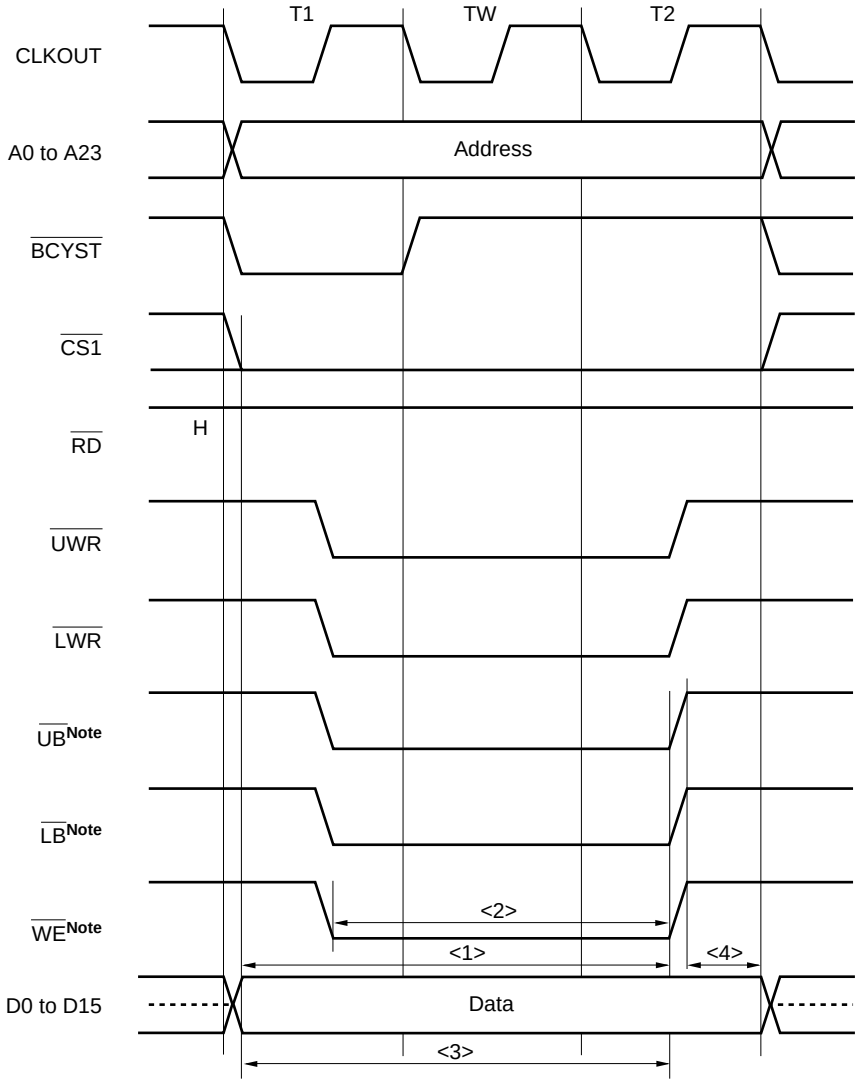
t_{SRDID} − added circuit delay time = 48 − 7
= 41 ns (> 10 ns)

<3> Output floating delay time following inactive state transition of $\overline{OE}$ signal from μPD431016LE-20: 7 ns (Max.)
Minimum value for data output delay time (from RD↑), based on the V850E/MS1's electrical characteristics (HV_{DD} = +5 V).

t_{DRDOD} (ns) = (0.5 + i) T − 12
= 0.5 × 40 − 12; i = 0, T = 40 ns
= 8 ns (> 7 ns)

Remark WD: Number of waits set by DWC
W: Number of waits due to $\overline{WAIT}$ signal
i: Idle state

Figure 3-3. Write Operation in μPD431016LE-20 - 1 (16-Bit Access)



Note $\overline{UB}$, $\overline{LB}$, and $\overline{WE}$ are pins of the μPD431016.

Remark Broken lines indicate high impedance.

<1> Time from active state transition of μPD431016LE-20's address and $\overline{CS}$ signals to end of write operation: 12 ns (Min.)
Minimum address setup time (to $\overline{UWR}$ and $\overline{LWR}\uparrow$), based on the V850E/MS1's electrical characteristics (HV_{DD} = +5 V).

t_{SAWR} (ns) = (1.5 + WD + W) T − 10
= 2.5 × 40 − 10; WD = 1, W = 0, T − 40 ns
= 90 ns (> 12 ns)

<2> μPD431016LE-20's $\overline{WE}$ active pulse width: 10 ns (Min.)

Minimum low-level width of $\overline{UWR}$ and $\overline{LWR}$, based on the V850E/MS1's electrical characteristics (HV_{DD} = +5 V).

t_{WWRL} (ns) = (1 + WD + W) T – 10

= 2 × 40 – 10; WD = 1, W = 0, T = 40 ns

= 70 ns (> 10 ns)

When maximum delay time from added circuit for $\overline{WE}$ is taken into account:

t_{WWRL} - added circuit delay time = 70 – 7

= 63 ns (> 10 ns)

<3> Time from μPD431016LE-20's data valid recognition to end of write operation: 10 ns (Min.)

Minimum data output setup time (to $\overline{UWR}$ and $\overline{LWR}\uparrow$), based on the V850E/MS1's electrical characteristics (HV_{DD} = +5 V).

t_{SODWR} (ns) = (1.5 + WD + W) T – 10

= 2.5 × 40 – 10; WD = 1, W = 0, T = 40 ns

= 80 ns (> 10 ns)

<4> Data hold time following end of μPD431016LE-20's write operation: 0 ns (Min.)

Minimum data output hold time (from $\overline{UWR}$ and $\overline{LWR}\uparrow$), based on the V850E/MS1's electrical characteristics (HV_{DD} = +5 V).

t_{HWROD} (ns) = 0.5 T – 10

= 0.5 × 40 – 10; T = 40 ns

= 10 ns

When maximum delay time from added circuit for $\overline{WE}$ is taken into account:

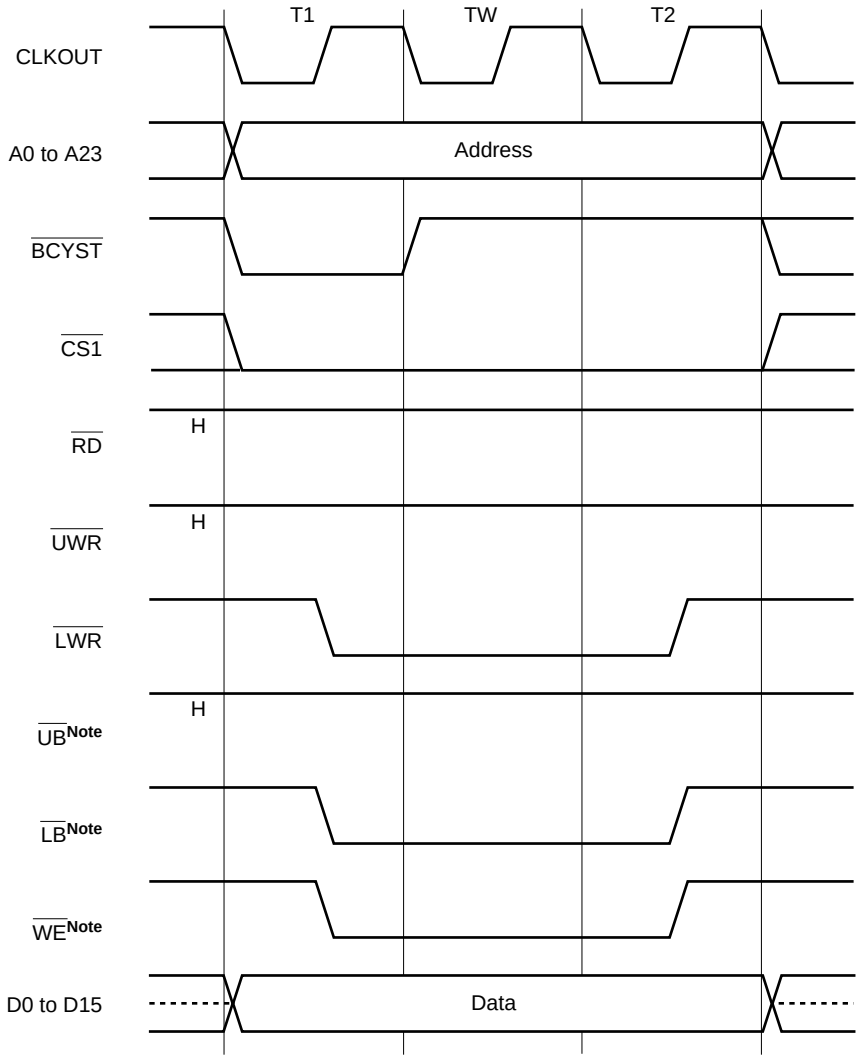
t_{HWROD} – added circuit delay time = 10 – 7

= 3 ns (> 0 ns)

Remark WD: Number of waits set by DWC

W: Number of waits due to $\overline{WAIT}$ signal

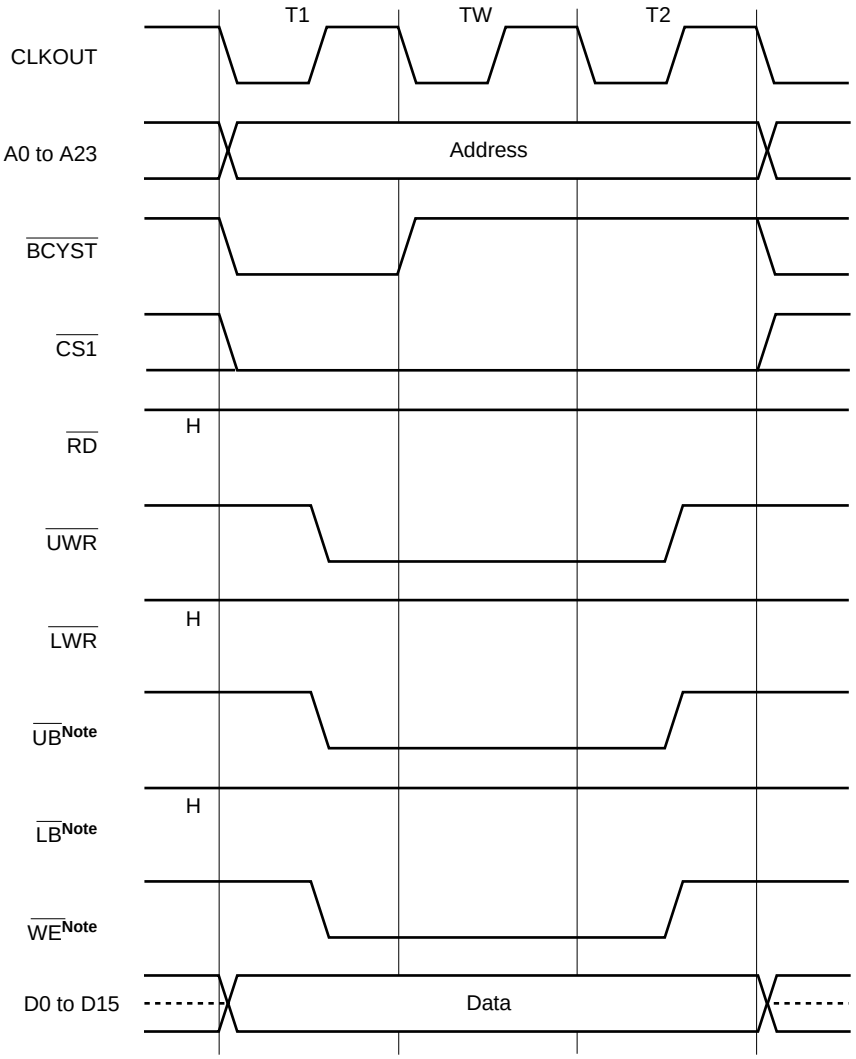
Figure 3-4. Write Operation in μPD431016LE-20 - 2 (Write in Byte Units to D0 to D7)



Note $\overline{UB}$, $\overline{LB}$, and $\overline{WE}$ are pins of the μPD431016.

Remark Broken lines indicate high impedance.

Figure 3-5. Write Operation in μPD431016LE-20 - 3 (Write in Byte Units to D8 to D15)



Note $\overline{UB}$, $\overline{LB}$, and $\overline{WE}$ are pins of the μPD431016.

Remark Broken lines indicate high impedance.

3.2 Connection with Slow PROM (27C1024-12)

In this circuit example, the V850E/MS1 uses one 27C1024 PROM (64 K × 16 bits, 120-ns access time) by using an external data bus buffer to connect to a 512-Kbyte external ROM space.

[Circuit configuration]

- V850E's internal system clock: 33 MHz
- Connected devices: HN27C1024H-12 × 1
- Memory usage: Memory block 0
  Assigned to address range 0000000H to 001FFFFH in external memory space (128-Kbyte space starting at address 0)

[Connection approach and caution points]

Since the HN27C1024H-12 has a large output floating delay time of 50 ns, a data bus buffer is inserted to prevent data contention that may occur when writing to another block after a read operation.

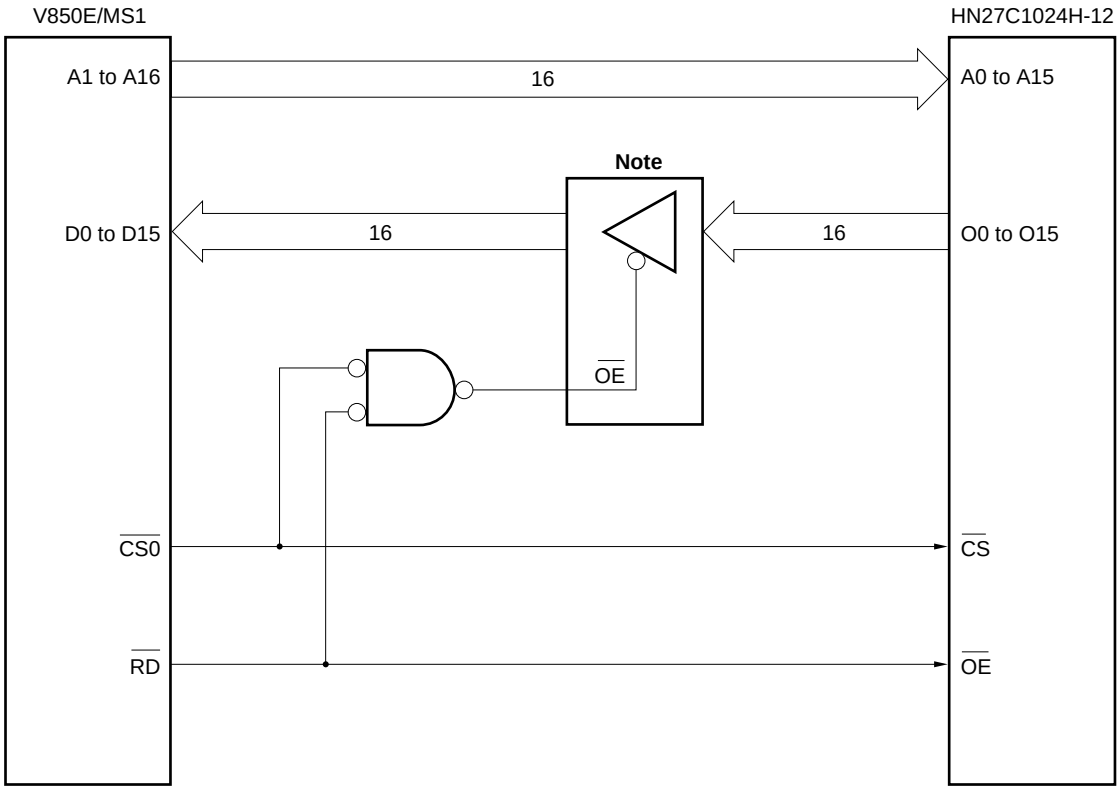
Caution Idle state insertion (1 clock) is not sufficient in this case.

[Register settings]

- Memory block 0: SRAM, external ROM, external I/O mode
- Wait setting: 4 wait cycles
- Idle state: Inserted

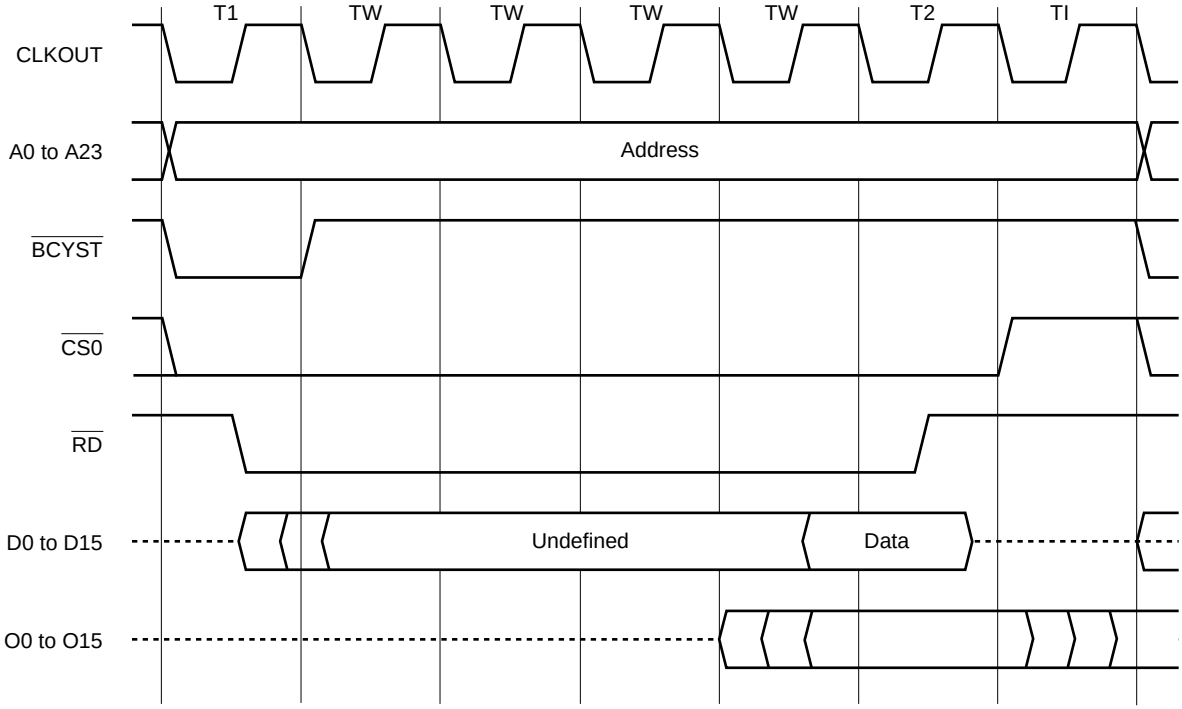
Register	Setting	Function
BCT	xxxxxxxxxxxxxx00B	Block 0: SRAM, external ROM, external I/O mode
BSC	xxxxxxxxxxxxxx01B	Block 0: 16 bits
DWC1	xxxxxxxxxxxxxx00B	Block 0: 4 waits
DWC2	xxxxxxx1B	
BCC	xxxxxxxxxxxxxx01B	Block 0: Idle is inserted

Figure 3-6. Circuit Example (Connection with HN27C1024H-12)



Note It is assumed that this is a 74xxx16244 circuit or its equivalent.

Figure 3-7. Read Operation in HN27C1024H-12



Remark Broken lines indicate high impedance.

3.3 Connection with SIMM (MC-428000A32)

The following are three examples of 32-Mbyte SIMM configurations (8 Mbytes × 32 bits) that include 4 banks using ports 00 and 01 in an 8-Mbyte address space (block 3).

(1) Circuit without a connected external bus master
(2) Circuit connected to an external bus master that does not access SIMM
(3) Circuit connected to an external bus master that accesses SIMM
(It is assumed that the external bus master is equipped with a SIMM-compliant interface such as one comprised of a gate array.)

[Circuit configuration]

- V850E's internal system clock: 33 MHz
- Connected devices: MC-428000A32-60 × 1
- Memory usage: Memory block 3
  Assigned to address range 0800000H to 0FFFFFFH in external memory space (8-Mbyte space starting at address 0800000H)
- Number of banks: 4 (using ports 00 and 01)

[Connection approach and caution points]

During the refresh cycle, all $\overline{\text{RAS}}$n signals are active so that all banks are refreshed. Since there is no $\overline{\text{OE}}$ pin in a 32-bit SIMM, the $\overline{\text{LCAS}}$ and $\overline{\text{UCAS}}$ signals must be held at their inactive level in relation to the SIMM when $\overline{\text{LWR}}$ and $\overline{\text{UWR}}$ are used for SRAM access during $\overline{\text{RAS}}$ active mode. The control method for this is to mask $\overline{\text{CAS}}$n, except when either $\overline{\text{OE}}$ or $\overline{\text{WE}}$ is output and during the refresh cycle.

Cautions

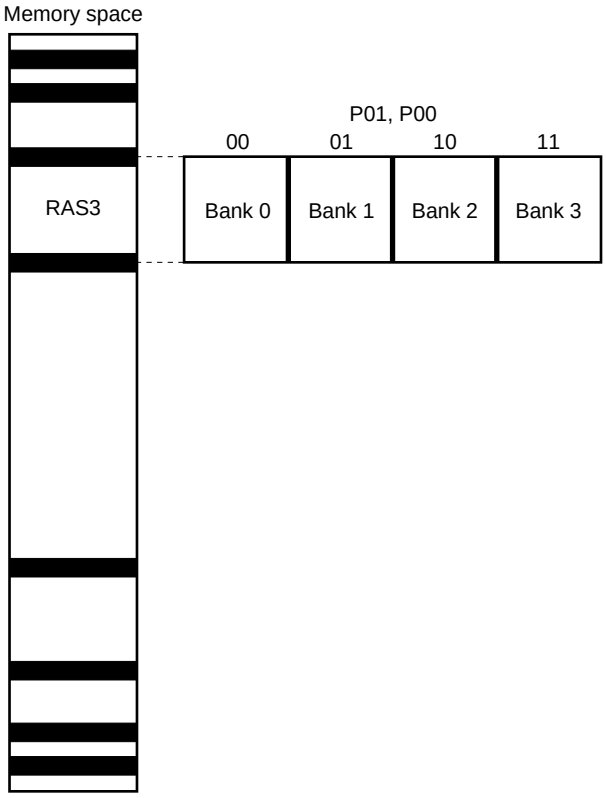
1. **When connecting to an external bus master, be sure that $\overline{\text{RAS}}$ is inactive during bus hold mode, before $\overline{\text{HLDRQ}}$ is set as inactive. If $\overline{\text{RAS}}$ is active until $\overline{\text{HLDAK}}$↑, a low-level pulse may be present in the SIMM's $\overline{\text{RAS}}$n via the $\overline{\text{HLDAK}}$↑ timing.**
2. **When connecting to an EDO DRAM 32-bit SIMM, $\overline{\text{OE}}$ is not controlled while RAS is active since there is no $\overline{\text{OE}}$ pin. Consequently, the DRAM should be set to RAS hold prohibit mode before use (to enable use of an EDO DRAM 32-bit SIMM in RAS hold enable mode, a bidirectional buffer must be used to prevent data bus control while accessing another block).**
3. **Since late write to DRAM is not supported in the SIMM, the $\overline{\text{WE}}$ signal must fall before $\overline{\text{CAS}}$n↓ occurs during write access.**
   Be sure to design the system's wire length, load, etc., so that the $\overline{\text{WE}}$ signal is not delayed.
4. **If read access (such as from the SDRAM) occurs immediately after read access from the SIMM, contention may occur between the SIMM's read data and the SRAM's read data, depending on the amount of delay time in the SIMM's control circuit. In such cases, a bidirectional buffer (controlled using $\overline{\text{OE}}$) must be set for the SIMM's data bus and the SIMM's $\overline{\text{CAS}}$n signal control is no needed.**

Bank switching during RAS hold mode

Perform the following steps.

<1> Set RAS hold mode prohibit status.
(Use RHD bit in DRC register)
<2> Perform a dummy read of the SIMM's memory block.
<3> Perform port access for bank switching.
(Read/modify/write)
<4> Set RAS hold mode enable status.
(Use RHD bit in DRC register)

Remark Be sure to read before write when performing port access for bank switching. A bit manipulation instruction can also be used.



[Register settings]

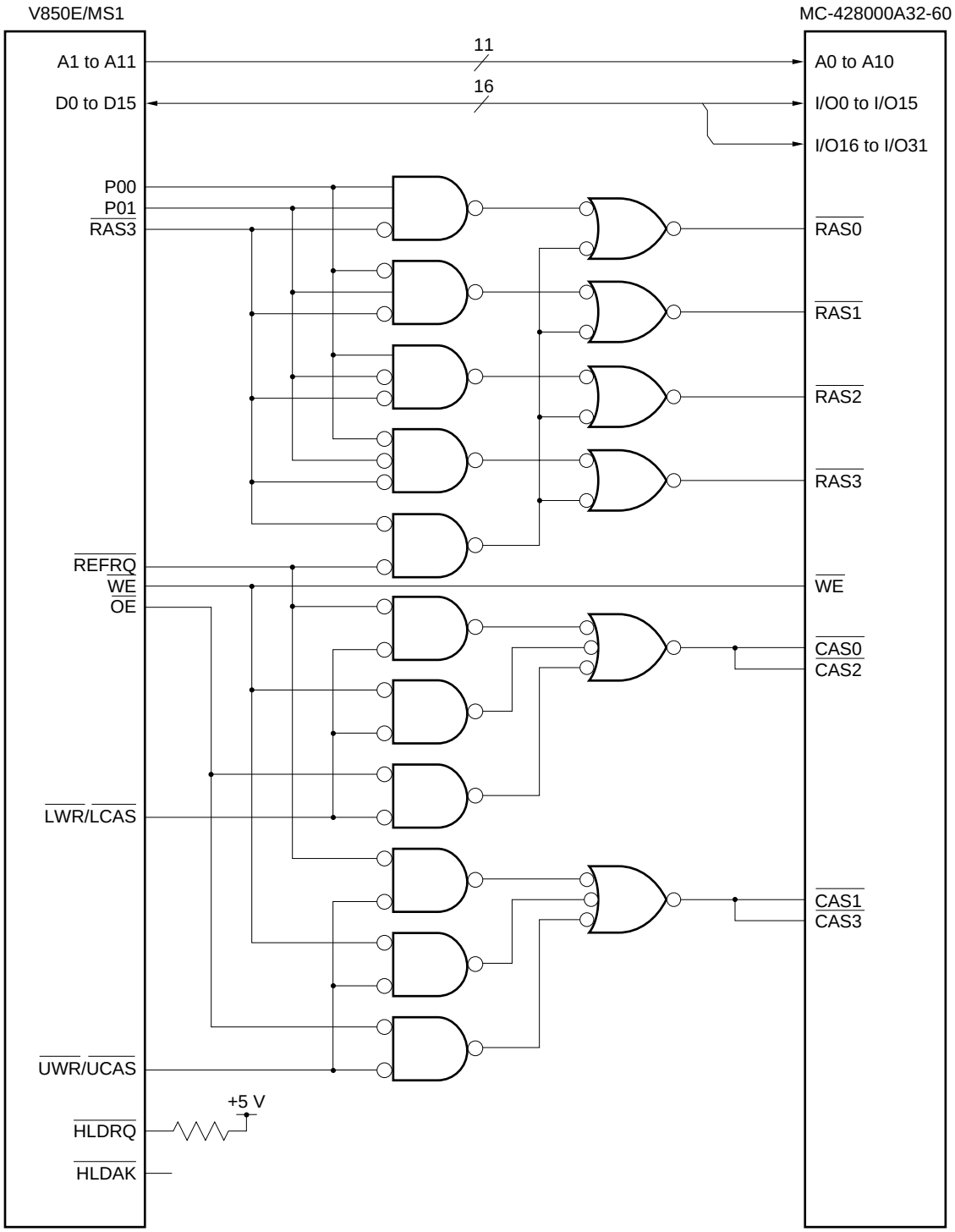
- Memory block 3: DRAM mode
- Specified DRAM configuration register: DRC2
- DRAM type: Fast page DRAM
- RAS hold mode: Enabled
- Idle state: Inserted

Register	Setting	Function
BCT	xxxxxxxx10xxxxxxB	Block 3: Specified in DRAM
BSC	xxxxxxxx01xxxxxxB	Block 3: 16 bits
BCC	xxxxxxxx01xxxxxxB	Block 3: Idle is inserted
DRC2	6503H	Fast page DRAM RPW = 2, RHW = 1, DAW = 1, CPW = 0, RHD = 0[Note] Address multiplex width = 11 bits
DTC	xxxxxxxx10xxxxxxB	Block 3: DRC2
RFC2	800FH	Refresh enabled, refresh interval: $32/\phi \times 16$
RWC	40H	RRW = 1, RCW = 0, SRW = 0

Note Be sure to set RAS hold mode prohibit status during bank switching.

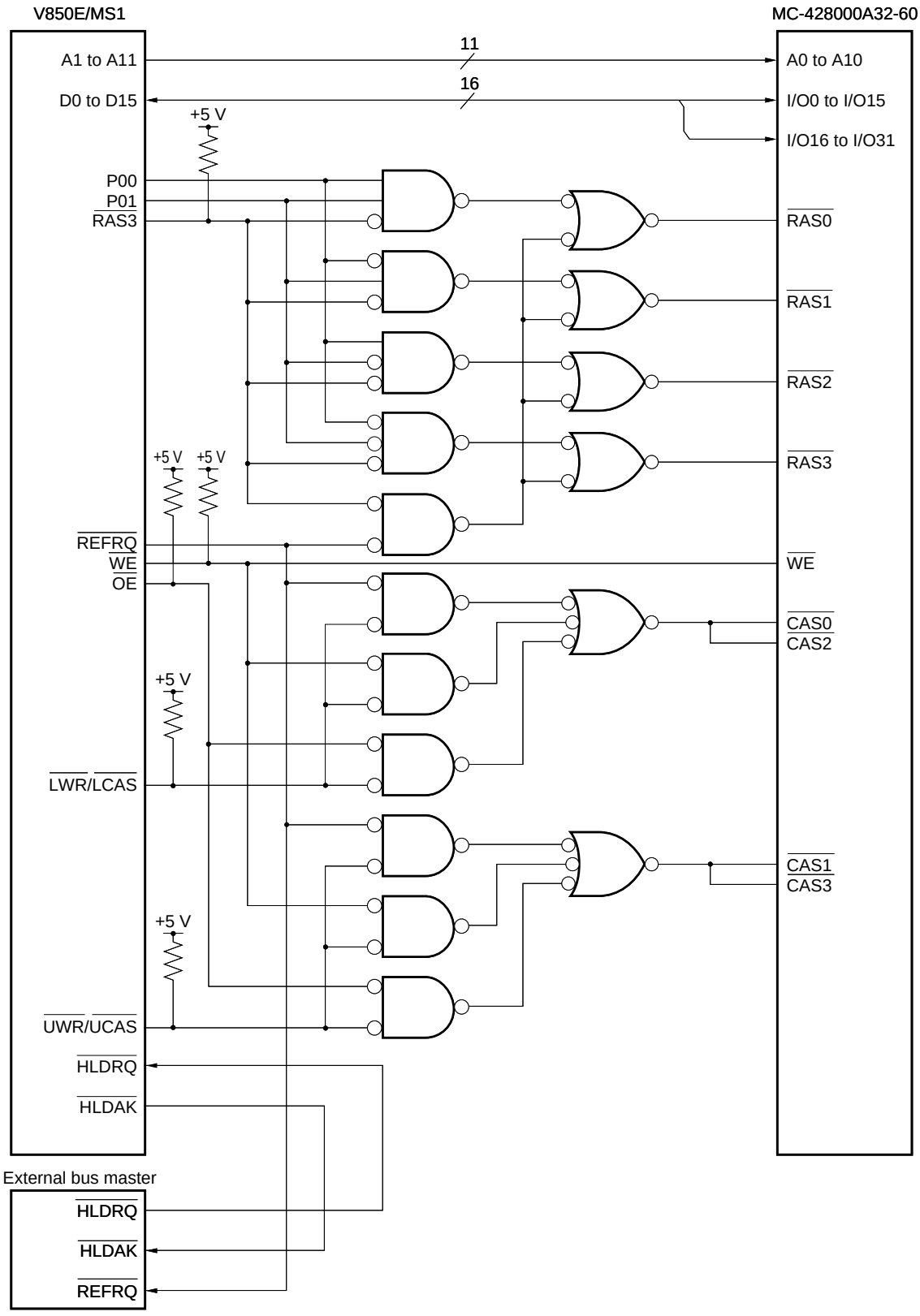
(1) Example of circuit without a connected external bus master

Figure 3-8. Example of Circuit without Connected External Bus Master



(2) Example of circuit with a connected external bus master

Figure 3-9. Example of Circuit with Connected External Bus Master



(3) Example of circuit with external bus master connected for SIMM access

Figure 3-10. Example of Circuit with External Bus Master Connected for SIMM Access

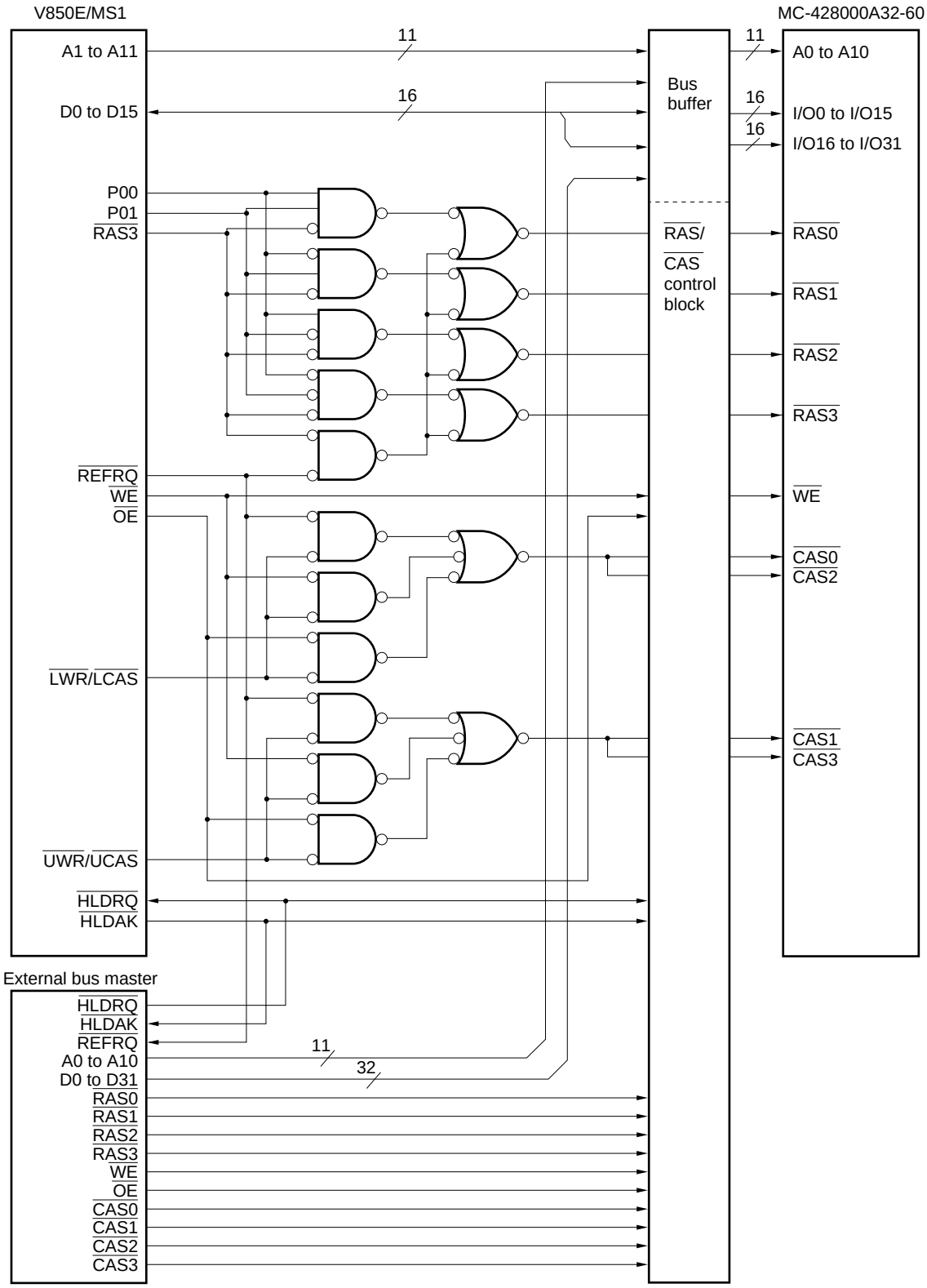


Figure 3-11. Detailed View of Bus Buffer

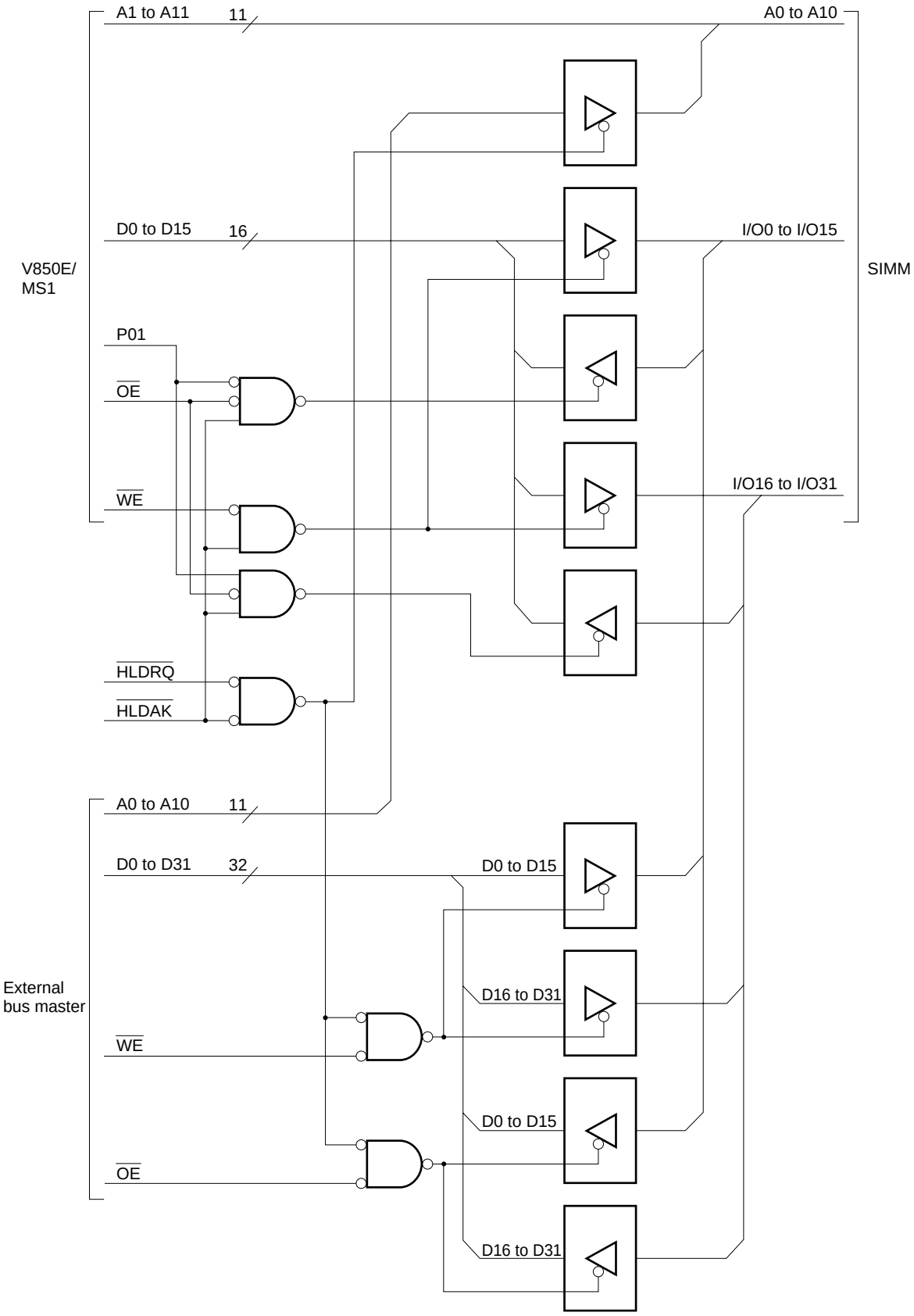


Figure 3-12. RAS/CAS Control Block

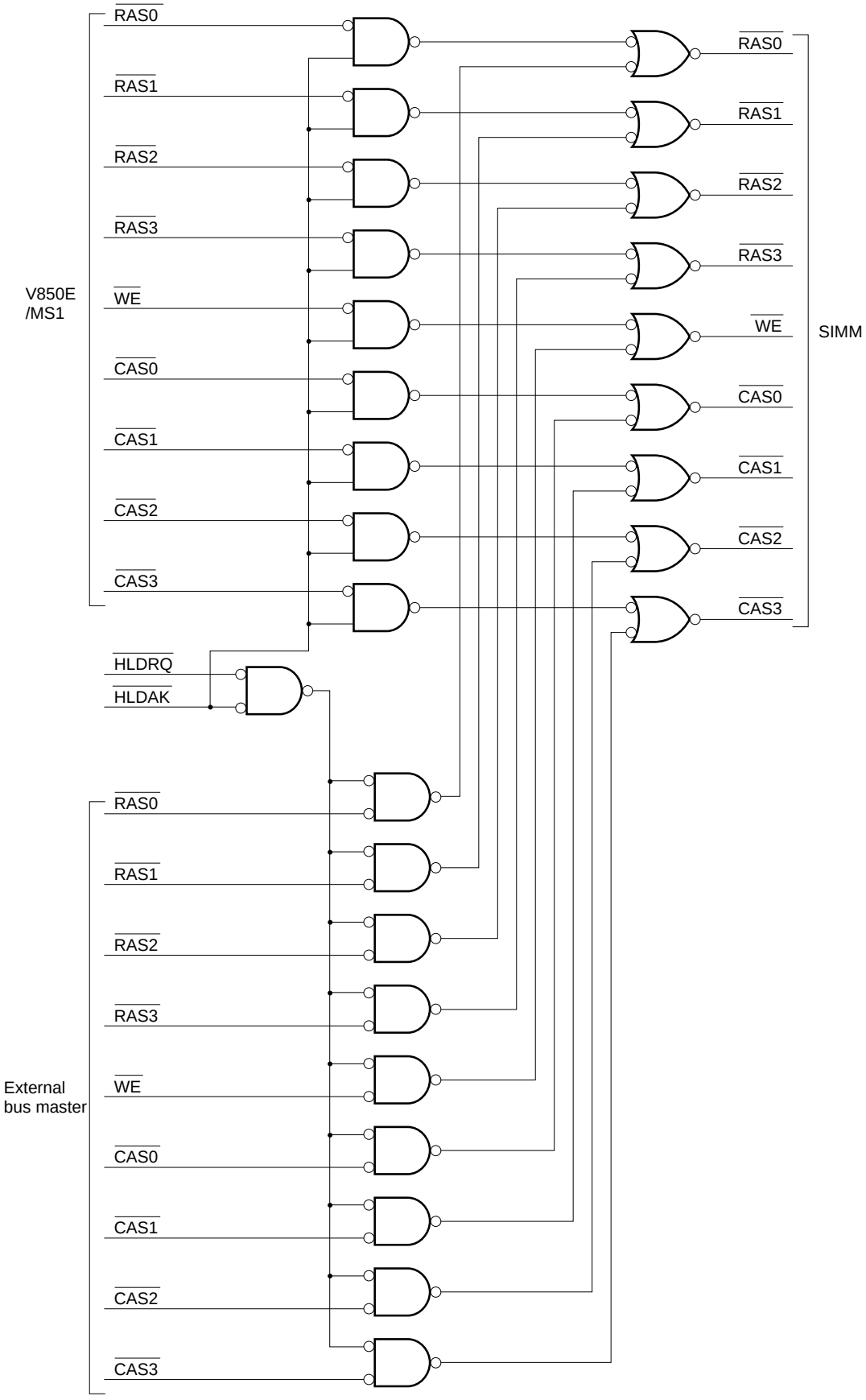
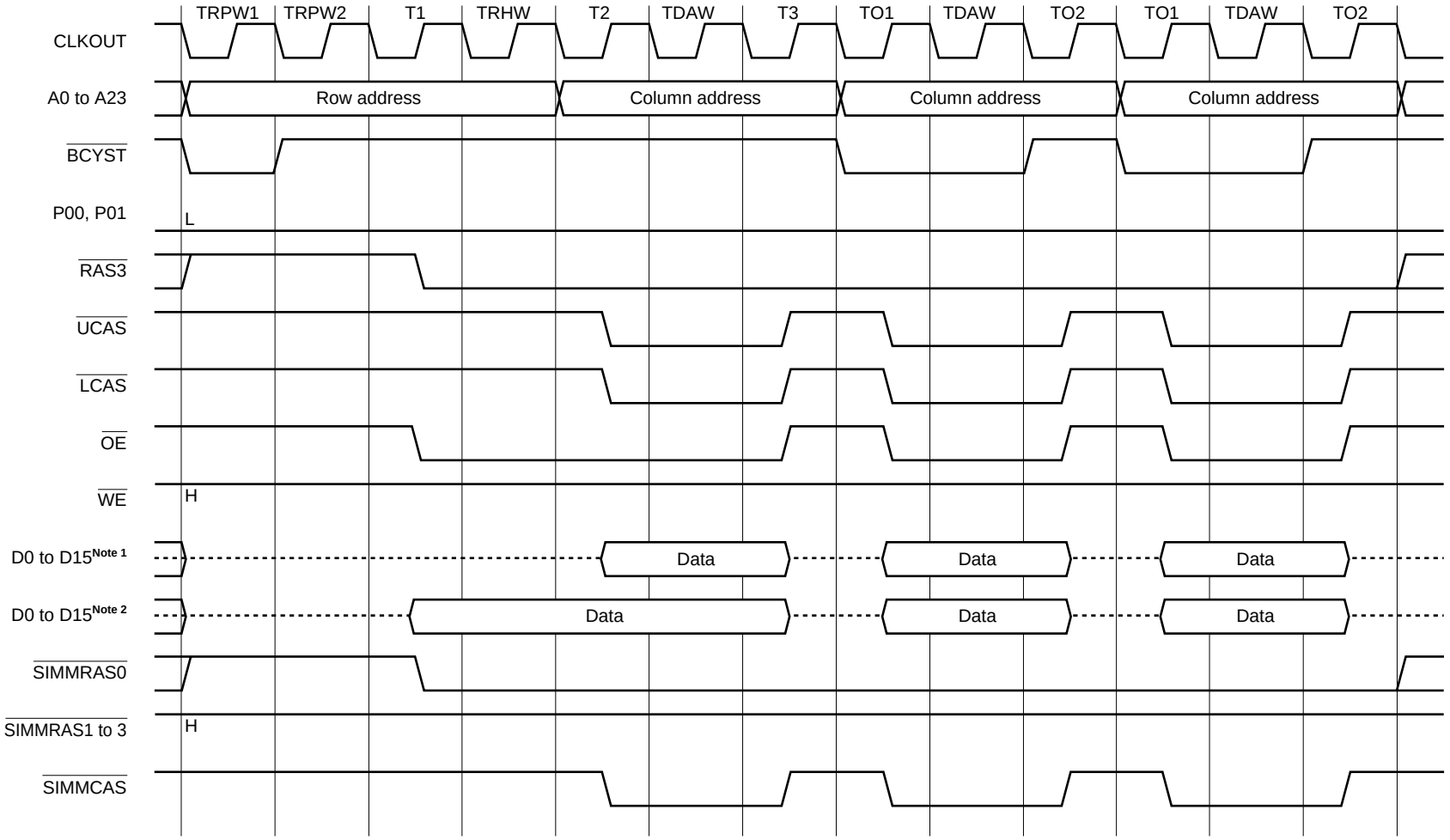


Figure 3-13. Read Operation in MC-428000A32-60

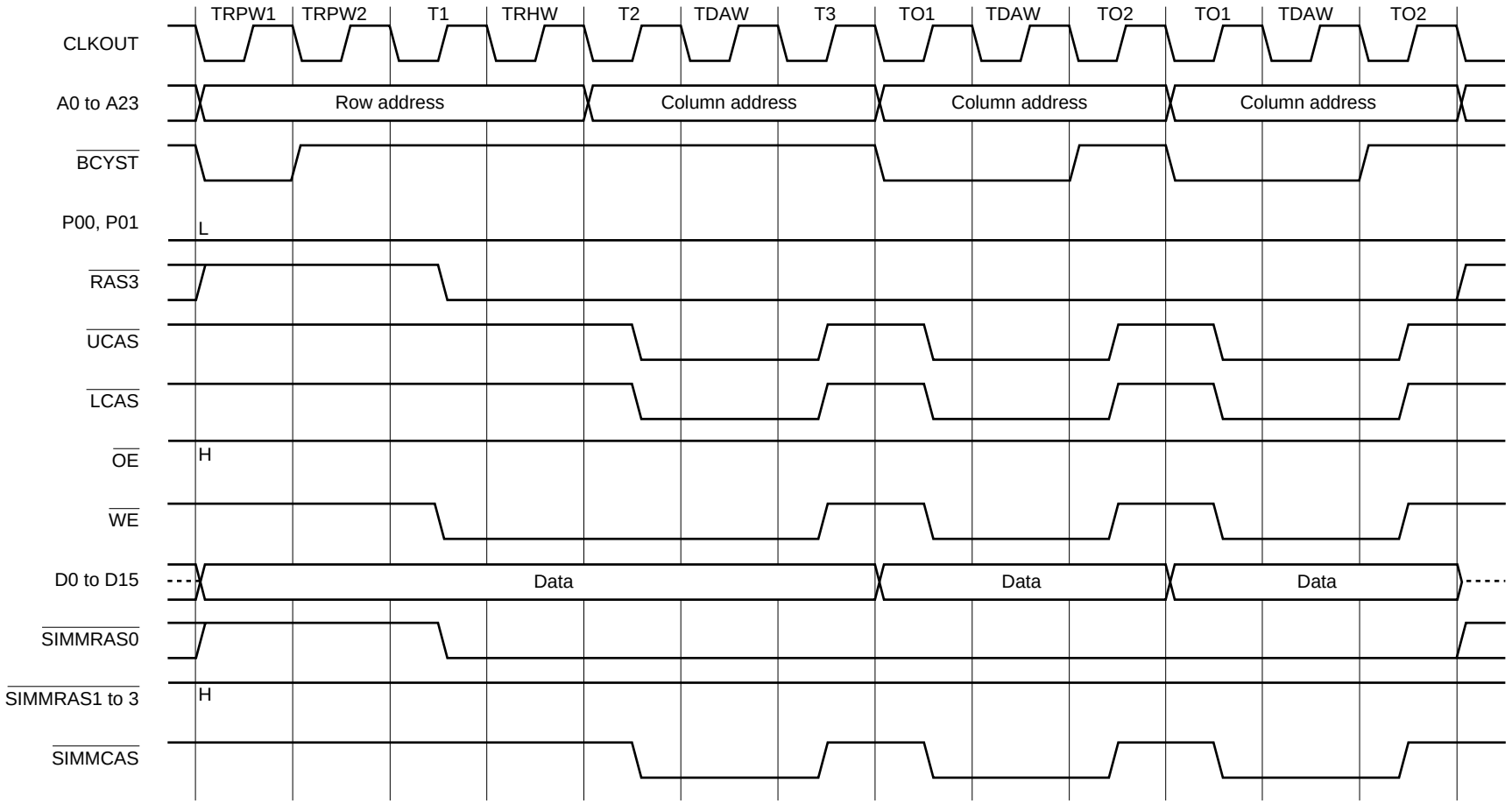


Notes 1 See **Figure 3-8. Example of Circuit without Connected External Bus Master** and **Figure 3-9. Example of Circuit with Connected External Bus Master**.

2. See **Figure 3-10. Example of Circuit with External Bus Master Connected for SIMM Access**.

Remark Broken lines indicate high impedance.

Figure 3-14. Write Operation in MC-428000A32-60



Remark Broken lines indicate high impedance.

3.4 Connection with DIMM (MC-422000AA64)

The followings are examples of 16-Mbyte DIMM configurations (2 Mbytes (64 bits) that include 8 banks using ports 00, 01, and 02 in a 2-Mbyte address space (block 6).

The timing is the same as when connection with a SIMM (see **3.3 Connection with SIMM MC-428000A32**).

[Circuit configuration]

- V850E's internal system clock: 33 MHz
- Connected devices: MC-422000AA64-60 × 1
- Memory usage: Memory block 6
  Assigned to address range 03C00000H to 03DFFFFFH in external memory space (2-Mbyte space starting at address 03C00000H)
- Number of banks: 8 (using ports 00, 01, and 02)

[Connection approach and caution points]

This is an 8-bank configuration that uses ports 00, 01, and 02. It is the same as the SIMM connection except for its bank configuration (see **3.3 Connection with SIMM (MC-428000A32**).

V850E/MS1 pin	DIMM pins controlled with banks							
P02, P01, P00	Bank 0 000	Bank 1 001	Bank 2 010	Bank 3 011	Bank 4 100	Bank 5 101	Bank 6 110	Bank 7 111
$\overline{\text{RAS6}}$	$\overline{\text{RAS0}}$	$\overline{\text{RAS0}}$	$\overline{\text{RAS1}}$	$\overline{\text{RAS1}}$	$\overline{\text{RAS2}}$	$\overline{\text{RAS2}}$	$\overline{\text{RAS3}}$	$\overline{\text{RAS3}}$
$\overline{\text{LCAS}}$	$\overline{\text{CAS0}}$	$\overline{\text{CAS2}}$	$\overline{\text{CAS0}}$	$\overline{\text{CAS2}}$	$\overline{\text{CAS4}}$	$\overline{\text{CAS6}}$	$\overline{\text{CAS4}}$	$\overline{\text{CAS6}}$
$\overline{\text{UCAS}}$	$\overline{\text{CAS1}}$	$\overline{\text{CAS3}}$	$\overline{\text{CAS1}}$	$\overline{\text{CAS3}}$	$\overline{\text{CAS5}}$	$\overline{\text{CAS7}}$	$\overline{\text{CAS5}}$	$\overline{\text{CAS7}}$

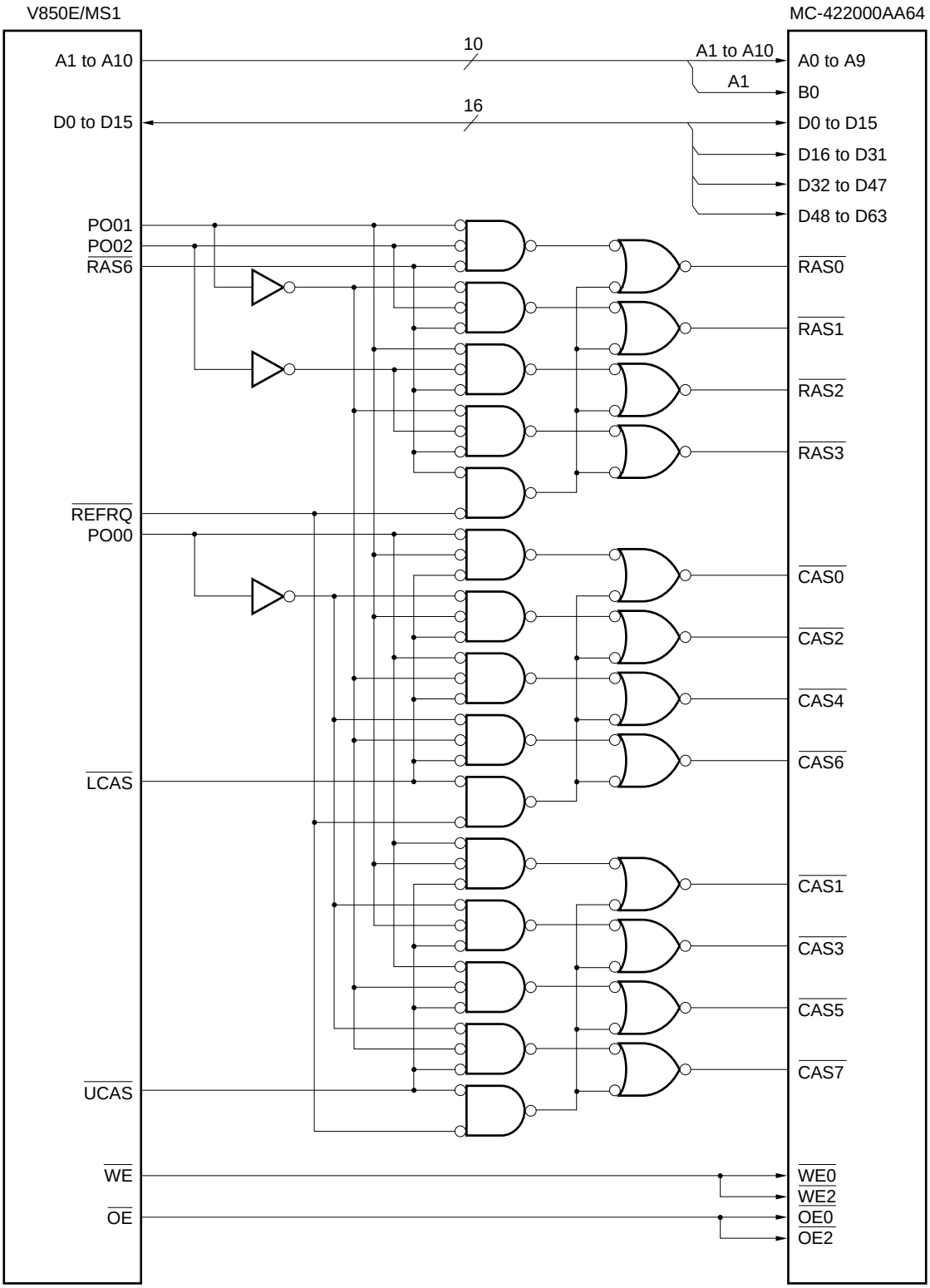
[Register settings]

- Memory block 5: DRAM mode
- Specified DRAM configuration register: DRC3
- DRAM type: Fast page DRAM
- RAS hold mode: Enabled
- Idle state: Inserted

Register	Setting	Function
BCT	xx10xxxxxxxxxxxB	Block 6: Specified in DRAM
BSC	xx01xxxxxxxxxxxB	Block 6: 16 bits
BCC	xx01xxxxxxxxxxxB	Block 6: Idle is inserted
DRC3	6502H	Fast page DRAM RPW = 2, RHW = 1, DAW = 1, CPW = 0, RHD = 0[Note] Address multiplex width = 10 bits
DTC	xx11xxxxxxxxxxxB	Block 6: DRC3
RFC3	800FH	Refresh enabled, refresh interval: 32/ϕ × 16
RWC	40H	RRW = 1, RCW = 0, SRW = 0

Note Be sure to set RAS hold mode prohibit status during bank switching.

Figure 3-15. Circuit Example (Connection with MC-422000AA64)



3.5 Connection with Communication/Printer IC

In the following example, one TL16C552A communication/printer IC is used to connect with the V850E in the block 6 space.

[Circuit configuration]

- V850E's internal system clock: 3 MHz
- Connected devices: TL16C552A × 1
- Memory usage: Memory block 6
  Assigned to address range 03C00000H to 03C0003FH in external memory space

[Connection approach and caution points]

Use the following approach when connecting the TL16C552A's pins.

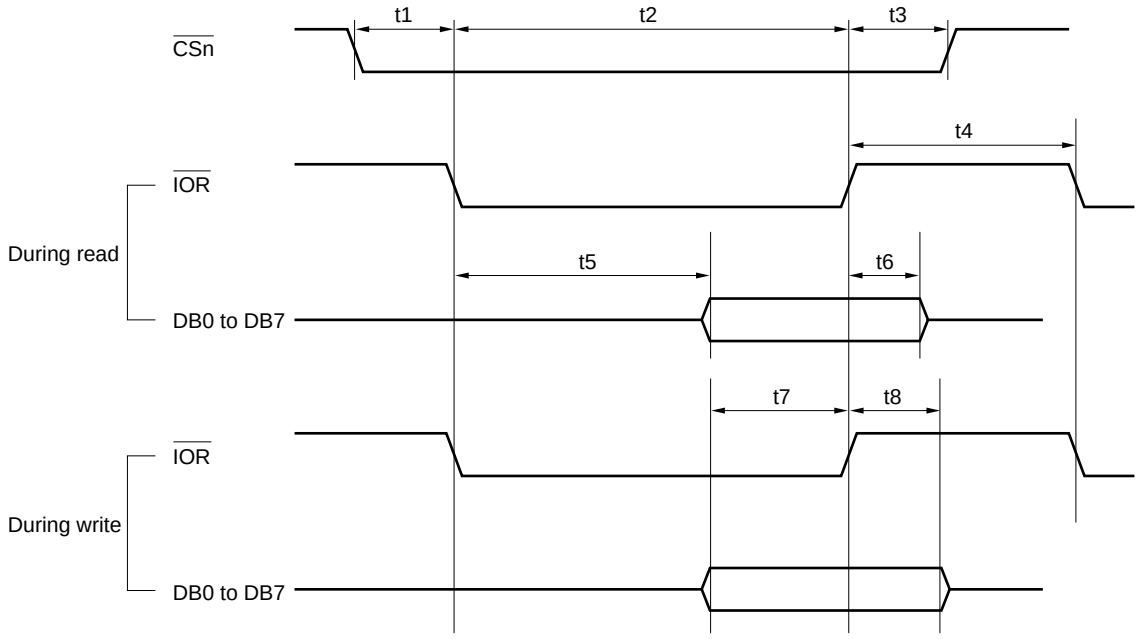
<1> DB0 to DB7 are connected via a data bus buffer to D0 to D7 in the V850E/MS1. The read data is latched (only byte access for even-numbered addresses is valid when accessing the TL16C552A).

<2> The three select signals ($\overline{CS0}$ to $\overline{CS2}$) are generated by decoding $\overline{CS6}$, A4, and A5 in the V850E/MS1.

V850E/MS1			TL16C552A		
$\overline{CS6}$	A5	A4	$\overline{CS0}$	$\overline{CS1}$	$\overline{CS2}$
L	L	L	L	H	H
L	L	H	H	L	H
L	H	L	H	H	L
L	H	H	H	H	H
H	×	×	H	H	H

<3> To comply with standards for the time between when the $\overline{CSn}$ signal goes active to when the $\overline{IOR}$ (or $\overline{IOW}$) signal goes active and the hold time between when the $\overline{IOR}$ (or $\overline{IOW}$) signal goes inactive to when the $\overline{CSn}$ signal goes inactive, $\overline{IOR}$ and $\overline{IOW}$ signals are generated using the CLKOUT signal instead of directly connecting the V850E/MS1's $\overline{RD}$ and $\overline{LWR}$ signals.

Figure 3-16. Timing of TL16C552A (Excerpted)



t1: IOR, IOW hold time = 15 ns (Min.)
t2: IOR, IOW pulse width = 80 ns (Min.)
t3: CS hold time = 20 ns (Min.)
t4: Read/write recovery time = 80 ns (Min.)
t5: Data output delay time = 60 ns (Max.)
t6: Output floating delay time = 60 ns (Max.)
t7: Data setup time = 15 ns (Min.)
t8: Data hold time = 15 ns (Min.)

Caution Avoid continuous access to protect the read/write recovery time (t4).

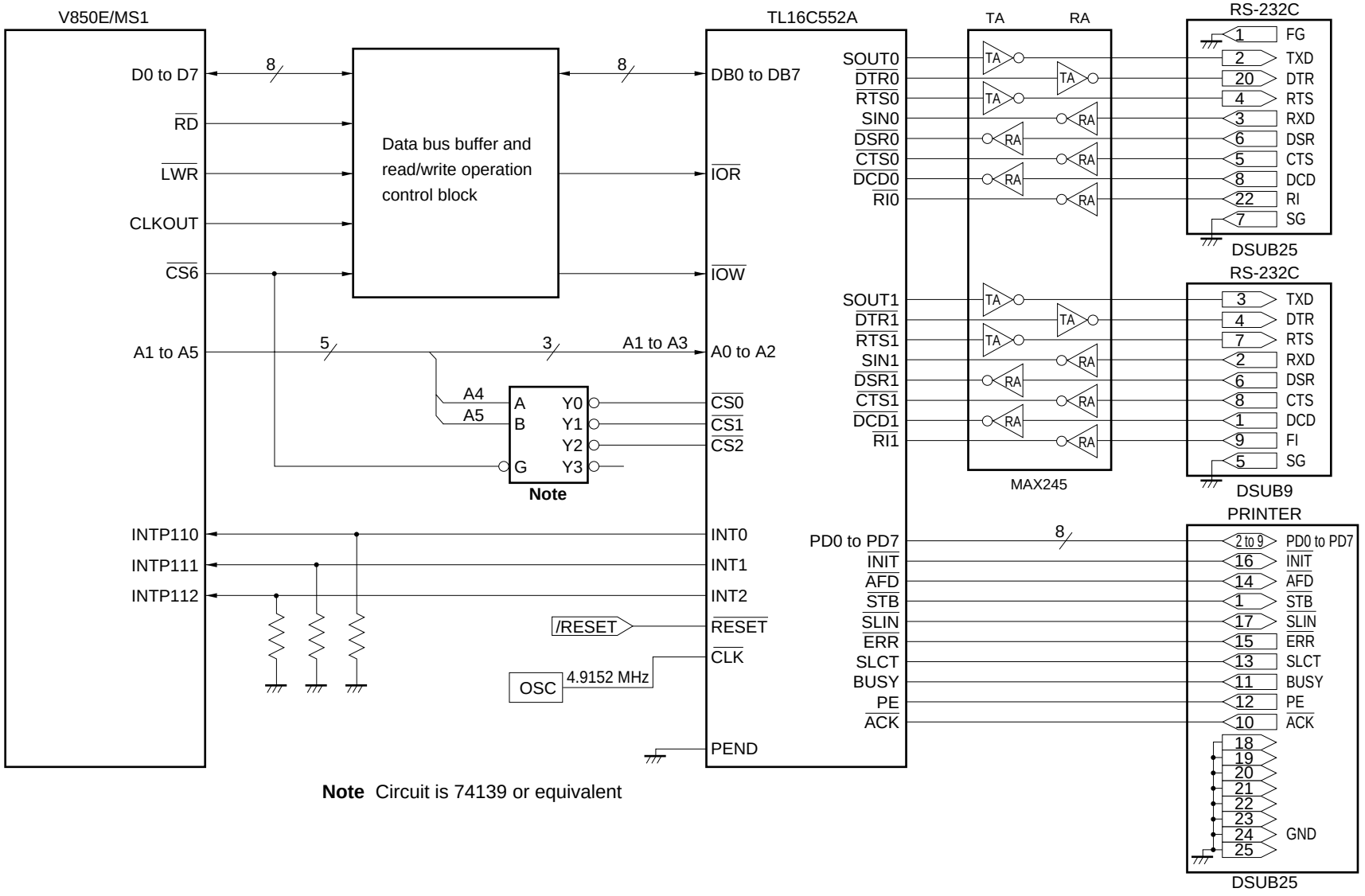
[Register settings]

- Memory block 6: SDRAM, external ROM, external I/O mode
- Wait setting: 4 waits
- Idle state: Not inserted

Register	Setting	Function
BCT	xx00xxxxxxxxxxxB	Block 6: SDRAM, external ROM, external I/O mode
BSC	xx00xxxxxxxxxxxB	Block 6: 8 bits[Note]
DWC1	xx00xxxxxxxxxxxB	Block 6: 4 waits
DWC2	x1xxxxxxB	
BCC	xx00xxxxB	Block 6: Idle is not inserted

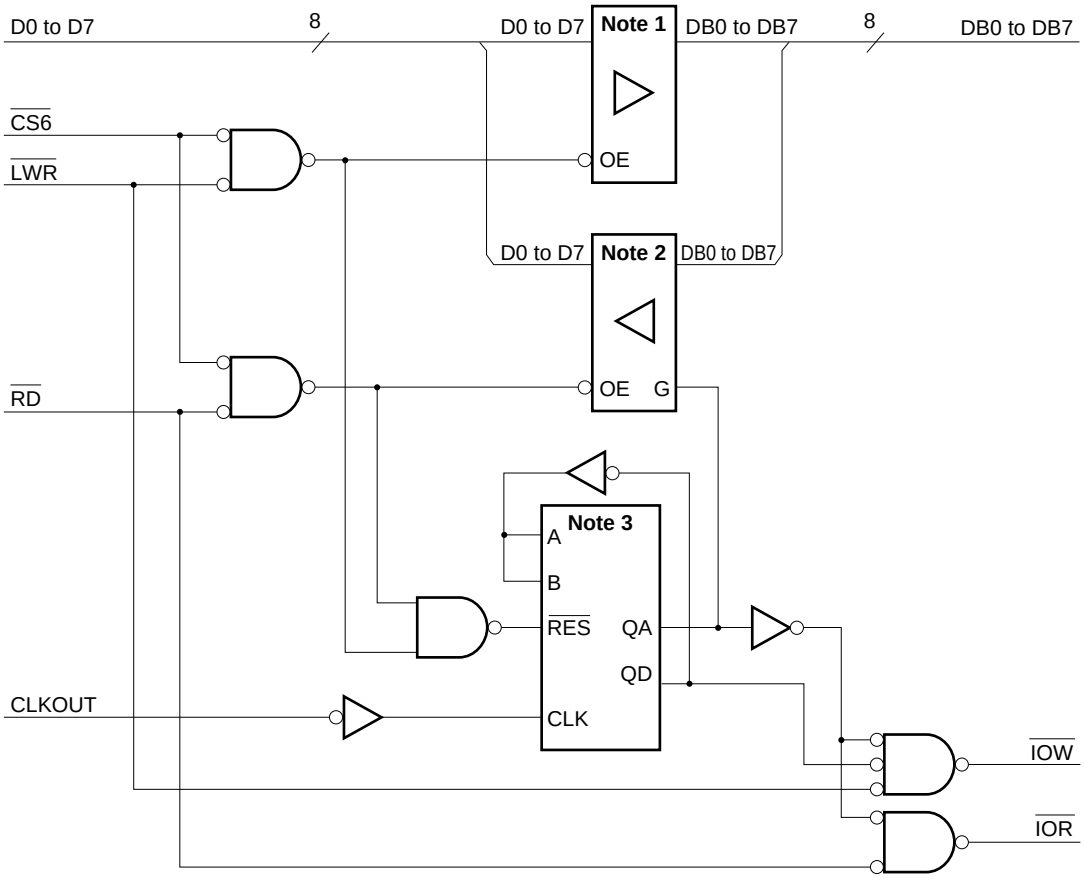
Note Since only byte-unit access for even-numbered addresses is valid, there is no problem with a 16-bit setting.

Figure 3-17. TL16C552A Circuit Connection Example



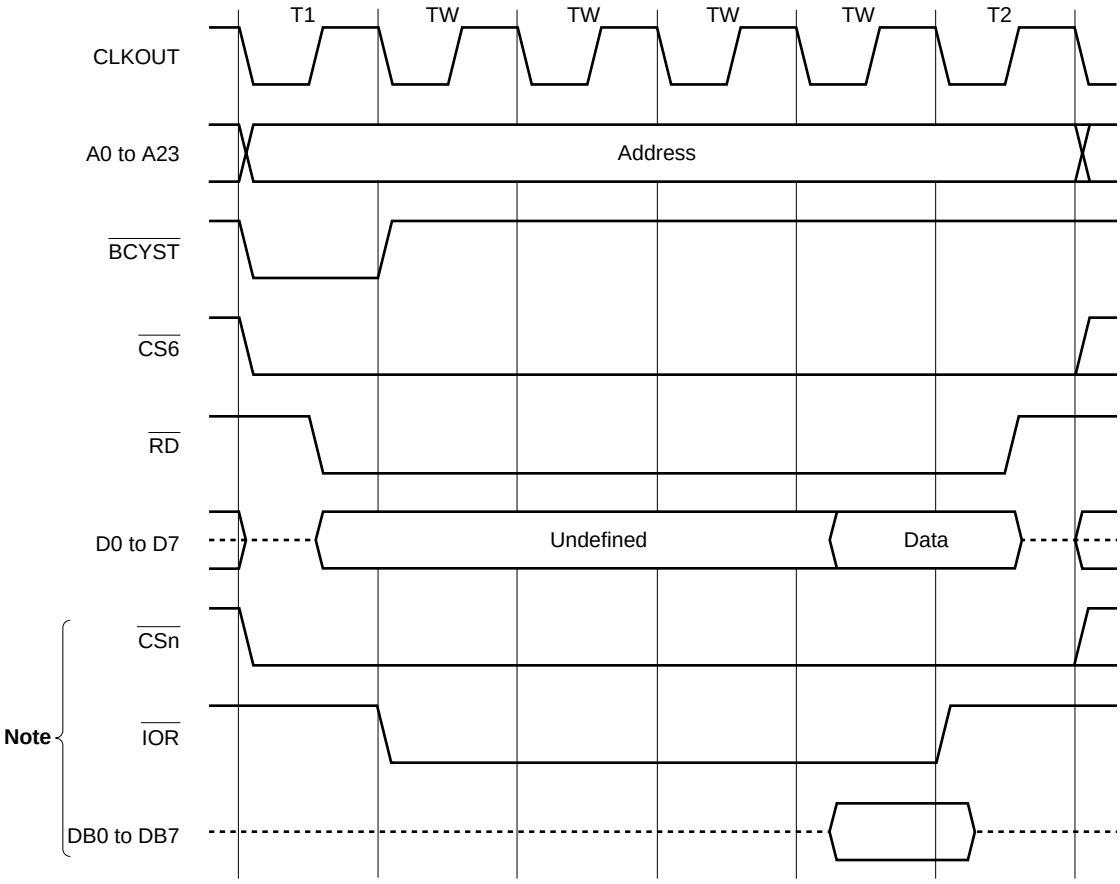
Note Circuit is 74139 or equivalent

Figure 3-18. Detailed View of Data Bus Buffer and Read/Write Operation Control Block



Notes **1.** Circuit is 74244 or equivalent
2. Circuit is 74373 or equivalent
3. Circuit is 74164 or equivalent

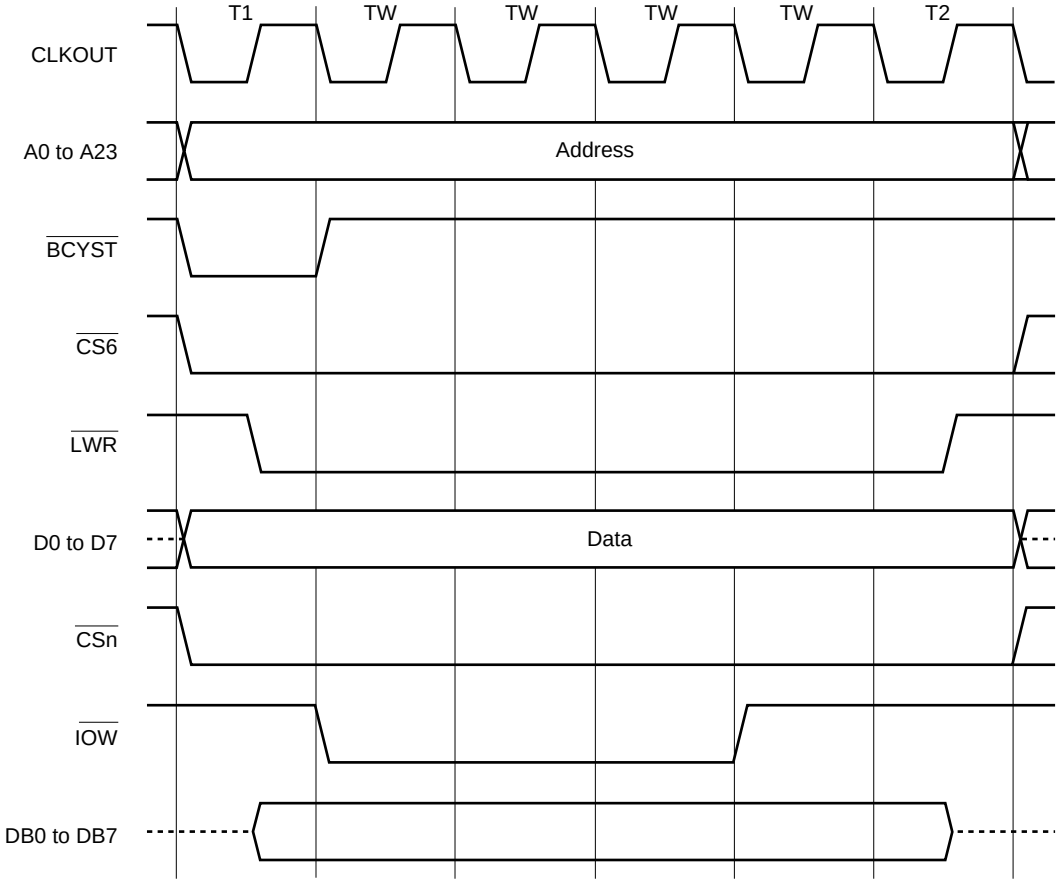
Figure 3-19. Read Operation in TL16C552A



Note This is a TL16C552A signal.

Remark Broken lines indicate high impedance.

Figure 3-20. Write Operation in TL16C552A



Remark Broken lines indicate high impedance.

CHAPTER 4 APPLICATION EXAMPLES

This chapter describes functions, circuits, and program examples related to the TB-V850E CPU board that integrates the V850E/MS1.

4.1 Functions of TB-V850E

4.1.1 General

The TB-V850E is a training board that has been developed as a tool for evaluating and studying the V850E/MS1 32-bit single-chip microcontroller.

The TB-V850E's features are described below.

(1) Enables use of V850E/MS1 with V_{DD} 3.3-V or HV_{DD} 5-V power supply

(2) Bus operations can be observed using a logic analyzer
All signals related to the bus interface can be assigned to logic analyzer connectors.

(3) Supports 40-MHz (maximum) operation
Two oscillators (slow and fast) are available and the supplied clock can be selected via jumper switch settings. Also, since the two oscillators are both mounted on a socket, their supplied clock can also be changed (the slower clock is used when observing operations via a logic analyzer).

(4) Equipped with various types of memory
- EPROM
- SRAM
- Fast page DRAM
- EDO DRAM
- Page ROM

(5) Serial interface
RS-232C × 3 channels
(Connects to on-chip UART1 in V850E/MS1)

(6) Includes flash memory programmer interface for internal flash memory
Connects to on-chip CSIO in V850E/MS1

(7) Analog input
Connects to output from sine-wave generator
Connects to analog output (0 V to 5V)
Connects to analog output of optical sensor

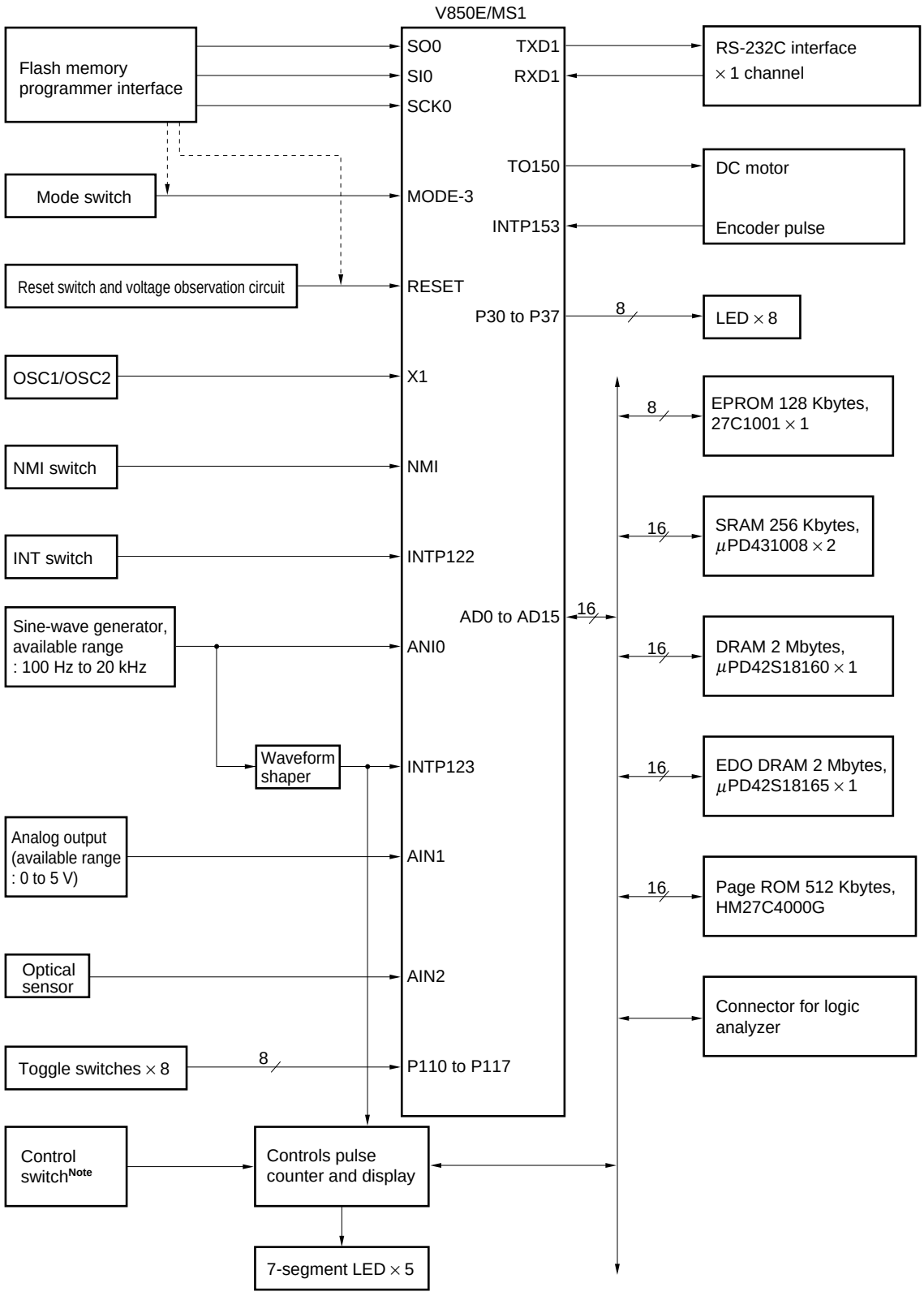
(8) General-purpose switch inputs (8) and LED outputs (8)
Uses V850E/MS1's on-chip PIO

(9) 7-segment LEDs (5 digits)
A switch is used to select between software control and hardware control for the LED display. The display shows the frequency of output from the sine-wave generator when hardware control has been selected.

(10) Includes DC motor with rotary encoder output
TM15 in the V850E/MS1's on-chip RPU is used to control the motor's speed.
The rotary encoder's output is connected to the INTP153 pin.

4.1.2 Board configuration diagram

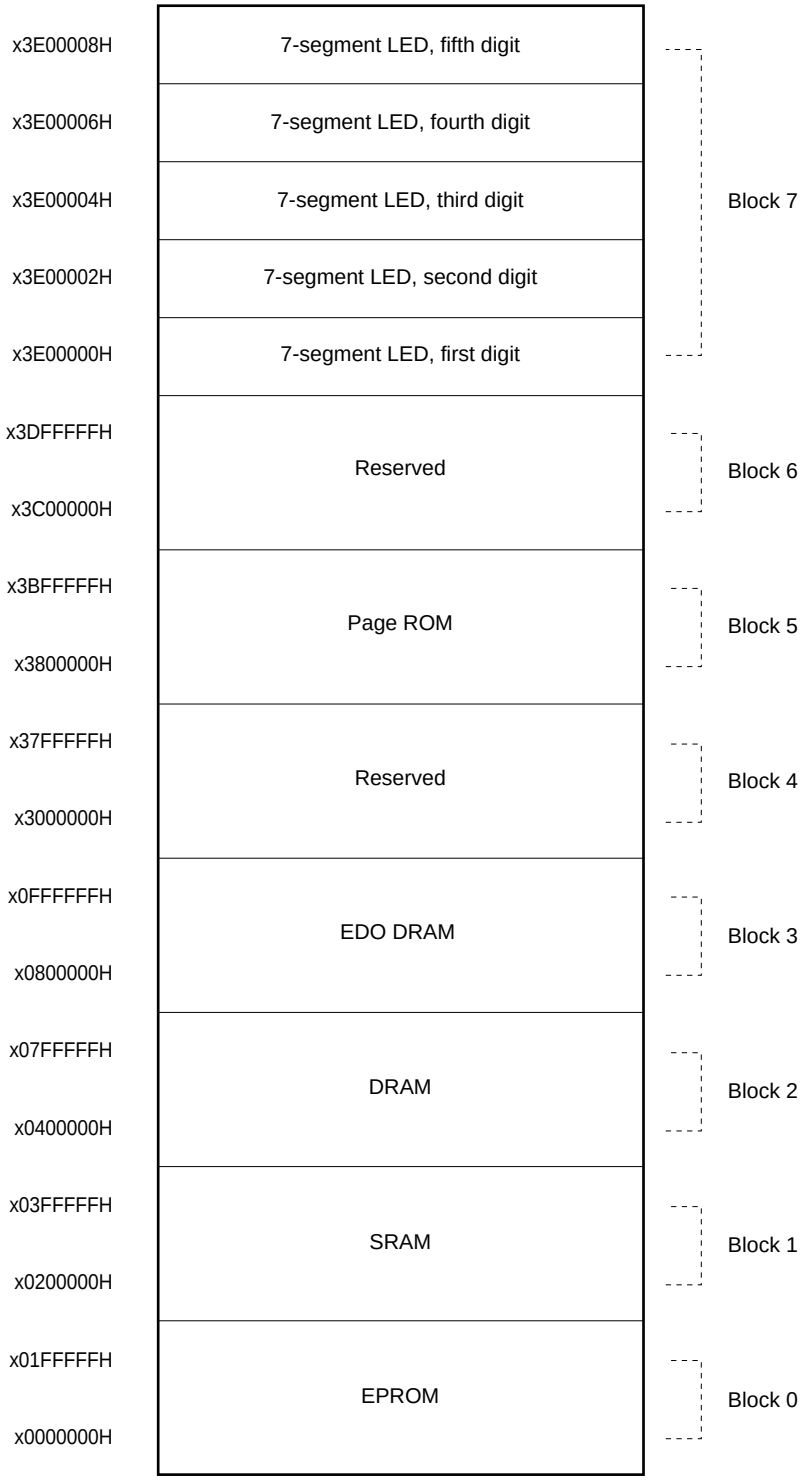
Figure 4-1. TB-V850E Board Configuration Diagram



Note This control switch is used to switch between hardware control and software control.

4.1.3 Memory map

Figure 4-2. Memory Map of TB-V850E



4.1.4 External bus interface connection

The V850E/MS1's external bus interface connects with an EPROM, SRAM, fast page DRAM, EDO DRAM, page ROM, and 7-segment LED. The V850E/MS1's BCU is used to implement wait control. Among the memory devices, the EPROM has an 8-bit bus width and all of the others have a 16-bit bus width. The 7-segment LED also has an 8-bit bus width.

EPROM:

A 32-pin socket that supports implementing of a 1-Mbit (128 K × 8 bits) EPROM (27C1001 or equivalent memory) is implemented in block 0. Access this space using an 8-bit bus width.

SRAM:

Two 1-Mbit (128 K × 8 bits) high-speed SRAMs (μPD431008) are implemented in block 1.

Fast page DRAM:

A 16-Mbit (1 M × 16 bits) fast page DRAM (μPD42S18160) is implemented in block 2. Refresh cycles are controlled by the V850E/MS1's BCU.

EDO DRAM:

A 16-Mbit (1 M × 16 bits) EDO DRAM (μPD42S18165) is implemented in block 3. Refresh cycles are controlled by the V850E/MS1's BCU.

Page ROM:

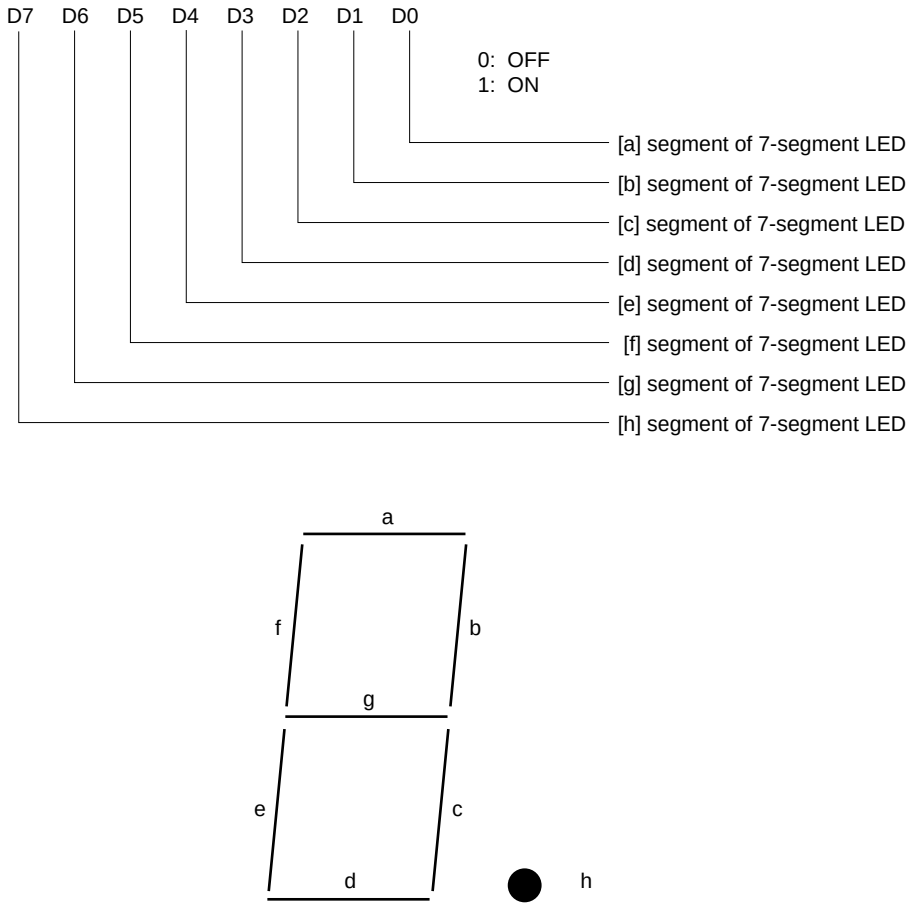
A 40-pin socket that supports implementing of a burst access-enabled 4-Mbit (256 K × 16 bits) EPROM (27C4000G) is implemented in block 5.

7-segment LED:

Five 7-segment LEDs are implemented in block 7. Only byte-unit writing access for even-numbered addresses is valid. If it is read, the read data is undefined. The address and data bus transition for each LED is listed below.

Address: x3E00000H First digit (write/byte)
Address: x3E00002H Second digit (write/byte)
Address: x3E00004H Third digit (write/byte)
Address: x3E00006H Fourth digit (write/byte)
Address: x3E00008H Fifth digit (write/byte)

Figure 4-3. 7-Segment LED



4.1.5 Connection of external interrupt input pins

An NMI pin and three maskable interrupt pins are connected.

Table 4-1. Interrupt Sources and Valid Edge Specifications

Interrupt	Interrupt source	Valid edge specification
NMI	NMI switch	Falling edge
INTP122	INT switch	Falling edge
INTP123	Sine-wave interrupt	Rising edge
INTP153	Pulse generator output interrupt	Rising edge

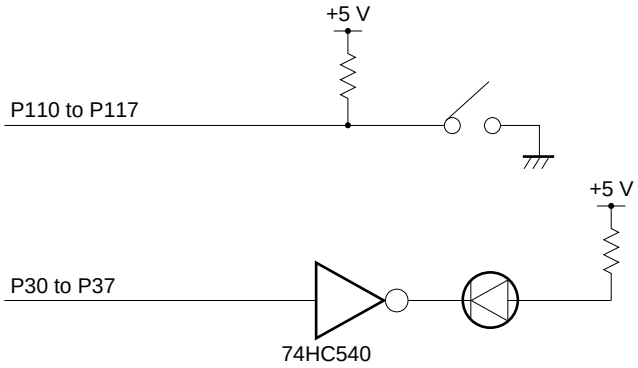
4.1.6 Port function connections

P110 to P117 are used as input ports and P30 to P37 are used as output ports. The input ports are connected to toggle switches and the output ports are connected to LEDs.

Table 4-2. List of I/O Ports Being Used

Port	I/O	Use
P110	I	General-purpose toggle switch 0
P111	I	General-purpose toggle switch 1
P112	I	General-purpose toggle switch 2
P113	I	General-purpose toggle switch 3
P114	I	General-purpose toggle switch 4
P115	I	General-purpose toggle switch 5
P116	I	General-purpose toggle switch 6
P117	I	General-purpose toggle switch 7
P30	O	General-purpose LED0 (lights when set to “1”)
P31	O	General-purpose LED1 (lights when set to “1”)
P32	O	General-purpose LED2 (lights when set to “1”)
P33	O	General-purpose LED3 (lights when set to “1”)
P34	O	General-purpose LED4 (lights when set to “1”)
P35	O	General-purpose LED5 (lights when set to “1”)
P36	O	General-purpose LED6 (lights when set to “1”)
P37	O	General-purpose LED7 (lights when set to “1”)

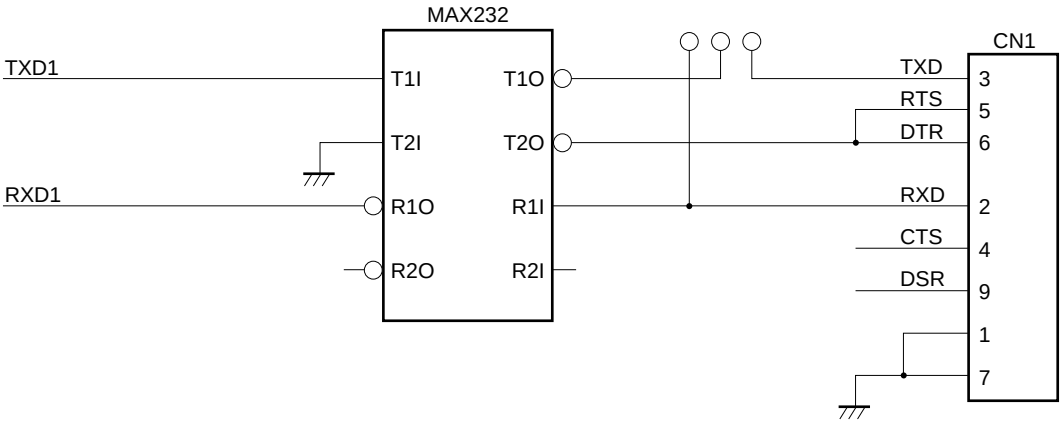
Figure 4-4. Port-Connected Circuit Example



4.1.7 Connection of UART

UART1 is used as an asynchronous RS-232C interface. Signals follow a two-wire system (TXD and RXD). The RTS and DTS signals (modem control signals) are fixed at the active level and the CTS and DSR signals are not connected. The TXD and RXD signals are looped back by jumper switches.

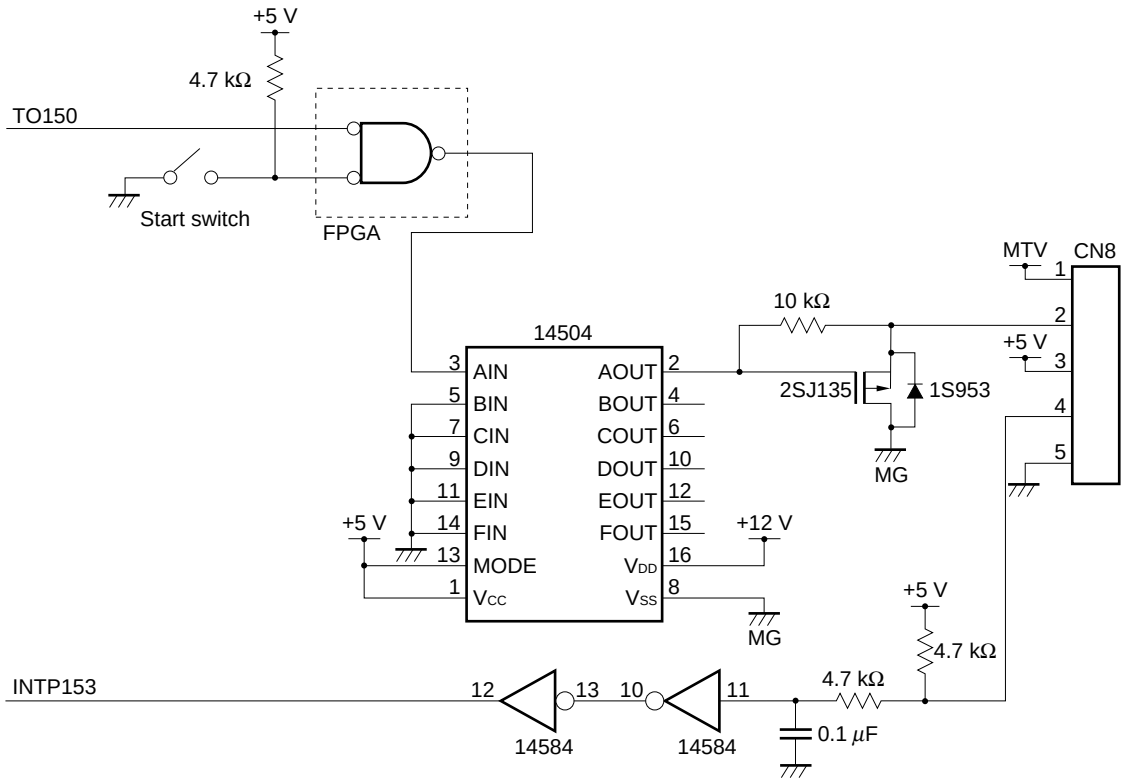
Figure 4-5. UART-Connected Circuit Example



4.1.8 Connection of RPU

The RPU is used for motor control of the TM15's TO150 output. The CC150 and CC151 registers are set as compare registers and the motor's rotational speed is controlled by changing the output pulse width. The motor's encoder output is connected to INTP153.

Figure 4-6. RPU-Connected Circuit Example



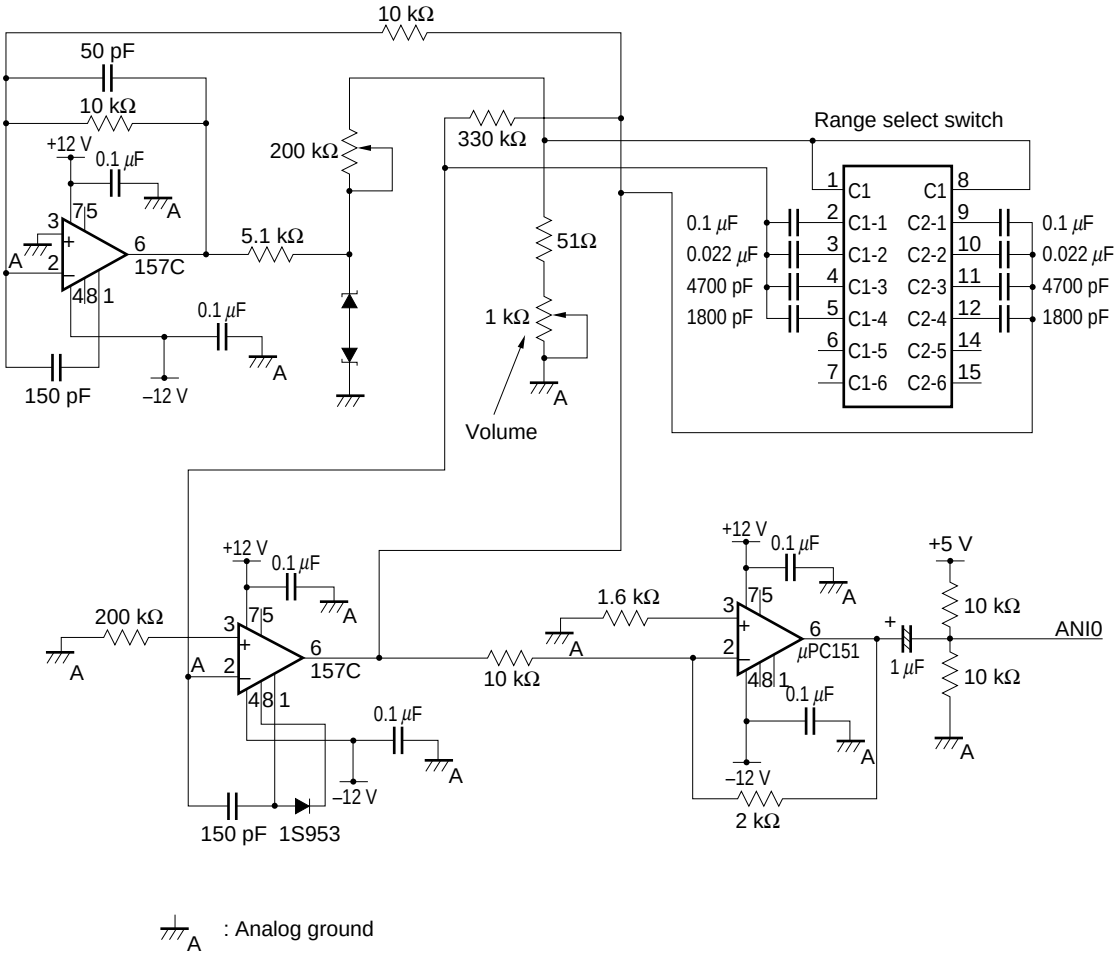
MTV: Power supply for motor
MG: Ground for motor

Remark The DC motor runs when pin 2 of CN8 is low.
A forced stop occurs when the start switch is set to OFF.

4.1.9 Connection of ADC

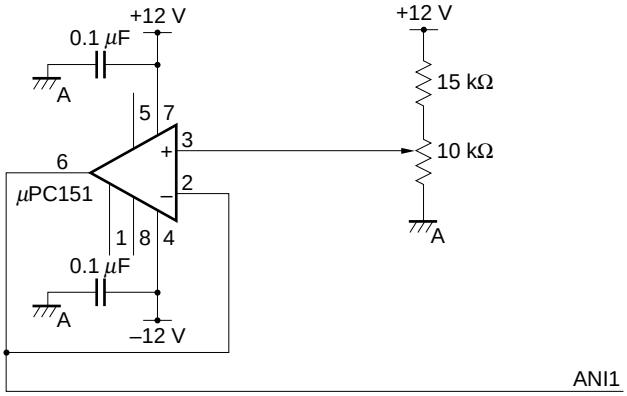
The three analog inputs for the sine-wave generator output, rheostat, and optical sensor are connected to ANI0, ANI1, and ANI2 respectively.

Figure 4-7. Connection of Sine-Wave Generator (ANI0)



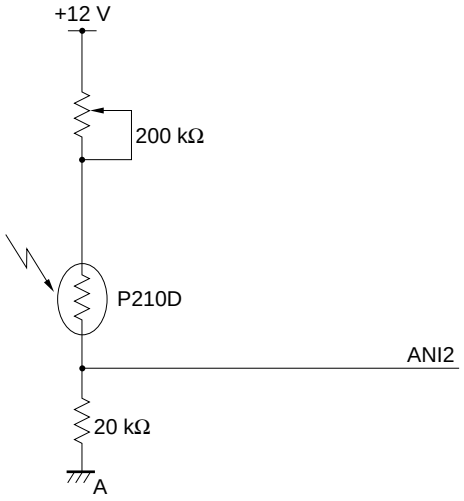
Remark The frequency can be modified via the range select switch and volume adjuster.

Figure 4-8. Connection of 0 to 5 V Input from Rheostat (ANI1)



: Analog ground

Figure 4-9. Connection of Optical Sensor (ANI2)



: Analog ground

4.1.10 Setting-related switches

The following switches are on the TB-V850E's board.

V850E/MS1 operation mode setting switch (DSW1):

This is a 4-bit DIP switch that sets the V850E/MS1's operation mode. It is connected to the V850E/MS1's MODE pins. The switch setting sets low level when ON and high level when OFF. Specification of the MODE3 pin via this switch is valid only when the slide switch for the flash memory programmer has not been set to the write side.

DSW1-1: Sets MODE0 pin
DSW1-2: Sets MODE1 pin
DSW1-3: Sets MODE2 pin
DSW1-4: Sets MODE3 pin

Remark The settings of DSW1 to 4 are ignored if the slide switch for the flash memory programmer has been set to the write side.

Slide switch for flash memory programmer (MSW1):

This slide switch is used when using the dedicated flash memory programmer to perform read or write operations involving the contents of the V850E/MS1's on-chip flash memory. When this switch is set to the write side, the V850E/MS1's MODE3 pin is set by the dedicated flash memory programmer.

Supplied clock setting switch (JP1):

This jumper switch specifies the clock that is supplied to the V850E/MS1's X1 pin.

Jumper set between 1-2: Selects OSC1 (fast clock)
Jumper set between 3-4: Selects OSC2 (slow clock)

RS-232C interface loopback switch (JP2):

This switch connects the send data and receive data in the RS-232C interface.

Jumper set between 1-2: Normal operation
Jumper set between 3-4: Send data is looped back to receive data

7-segment LED switch (MSW2):

This is an alternate toggle switch that selects between software control or hardware control of the 7-segment LED display that is implemented in this unit.

DC motor start switch (MSW3):

This is an alternate toggle switch that sets DC motor control as valid. The motor will not operate unless this switch has been set to ON. Setting it to OFF while the motor is running will cause the motor to stop.

General-purpose toggle switches (TSW1 to TSW8):

These are eight alternate toggle switches that are connected to the V850E/MS1's input ports (P110 to P117). P110 corresponds to TSW1 and P117 corresponds to TSW8. "0" is read when a switch is ON and "1" is read when it is OFF.

INT switch (INT):

This is a pushbutton switch that generates a maskable interrupt in relation to the V850E/MS1. It is connected to the INTP122 pin.

NMI switch (NMI):

This is a pushbutton switch that generates a non-maskable interrupt in relation to the V850E/MS1.

Reset switch (RESET):

This is a pushbutton switch that resets the TB-V850E. This switch takes the ORed result of the power on reset signal and the reset signal from the flash memory programmer interface connector.

4.1.11 Connectors

The connectors on the TB-V850E board are described below.

RS-232C interface connector (CN1):

Connector to be used: DSUB9 pin (DE-9S-T-N)

Pin No.	Pin name	Description of signal
1	NC	Not connected
2	RXD	Receive data
3	TXD	Transmit data
4	DTR	Data terminal ready
5	GND	Signal ground
6	NC	Not connected
7	RTS	Request to send
8	NC	Not connected
9	NC	Not connected

Flash memory programming interface connector (CN2):

Connector to be used: 10-pin header (3662-6002LCSC)

Pin No.	Pin name	Description of signal
1	GND	Signal ground
2	SI	Connects to CPU's SO0 pin
3	SO	Connects to CPU's SIO pin
4	SCK	Connects to CPU's $\overline{\text{SCK0}}$ pin
5	CLK	Not connected
6	$\overline{\text{RESET}}$	Reset input
7	VDD	+5 V
8	VPP	+10 V
9	NC	Not connected
10	NC	Not connected

Logic analyzer connectors (CN3 to CN6)

CN3

Pin No.	Pin name	Pin No.	Pin name
1	NC	11	D8
2	NC	12	D7
3	NC	13	D6
4	D15	14	D5
5	D14	15	D4
6	D13	16	D3
7	D12	17	D2
8	D11	18	D1
9	D10	19	D0
10	D9	20	GND

CN4

Pin No.	Pin name	Pin No.	Pin name
1	NC	11	D8
2	NC	12	D7
3	NC	13	D6
4	A15	14	A5
5	A14	15	A4
6	A13	16	A3
7	A12	17	A2
8	A11	18	A1
9	A10	19	A0
10	A9	20	GND

CN5

Pin No.	Pin name	Pin No.	Pin name
1	NC	11	$\overline{CS0}$
2	NC	12	A23
3	NC	13	A22
4	$\overline{CS7}$	14	A21
5	$\overline{CS6}$	15	A20
6	$\overline{CS5}$	16	A19
7	$\overline{CS4}$	17	A18
8	$\overline{CS3}$	18	A17
9	$\overline{CS2}$	19	A16
10	$\overline{CS1}$	20	GND

CN6

Pin No.	Pin name	Pin No.	Pin name
1	NC	11	$\overline{OE}$
2	NC	12	$\overline{WE}$
3	NC	13	$\overline{RD}$
4	UDQM	14	$\overline{UCAS}$/$\overline{UWR}$
5	LDQM	15	$\overline{LCAS}$/$\overline{LWR}$
6	CKE	16	$\overline{REFRQ}$
7	$\overline{SDRAMWE}$	17	$\overline{WAIT}$
8	$\overline{SDRAMCAS}$	18	$\overline{RESET}$
9	$\overline{SDRAMRAS}$	19	CLKOUT
10	$\overline{SDRAMCS}$	20	GND

4.2 Internal Register Settings

This section describes internal registers whose settings are determined by the TB-V850E's hardware configuration. The values set to other registers are determined by the application program. See **4.3 Program Examples**.

4.2.1 Bus interface

The settings related to the TB-V850E's bus interface are described below. The settings in these registers correspond to the V850E/MS1's internal system clock's 20-MHz operation (the external clock operates at 4 MHz). It is assumed that the EPROM and page ROM have an access time of 100 ns.

Figure 4-10. Memory Expansion Mode Register (MM) Settings

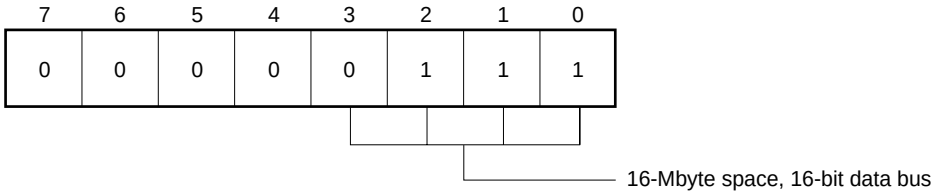
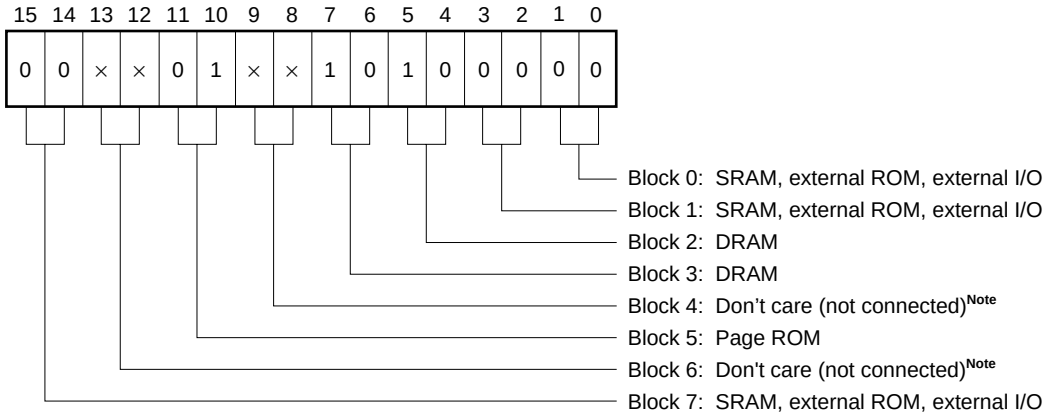
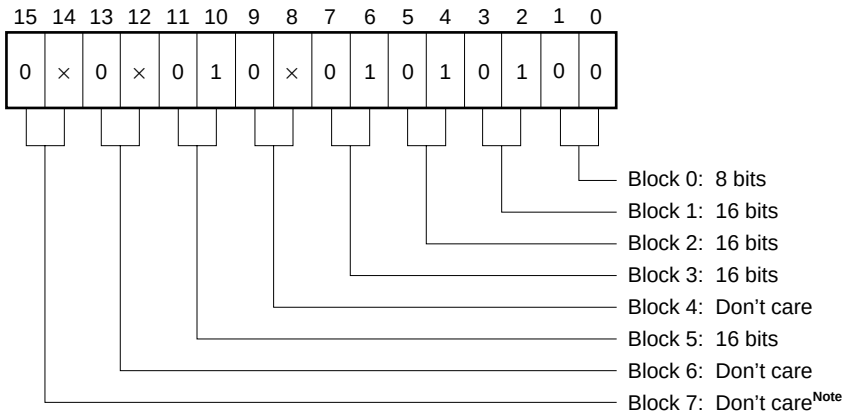


Figure 4-11. Bus Cycle Type Configuration Register (BCT) Settings



Note This setting can be any value other than "11".

Figure 4-12. Bus Size Configuration Register (BSC) Settings



Note Block 7's setting is "don't care" because it is valid only for byte access of even-numbered addresses.

Figure 4-13. Data Wait Control Registers 1 and 2 (DWC1 and DWC2) Settings

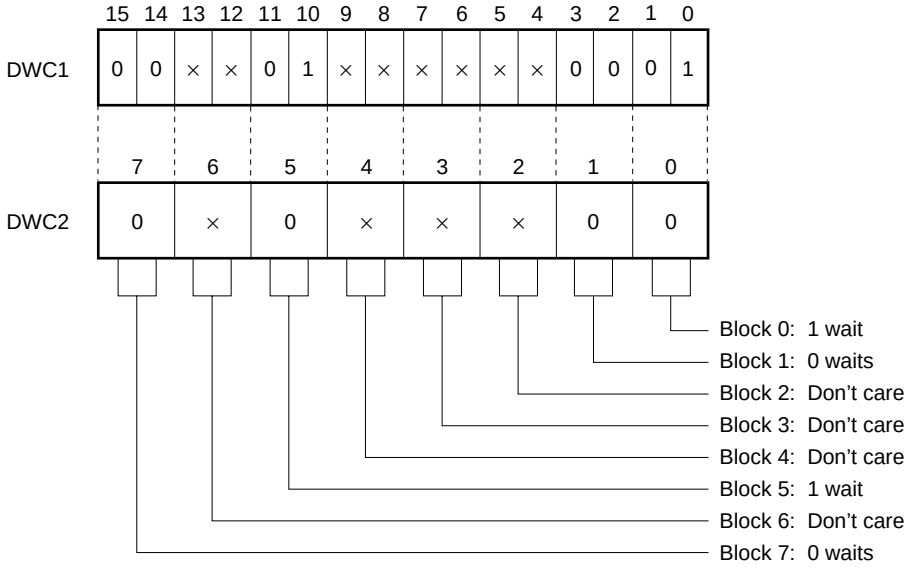


Figure 4-14. Bus Cycle Control Register (BCC) Settings

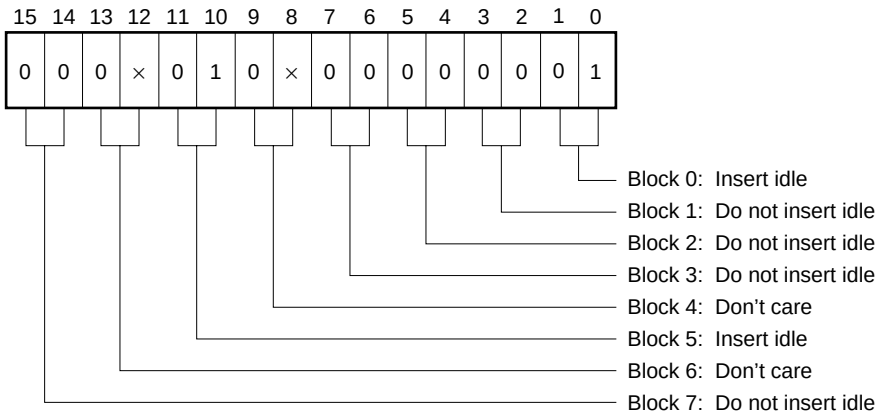


Figure 4-15. Page ROM Configuration Register (PRC) Settings

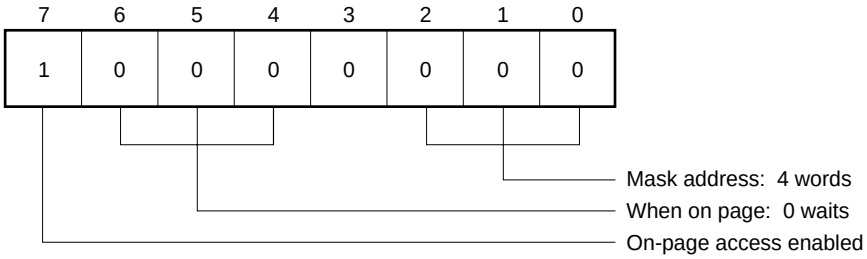


Figure 4-16. DRAM Type Configuration Register (DTC) Settings

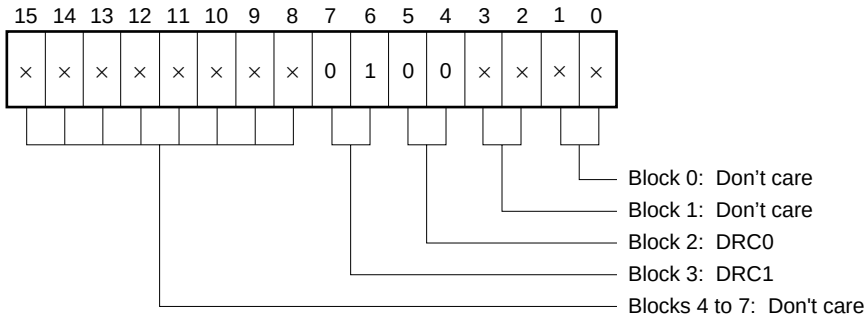


Figure 4-17. DRAM Configuration Register 0 (DRC0) Settings

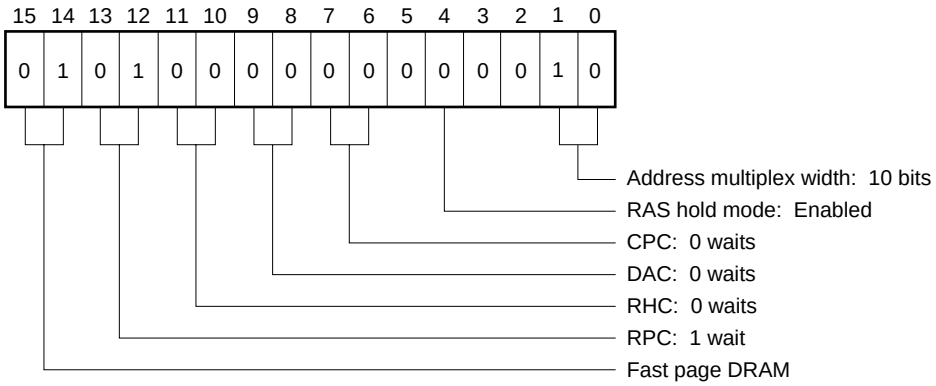


Figure 4-18. DRAM Configuration Register 1 (DRC1) Settings

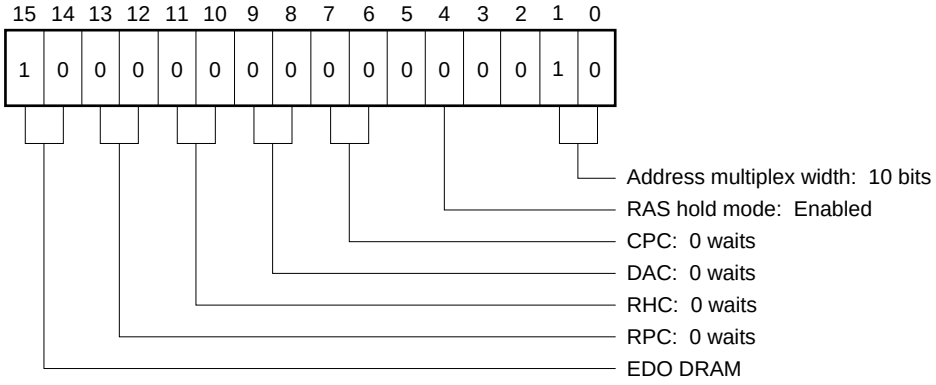


Figure 4-19. DRAM Configuration Registers 2 and 3 (DRC2 and DRC3) Settings

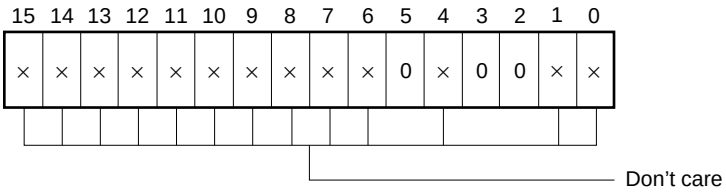


Figure 4-20. Refresh Control Registers 0 and 1 (RFC0 and RFC1) Settings

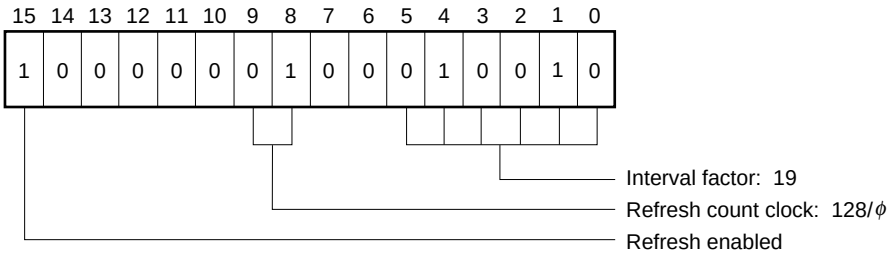


Figure 4-21. Refresh Control Registers 2 and 3 (RFC2 and RFC3) Settings

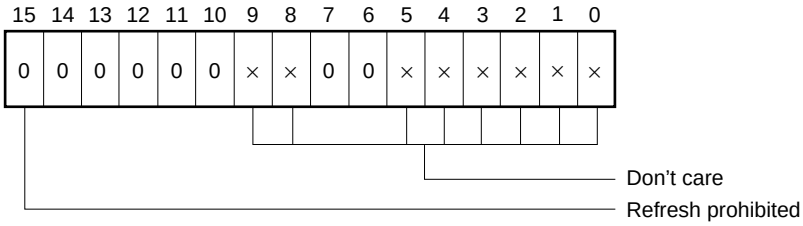
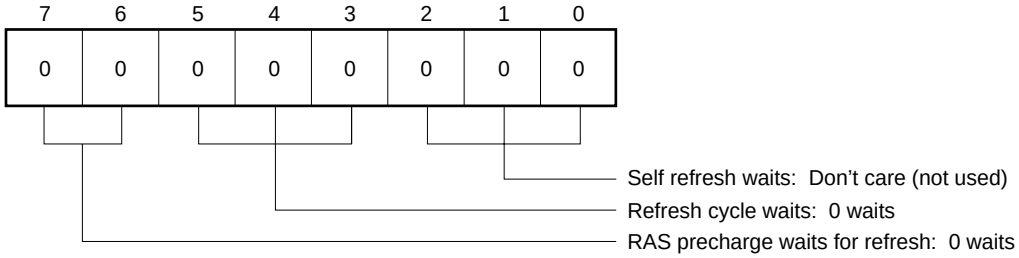
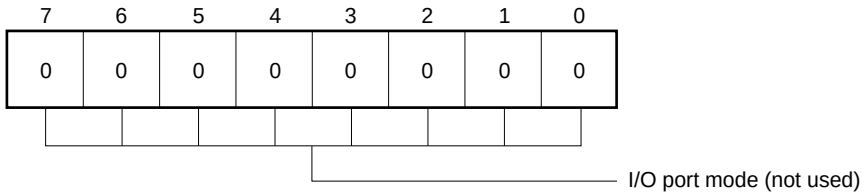


Figure 4-22. Refresh Wait Control Register (RWC) Settings



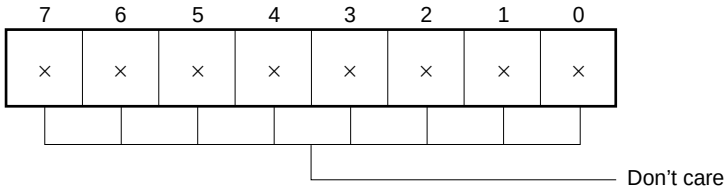
4.2.2 Port functions (pin function settings)

Figure 4-23. Port 0 Mode Control Register (PMC0) Settings



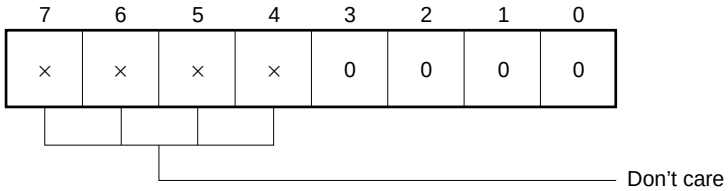
Remark PMC1 and PMCX have the same settings.

Figure 4-24. Port 0 Mode Register (PM0) Settings



Remark PM1, PM4, PM5, PM6, PM8, PM9, PM10, PM12, PMA, PMB, and PMX have the same settings.

Figure 4-25. Port/Control Select Register 0 (PCS0) Settings



Remark PCS1 and PCS11 have the same settings.

Figure 4-26. Port 2 Mode Control Register (PMC2) Settings

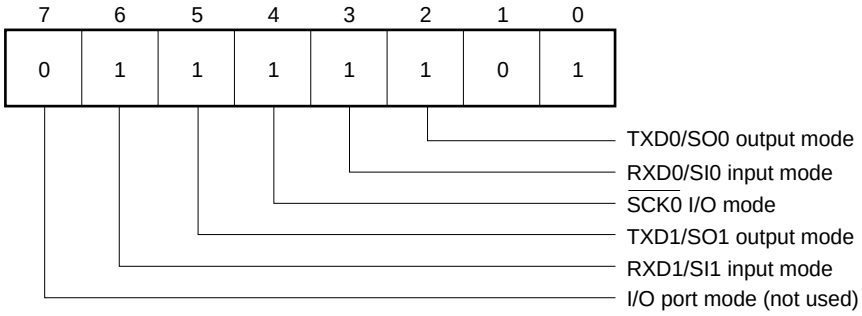


Figure 4-27. Port 2 Mode Register (PM2) Settings

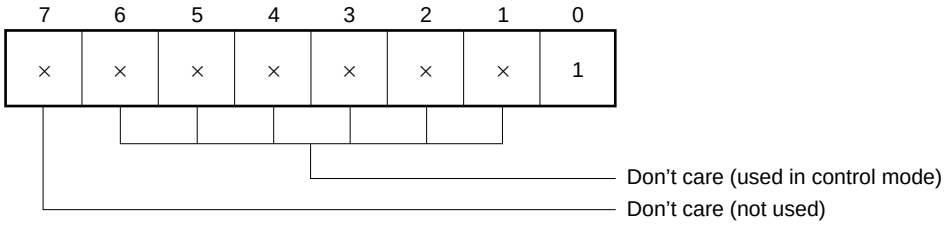


Figure 4-28. Port 3 Mode Control Register (PMC3) Settings

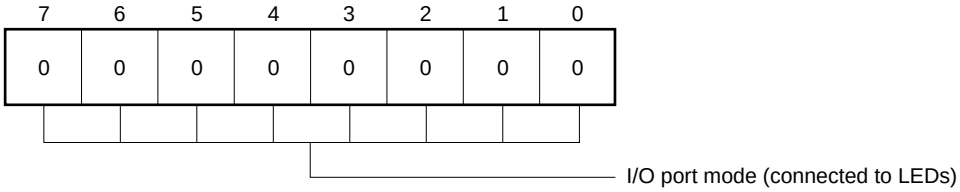


Figure 4-29. Port 3 Mode Register (PM3) Settings

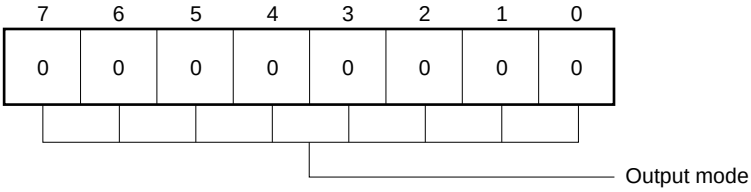


Figure 4-30. Port/Control Select Register 3 (PCS3) Settings

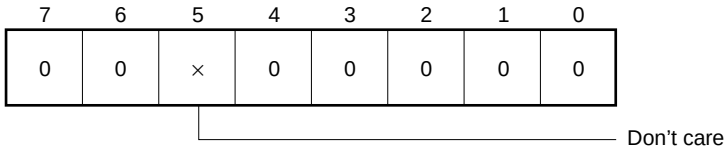
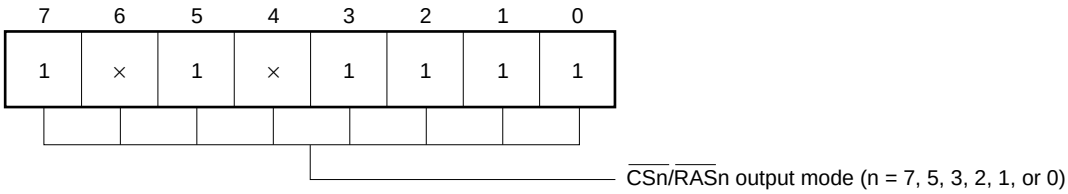
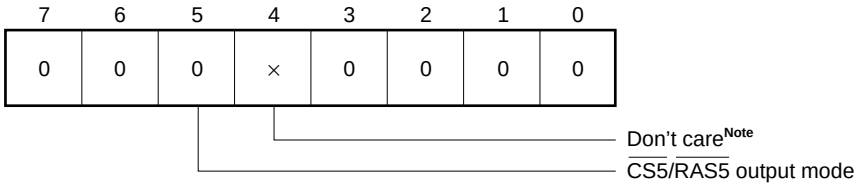


Figure 4-31. Port 8 Mode Control Register (PMC8) Settings



Remark Block 4 and block 6 are not used.

Figure 4-32. Port/Control Select Register 8 (PCS8) Settings



Note This setting is "don't care" because block 4 is not used.

Figure 4-33. Port 9 Mode Control Register (PMC9) Settings

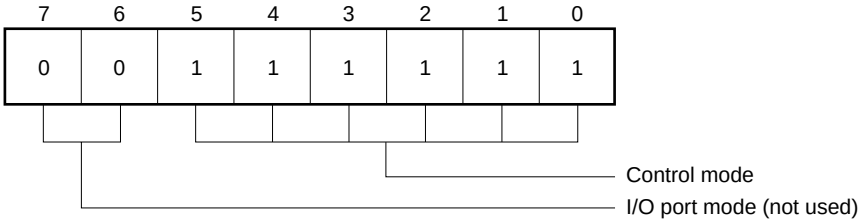


Figure 4-34. Port 10 Mode Control Register (PMC10) Settings

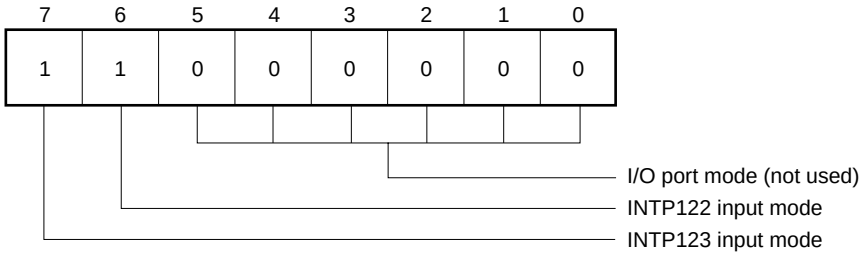


Figure 4-35. Port/Control Select Register 10 (PCS10) Settings

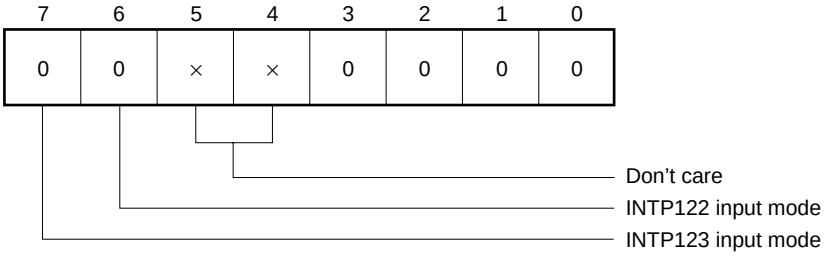


Figure 4-36. Port 11 Mode Control Register (PMC11) Settings

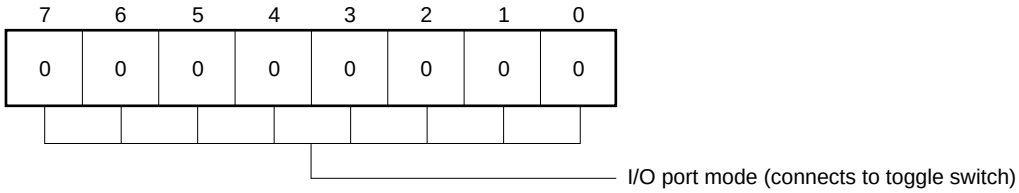


Figure 4-37. Port 11 Mode Register (PM11) Settings

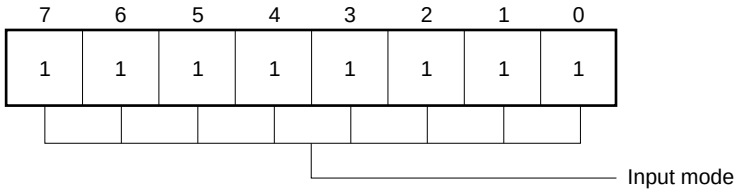
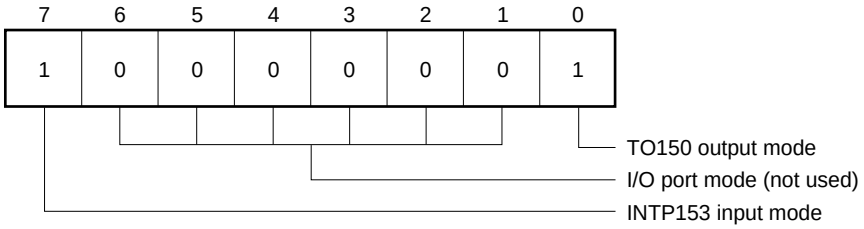


Figure 4-38. Port 12 Mode Control Register (PMC12) Settings



4.2.3 Interrupt control unit

Figure 4-39. External Interrupt Mode Register 0 (INTM0) Settings

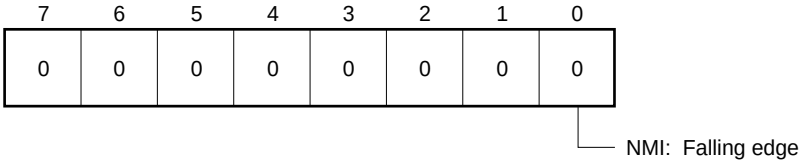
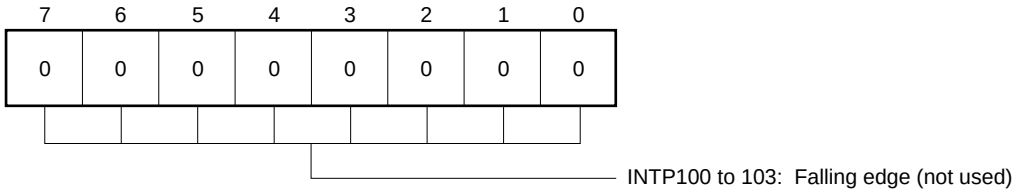


Figure 4-40. External Interrupt Mode Register 1 (INTM1) Settings



Remark INTM2, INTM4, and INTM5 have the same settings.

Figure 4-41. External Interrupt Mode Register 3 (INTM3) Settings

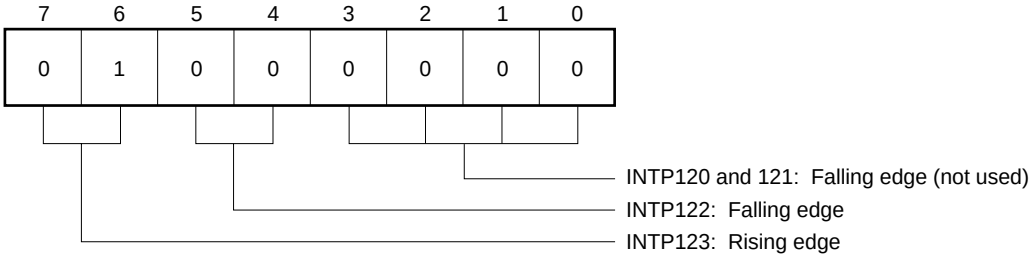
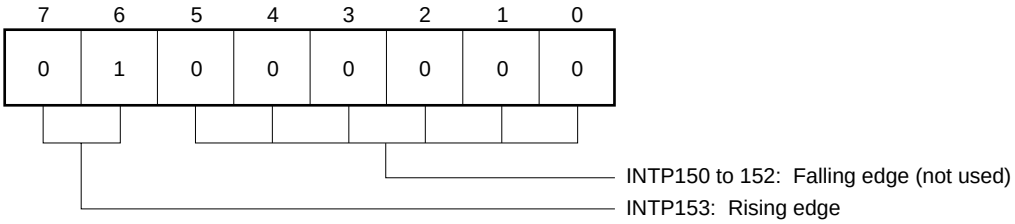
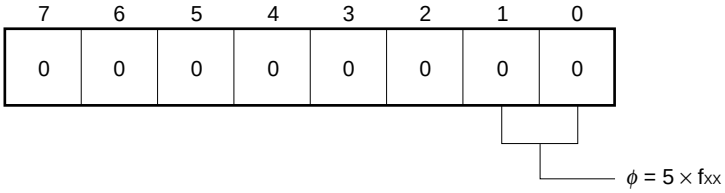


Figure 4-42. External Interrupt Mode Register 6 (INTM6) Settings



4.2.4 Clock generation function

Figure 4-43. Clock Control Register (CKC) Settings



Remark ϕ: Internal system clock's frequency
f_{XX}: External clock's frequency

4.3 Program Examples

Sections 4.3.1 to 4.3.9 below show examples of programs that are run in the TB-V850E.

It is assumed that the programs shown in sections 4.3.2 to 4.3.9 are linked with the TB-V850E initialization program shown in section 4.3.1.

4.3.1 TB-V850E initialization program

```
; This program for processing of common initialization settings is available for use when developing several
  programs to be run on the TB-V850E.
; The values set by this program are the same as the default values.
; <Registers used>
; r11:  For temporary use

######Reset interrupt servicing
.text
    .section “RESET”
    jr  init  ; To initialization processing

######Initializes the I/O register (for TB-V850E only)
.text
#Bus control register settings
init:
    mov     0x07,    r11
    st.b    r11,     MM[r0]      ;  Sets memory expansion mode register
    mov     0x0401,  r11
    st.h    r11,     DWC1[r0]    ;  Sets data wait control register 1
    mov     0x0401,  r11
    st.h    r11,     BCC[r0]     ;  Sets bus cycle control register
    mov     0x06a0,  r11
    st.h    r11,     BCT[r0]     ;  Sets bus cycle type control register
    mov     0x1554,  r11
    st.h    r11,     BSC[r0]     ;  Sets bus size configuration register
    mov     0x00,    r11
    st.h    r11,     DWC2[r0]    ;  Sets data wait control register 2

#Memory access control register settings
    mov     0x5102,  r11
    st.h    r11,     DRC0[r0]    ;  Sets DRAM configuration register 0
    mov     0x8002,  r11
    st.h    r11,     DRC1[r0]    ;  Sets DRAM configuration register 1
    mov     0x3f01,  r11
    st.h    r11,     DRC2[r0]    ;  Sets DRAM configuration register 2
```

```
    mov     0x3f01,  r11
    st.h    r11,     DRC3[r0]     ;  Sets DRAM configuration register 3
    mov     0x8112,  r11
    st.h    r11,     RFC0[r0]     ;  Sets refresh control register 0
    mov     0x8112,  r11
    st.h    r11,     RFC1[r0]     ;  Sets refresh control register 1
    mov     0x0000,  r11
    st.h    r11,     RFC2[r0]     ;  Sets refresh control register 2
    mov     0x0000,  r11
    st.h    r11,     RFC3[r0]     ;  Sets refresh control register 3
    mov     0x0040,  r11
    st.h    r11,     DTC[r0]      ;  Sets DRAM type configuration register
    mov     0x80,    r11
    st.b    r11,     PRC[r0]      ;  Sets page ROM configuration register
    st.b    r0,      RWC[r0]      ;  Sets refresh wait control register

#Clock generation function register settings
    mov     0x00,    r11
    st.b    r11,     PRCMD[r0]    ;  Issues store instruction to command register
    st.b    r11,     CKC[r0]      ;  Sets clock control register

#Port 0:  Reset value
    mov     0xff,    r11
    st.b    r11,     PM0[r0]      ;  Sets port 0 mode register
    mov     0x00,    r11
    st.b    r11,     PMC0[r0]     ;  Sets port 0 mode control register
    mov     0x00,    r11
    st.b    r11,     PCS0[r0]     ;  Sets port/control select register 0

#Port 1:  Reset value
    mov     0xff,    r11
    st.b    r11,     PM1[r0]      ;  Sets port 1 mode register
    mov     0x00,    r11
    st.b    r11,     PMC1[r0]     ;  Sets port 1 mode control register
    mov     0x00,    r11
    st.b    r11,     PCS1[r0]     ;  Sets port/control select register 1

#Port 2:  Used by UART
    mov     0xff,    r11
    st.b    r11,     PM2[r0]      ;  Sets port 2 mode register
    mov     0x7d,    r11          ;  Sets control mode
    st.b    r11,     PMC2[r0]     ;  Sets port 2 mode control register
```

```
#Port 3:  Used by LED display
    mov     0x00,   r11             ;  Sets output mode
    st.b    r11,    PM3[r0]         ;  Sets port 3 mode register
    mov     0x00,   r11
    st.b    r11,    PMC3[r0]        ;  Sets port 3 mode control register
    mov     0x00,   r11
    st.b    r11,    PCS3[r0]        ;  Sets port/control select register 3

#Port 4:  Reset value
    mov     0xff,   r11
    st.b    r11,    PM4[r0]         ;  Sets port 4 mode register

#Port 5:  Reset value
    mov     0xff,   r11
    st.b    r11,    PM5[r0]         ;  Sets port 5 mode register

#Port 6:  Reset value
    mov     0xff,   r11
    st.b    r11,    PM6[r0]         ;  Sets port 6 mode register

#Port 7:  Not set

#Port 8:  Used by control mode
    mov     0xff,   r11
    st.b    r11,    PM8[r0]         ;  Sets port 8 mode register
    mov     0xff,   r11
    st.b    r11,    PMC8[r0]        ;  Sets port 8 mode control register
    mov     0x00,   r11
    st.b    r11,    PCS8[r0]        ;  Sets port/control select register 8

#Port 9:  Control signal output settings when memory is expanded
    mov     0xff,   r11
    st.b    r11,    PM9[r0]         ;  Sets port 9 mode register
    mov     0x3f,   r11
    st.b    r11,    PMC9[r0]        ;  Sets port 9 mode control register
    mov     0x00,   r11
    st.b    r11,    PCS9[r0]        ;  Sets port/control select register 9

#Port 10:  INT switch (INTP122), sine-wave (INTP123) interrupt settings
    mov     0xff,   r11
    st.b    r11,    PM10[r0]        ;  Sets port 10 mode register
    mov     0xc0,   r11
    st.b    r11,    PMC10[r0]       ;  Sets port 10 mode control register
    mov     0x00,   r11
    st.b    r11,    PCS10[r0]       ;  Sets port/control select register 10
```

```
#Port 11:  Used by toggle switch input
    mov     0xff,    r11
    st.b    r11,     PM11[r0]     ;  Sets port 11 mode register
    mov     0x00,    r11
    st.b    r11,     PMC11[r0]    ;  Sets port 11 mode control register
    mov     0x00,    r11
    st.b    r11,     PCS11[r0]    ;  Sets port/control select register 11

#Port 12:  Pulse generator output interrupt (INTP153) settings
    mov     0xff,    f11
    st.b    r11,     PM12[r0]     ;  Sets port 12 mode register
    mov     0x81,    r11
    st.b    r11,     PMC12[r0]    ;  Sets port 12 mode control register

# Port A:  Reset value
    mov     0xff,    r11
    st.b    r11,     PMA[r0]      ;   Sets port A mode register

# Port B:  Reset value
    mov     0xff,    r11
    st.b    r11,     PMB[r0]      ;  Sets port B mode register

# Port X:  Reset value
    mov     0xff,    r11
    st.b    r11,     PMX[r0]      ;  Sets port X mode register
    mov     0x00,    r11
    st.b    r11,     PMCX[r0]     ;  Sets port X mode control register

#External interrupt mode register
    mov     0x00,    r11
    st.b    r11,     INTM0[r0]    ;  Sets external interrupt mode register 0
    mov     0x00,    r11
    st.b    r11,     INTM1[r0]    ;  Sets external interrupt mode register 1
    mov     0x00,    r11
    st.b    r11,     INTM2[r0]    ;  Sets external interrupt mode register 2
    mov     0x40,    r11
    st.b    r11,     INTM3[r0]    ;  Sets external interrupt mode register 3
    mov     0x00,    r11
    st.b    r11,     INTM4[r0]    ;  Sets external interrupt mode register 4
    mov     0x00,    r11
    st.b    r11      INTM5[r0]    ;  Sets external interrupt mode register 5
    mov     0x40,    r11
    st.b    r11,     INTM6[r0]    ;  Sets external interrupt mode register 6

    jr      start                 ;  To main program
```

4.3.2 Memory access

```
;  This program writes fixed data to address xx200000H in an external SRAM area
;  <Registers used>
;  r10:  SRAM address
;  r11:  Data to be set (55H)

.globl   start
.set     sram_adr,     0x200000     ;  SRAM address
.text
start:
    mov     sram_adr, r10           ;  Sets write address
    movea 0x55, r0    r11           ;  Sets write data
loop:
    st.b    r11,          0x0[r10]  ;  Writes in byte units
    br      loop                    ;  Loopback
```

4.3.3 Memory fill

```
; This program zero-clears a 256-Kbyte section of an external SRAM area (address range: xx200000H to
  xx23FFFFH).
; <Registers used>
; r10: Write address
; r11: End of fill address

.globl  start
.set    sram_adr_s, 0x200000    ; SRAM address (start of fill address)
.set    sram_adr_e, 0x240000    ; SRAM address (end of fill address)
.text
start:
    mov     sram_adr_s, r10     ; Sets fill start address to write address
    mov     sram_adr_e, r11     ; Sets fill end address
loop:
    st.w    r0,     0x0[r10]    ; Writes zeros in word units
    add     0x4     r10         ; Updates address
    cmp     r10,    r11         ; End address?
    bne     loop                ; Loopback if not end address
forever:
    br      forever             ; Processing completion loop
```

4.3.4 Switch input and LED output

```
; This program reads the status of port 11 (toggle switch) and writes the read data to port 3 (LED).
: <Registers used>
; r10: I/O data

.globl  start
.text
start:
loop:
    id.b    P11[r0], r10        ; Input from port 11
    st.b    r10,    P3[r0]      ; Output to port 3
    br      loop                ; Loopback
```

4.3.5 Timer interrupt

```
;  This program increments and lights LED lamps when a timer interrupt occurs.
;  The timer interrupt interval is set as 100 ms.
;  <Registers used>
;  r11:  For temporary use
;  r12:  LED ON value
;  r13:  LED address

.globl      _intcm40
.globl      start
.set        led_adr,   0xfffff006          ;  LED address

    --Interrupt handler settings
.section    “INTCM40”
    jr      _intcm40                       ;  To timer interrupt service

.text
start:
    --Count clock settings                 ;  φ = 20 MHz
    st.b    r0,        TMC40[r0]           ;  φ = φ/32
    --Interrupt interval settings
    mov     62500,     r11                 ;  100 ms = (φ/32) * (62500)
    st.h    r11,       CM40[r0]            ;  Value setting
    mov     r0,        r12                 ;  Initialization of LED ON value
    mov     led_adr,   r13                 ;  LED address setting
    st.b    r12,       0[r13]              ;  LED initialization (all OFF)
    --Interrupt control register settings
    mov     0x07,      r11                 ;  Interrupt priority level 7
    st.b    r11,       CMIC40[r0]          ;  Enables timer 4 interrupt
    set1    7,         TMC40[r0]           ;  Starts timer 4 count
    ei                                     ;  Enables interrupts
forever_lp:
    nop
    br      forever_lp

    --Processing of timer 4 interrupt
_intcm40:
    add     1,         r12                 ;  Increments display counter
    st.b    r12,       0[r13]              ;  LED display
    reti
```

4.3.6 Multiple interrupts

```
;  When a timer interrupt occurs, the LEDs are either incremented and lit or decremented and lit.
;  Each time the INT switch is pressed, the mode is switched between increment mode and decrement mode.
;  An interrupt triggered by the INT switch can be received only during the timer interrupt service routine.
;  The timer interrupt interval is set as 100 ms.
;  <Registers used>
;  r3:  Stack address
;  r11:  For temporary use
;  r12:  LED ON value
;  r13:  LED address
;  r14:  Increment/decrement switch flag
;  r20:  For temporary use

.globl      _intcm40
.globl      start
.set        led_adr,     0xfffff006   ;  LED address
.set        stack_adr,   0x220000     ;  Stack address

    --Interrupt handler settings
.section    “INTCM40”
    jr          _intcm40              ;  To timer interrupt service
.section    “INTP122”
    jr          _intp122              ;  To INT switch interrupt service

.text
start:
    --Count clock setting             ;  φ = 20 MHz
    st.b        r0,         TMC40[r0] ;  φ = φ/32
    --Interrupt interval setting
    mov         62500,      r11       ;  100 ms = (φ/32) * (62500)
    st.h        r11,        CM40[r0]  ;  Value setting
    --Initialization of various data
    mov         r0,         r12       ;  Initialization of LED ON value
    mov         led_adr,    r13       ;  LED address setting
    st.b        r12,        0[r13]    ;  LED initialization (all OFF)
    mov         stack_adr,  r3        ;  Stack address setting
    mov         r0,r14                ;  Initialization of increment setting
    --Interrupt control register settings
    mov         0x40,       r11       ;  Prohibits interrupts, interrupt priority level 0
    st.b        r11,        P12IC2[r0]  ;  INT switch interrupt setting
    mov         0x07,       r11       ;  Enables interrupts, interrupt priority level 7
    st.b        r11,        CMIC40[r0]  ;  Timer 4 interrupt setting
    set1        7,          TMC40[r0]  ;  Timer 4 count start
    ei                                ;  Enables interrupt
forever_lp:
    nop
    br          forever_lp
```

```
    --INT switch interrupt service
_intp122:
    notr14, r14         ;  Invert increment/decrement flag
    reti

    --Timer 4 interrupt servicing
_intcm40:
    --Save to EIPC, EIPSW stacks
    add     -8,     r3
    stsr    0,      r20
    st.w    r20     4[r3]
    stsr    1,      r20
    st.w    r20     0[r3]
    --Enable INT switch interrupt servicing
    clr1    6,      P12IC2[r0]  ;  Cancels interrupt masking
    ei                          ;  Enables interrupt servicing
    --Create/display LED display data
    cmp     r0,     r14         ;  Increment/decrement judgement
    bne     _cm40_dec           ;  If decrement
    add     1,      r12         ;  Increments display counter
    br      _cm40_disp          ;  To display processing
_cm40_dec:
    sub     1,      r12         ;  Decrements display counter
_cm40_disp:
    st.b    r12     0[r13]      ;  LED display
--INT switch interrupt disable
    di                          ;  Disables interrupts
    set1    6,      P12IC2[r0]  ;  INT switch interrupt mask setting
    --Restore from EIPC and EIPSW stacks
    ld.w    0[r3],  r20
    ldsr    r20,    1
    ld.w    4[r3],  r20
    ldsr    r20,    0
    add     8,      r3
    reti
```

4.3.7 DMA transfer between memory devices

```
; Using the DMA function, this program transfers a 64-Kbyte section of memory contents starting from address
  xx200000H to address xx210000H.
; <Registers used>
; r10:  For temporary use
; r11:  For temporary use

.globl      _intdma0
.globl      forever_lp
.globl      start
.set        source_adr, 0x200000  ; Source address
.set        desti_adr,  0x210000  ; Destination address

    --Interrupt handler settings
.section    “INTDMA0”
    jr      _intdma0              : INTDMA0 (DMA transfer completion interrupt)
.text
start:
    --DMA transfer settings
      --Source and destination address settings
    movea   hi (source_adr) , r0, r11   ; Source address (high) setting
    st.h    r11,    DSA0H[r0]
    movea   lo (source_adr) , r0, r11   ; Source address (low) setting
    st.h    r11,    DSA0L[r0]
    movea   hi (desti_adr) , r0, r11    ; Destination address (high) setting
    st.h    r11,    DDA0H[r0]
    movea lo (desti_adr), r0, r11       ; Destination address (low) setting
    st.h    r11,    DDA0L[r0]
    --Byte transfer settings
    mov     0xFFFF, r11         ; Sets transfer count – 1
    st.h    r11,    DBC0[r0]
    --Addressing control register settings
    --Transfer data size:  8 bits, count direction for source address:  increment
    --Count direction for destination address:  increment, transfer mode:  single-step mode
    --Transfer type:  two-cycle transfer
    mov     0x04,   r11
    st.h    r11,    DADC0[r0]
    --DMA interrupt control register setting
    mov     0x7,    r11         ; Enables interrupts, interrupt priority level 7
    st.b    r11,    DMAIC0[r0]
    --DMA channel control register settings
    set1    0,      DCHC0[r0]   ; Enables DMA transfer
    set1    1,      DCHC0[r0]   ; Starts DMA transfer (software trigger:  ON)
```

```
    --Interrupt enable settings
    ei                              ; Enables interrupts
forever_lp:
    nop
    br          forever_lp          ; Terminates endless loop

    --DMA completion interrupt service
_intdma0:
    id.b        DCHC0[r0],    r10   ; Read to clear register
    reti
```

4.3.8 DMA transfer from UART to memory

```
;  This program copies SRAM data via a 4-Kbyte UART.
;  Source address:  xx200000H (SRAM)
;  Destination address:  xx210000H (SRAM)
;  Transfers from source address to UART1 are in byte units.
;  UART1 is a loopback, so reception ends after completion of transmission.
;  Receive data is copied to the destination address using DMA0.
;  In such cases, the DMA0 trigger source is set when UART1 reception is completed.
;  <Registers used>
;  r10:  For temporary use
;  r11:  For temporary use
;  r15:  UART send completion flag
;  r16:  Processing end flag
;  r20:  Source address
;  r29:  Return address when jarl instruction is used

.globl      _indma0
.globl      _intser1
.globl      _intst1
.globl      _intsr1
.globl      send_lp
.globl      send_1byte
.globl      start
.globl      forever_lp

.set        source_adr, 0x200000  ;  Source address
.set        desti_adr,  0x210000  ;  Destination address
.set        rxb1_adr,   0xfffff0da  ;  Receive buffer (RXB1) address

    --Interrupt handler settings
.section    “INTSR1”
    jr      _intsr1               ;  INTSR1 (UART1 reception completion interrupt)
.section    “INTST1”
    jr      _intst1               ;  INTST1 (UART1 transmission completion interrupt)
.section    “INTSER1”
    jr      _intser1              ;  INTSER1 (UART1 receive error interrupt)
.section    “INTDMA0”
    jr      _intdma0              ;  DMA transfer completion interrupt
.text
start:
    --Data settings for checking (fill with fixed value “55H”)
    mov     source_adr,  r20      ;  Source address
    movea 0x55, r0,      r11      ;  Uses fixed value “55H” as data setting
```

```
lp1:
    st.b    r11,    0[r20]      ; Writes data setting to source address
    add     1,  r20             ; Increments source address
    cmp     0x201000, r20       ; End address?
    jnz     lp1                 ; Loops if not end address

    --DMA transfer settings
      --Source address and destination address settings
    movea   hi (rxb1_adr) , r0, r11  ; Source address (high) setting
    st.h    r11,    DSA0H[r0]
    movea lo (rxb1_adr) , r0, r11    ; Source address (low) setting
    st.h    r11,    DSA0L[r0]
    movea hi (desti_adr) , r0, r11   ; Destination address (high) setting
    st.h    r11,    DDA0H[r0]
    movea lo (desti_adr) , r0, r11   ; Destination address (low) setting
    st.h    r11,    DDA0L[r0]
    --Byte transfer settings
    mov     0x0fff,  r11        ; Sets transfer count – 1
    st.h    r11,    DBC0[r0]
    --Addressing control register settings
      --Transfer data size:  8 bits, count direction for source address:  fixed
      --Count direction for destination address:  increment, transfer mode:  single mode
      --Transfer type:  two-cycle transfer
    mov     0x0080, r11
    st.h    r11,    DADC0[r0]
    --DMA trigger source register settings
    mov     0x17,   r11         --Sets DMA transfer trigger source to INTSR1
    st.b    r11,    DTFR0[r0]
    --DMA interrupt control register settings
    mov     0x7,    r11         ; Enables interrupts, interrupt priority level 7
    st.b    r11,    DMAIC0[r0]
    --Asynchronous serial interface mode register settings
      --Transmit/receive enabled, no parity, data length:  8 bits, stop bits: 1 bit
      --Serial clock:  Baud rate generator output
    mov     0xc8,   r11
    st.b    r11,    ASIM10[r0]
    st.b    r0,     ASIM11[r0]  ; Prohibits extended bit operations
    --Baud rate generator settings
      --Sets 9600 bps (system clock: 10 MHz)
    --Baud rate generator compare register (timer count value) settings
    mov     16,     r11
    st.b    r11,    BRGC1
```

```
    --Baud rate generator prescaler mode register (prescaler setting) settings
    mov     0x80,    r11
    st.b    r11,     BPRM1
    --UART1 receive error interrupt control register settings
    mov     0x7,     r11          ; Enables interrupts, interrupt priority level 7
    st.b    r11,     SEIC1[r0]
    --UART1 reception completion interrupt control register settings
    mov     0x47,    r11          ; Enables interrupts, interrupt priority level 7
    st.b    r11,     SRIC1[r0]
    --UART1 transmission completion interrupt control register settings
    mov     0x7,     r11          ; Enables interrupts, interrupt priority level 7
    st.b    r11,     STIC1[r0]
    --DMA channel control register settings
    st.b    r0,      DCHC0[r0]
    set1    0,       DCHC0[r0]    ; DMA transfer enabled
    --Initialization of control data
    mov     0,       r15          ; UART1 ready to send
    mov     0,       r16          ; Transmission end flag OFF
    mov     source_adr,  r20      ; Transfer source memory address
    ei                            ; Enables interrupts

    --UART1 transmit completion standby
send_lp:
    cmp     0,       r15          ; UART1 transfer check
    bnz     send_lp               ; Loops until transfer is completed

    --UART1 transfer processing
    jarl    send_1byte,  r29      ; Transfers 1-byte data
    cmp     r0,      r16          ; Transfer completed?
    bz      send_lp               ; If not completed, wait until transfer is completed.

    --Terminate endless loop
forever_lp:
    nop
    nop
    nop
    br      forever_lp

    --Processing to send one byte of data from source address
send_1byte:
    tst1    7,DCHC0[r0]           ; DMA transfer completed?
    bnz     sd_1byte_end          ; If transfer is completed, end processing
```

```
    tst1    7,ASIS1[r0]         ; OK to send to UART1?
    bnz     sd_1byte_exit       ; Ends processing if transmission is not possible
    ld.b    0[r20],  r12        ; Loads source data
    add     1,       r20        ; Increments transmit data address
    mov     1,       r15        ; Prohibits next transmission
    st.b    r12,     TXS1L[r0]  ; Sends data to UART1

sd_1byte_exit:
    jmp     [r29]
sd_1byte_end:
    mov     1,       r16        ; Transmission end flag ON
    jmp     [r29]

    --Transmission completion interrupt
_intst1:
    mov     0,       r15        ; Enables next data send
    reti

    --Reception completion interrupt
_intsr1:
    nop
    reti

    --Receive error interrupt
_intser1:
    ld.b    RXB1L[r0],  r13     ; Reads and discards data
    sub     1,       r20        ; Decrements transmit data address
    mov     0,       r15        ; Enables next data transmission
    reti

    --DMA transfer completion interrupt
_intdma0:
    nop
    reti
```

4.3.9 Control of motor speed via switch input

```
; The motor's speed is controlled by RPU output of the port 11 (toggle switch) mode as the motor speed control
  setting.
; <Registers used>
; r10:  For temporary use
; r11:  Motor speed setting
; r20:  Toggle switch value

.globl      start
.text
start:
    mov     0x0,      r20           ; Sets previous toggle switch to "stop motor" mode
loop:
    ld.bu   P11[r0],  r11           ; Inputs toggle switch setting as unsigned value
    cmp     r11,      r20           ; Compares with previous toggle switch setting
    bne     time_set                ; Goes to setup processing if value differs from previous setting
    br      loop                    ; Loopback
time_set:
    clr1    7,        TMC15[r0]     ; Stops timer
    mov     r11,      r20           ; Updates toggle switch setting
    cmp     r0,       r20           ; Compares toggle switch setting with "0"
    be      time_dis                ; Sets output prohibit if toggle switch value is "0"
    shl8,   r11                     ; Creates setting values (8 bits R 16 bits)
    --Compare register settings (motor speed is increased if output low status is held for a long time)
    mov     1,        r10
    st.h    r10,      CC150[r0]     ; Count when status changes to low
    st.h    r11,      CC151[r0]     ; Count when status changes to high
    --TOC15 register setting
    mov     0x20,     r10
    st.b    r10,      TOC15[r0]     ; Active level low, enables timer output
    --TMU15 register setting
    mov     0x30,     r10
    st.h    r10,      TUM15[r0]     ; Sets compare operation
    --TMC15 register setting
    mov     0x08,     r10
    st.b    r10,      TMC15[r0]     ; Count clock setting
    --Start timer
    set1    7,        TMC15[r0]     ; Starts output
    br      loop                    ; Loopback
time_dis:
    --Prohibit timer output:  Sets inactive level output, sets high-fixed output (return to default status)
    st.b    r0,       TOC15[r0]     ; Prohibits timer output
    br      loop                    ; Loopback
```

4.4 TB-V850E Specifications

4.4.1 List of specifications

Table 4-3. List of TB-V850E Specifications

Item	Description
V850E/MS1	Internal system clock = 40 MHz (maximum) Connect crystal oscillator to pin X1 (leave pin X2 open). • Two types of crystal oscillator sockets are implemented • Select using jumper switches before connecting • Internal system clock (ϕ) = 5 × f_{XX} Operation mode is set by DIP switches.
EPROM	Capacity: 128 Kbytes ROM usage: One μPD27C1001 or equivalent device
Page ROM	Capacity: 512 Kbytes ROM usage: One HM27C4000G or equivalent devices
SRAM	Capacity: 256 Kbytes SRAM usage: Two μPD431008LE-20 or equivalent devices
DRAM	Capacity: 2 Mbytes DRAM usage: One μPD42S18160G5-60-7JF
EDO DRAM	Capacity: 2 Mbytes DRAM usage: One μPD42S18165G5-60-7F
Switches	Toggle switches: 8 Push-button switches: 3 NMI switch: 1 INT switch: 1 Reset switch: 1
LED	7-segment LEDs: 5 LED lamps: 9 General-purpose lamps (red): 8 Power lamp: 1 A switch is used to select between software display or pulse-counter display for the 7-segment LED display.
Sine-wave generator	Oscillation from VCO (Voltage Controlled Oscillator) Frequency: Range is 100 Hz to 20 kHz (rotary switch, volume adjuster) Amplitude: Fixed at 5 V_{P-P} Input to ANI0
Waveform shaper	Changes output from sine-wave generator to square wave and inputs it to INTC.
Analog output	Volume-adjusted voltage level is input to ANI1. Voltage level: 0 to 5 V
Optical sensor	Input to ANI2
RS-232C interface	Uses V850E/MS1's on-chip UART1
Pulse counter	Counts frequency of sine-wave generator Five connected decimal counters Counter output can be displayed on 7-segment LEDs.

4.4.2 Circuit diagrams

Diagrams of TB-V850E circuits are shown in Figures 4-44 to 4-49 below.

(1) CPU and LED, toggle switches

This circuit mainly includes the V850E/MS1, an oscillator, mode setting switches, 8 toggle switches, 8 LEDs, and an INT switch.

(2) Memory

This circuit mainly includes EPROM, SRAM, fast page DRAM, EDO DRAM, and page ROM memory devices.

(3) Device control circuit

This circuit mainly includes an EPF10K10QC208-3, EPC1PC8, 7-segment LED select switch, DC motor, and start switch.

EPF10K10QC208-3: FPGA (Field Programmable Gate Array)
Various signals related to the CPU's bus interface and output signals from the sine-wave generator are input to this device, which controls the pulse count and LEDs.

EPC1PC8: Serial EEPROM
This device is used to store data that is written to the FPGA.

(4) Flash memory programmer interface

This circuit mainly includes a power on reset circuit, flash memory programmer interface, and connectors used for the logic analyzer.

TL7705A: Power supply monitor
This is used by the function that triggers resets.

(5) LED control circuit

This circuit mainly includes five 7-segment LEDs, three 74FCT16244 devices, and a MAX232 device.

74FCT16244: 16-bit buffer

MAX232: RS-232 driver/receiver

(6) I/O circuit

This circuit mainly includes analog amplifier and optical sensor devices, a DC motor connector, and a power supply connector.

[MEMO]

Figure 4-44. V850E CPU

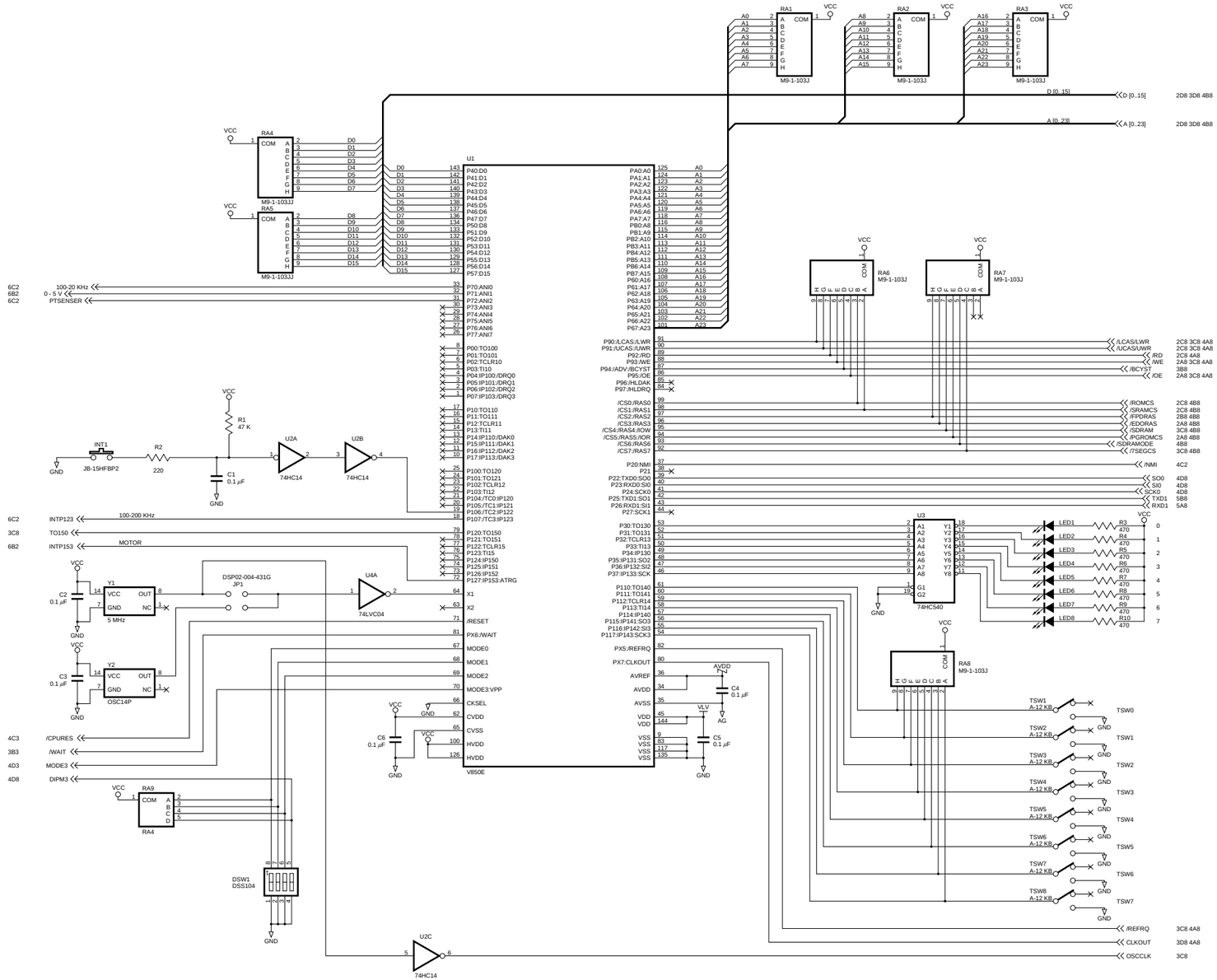


Figure 4-45. Memory

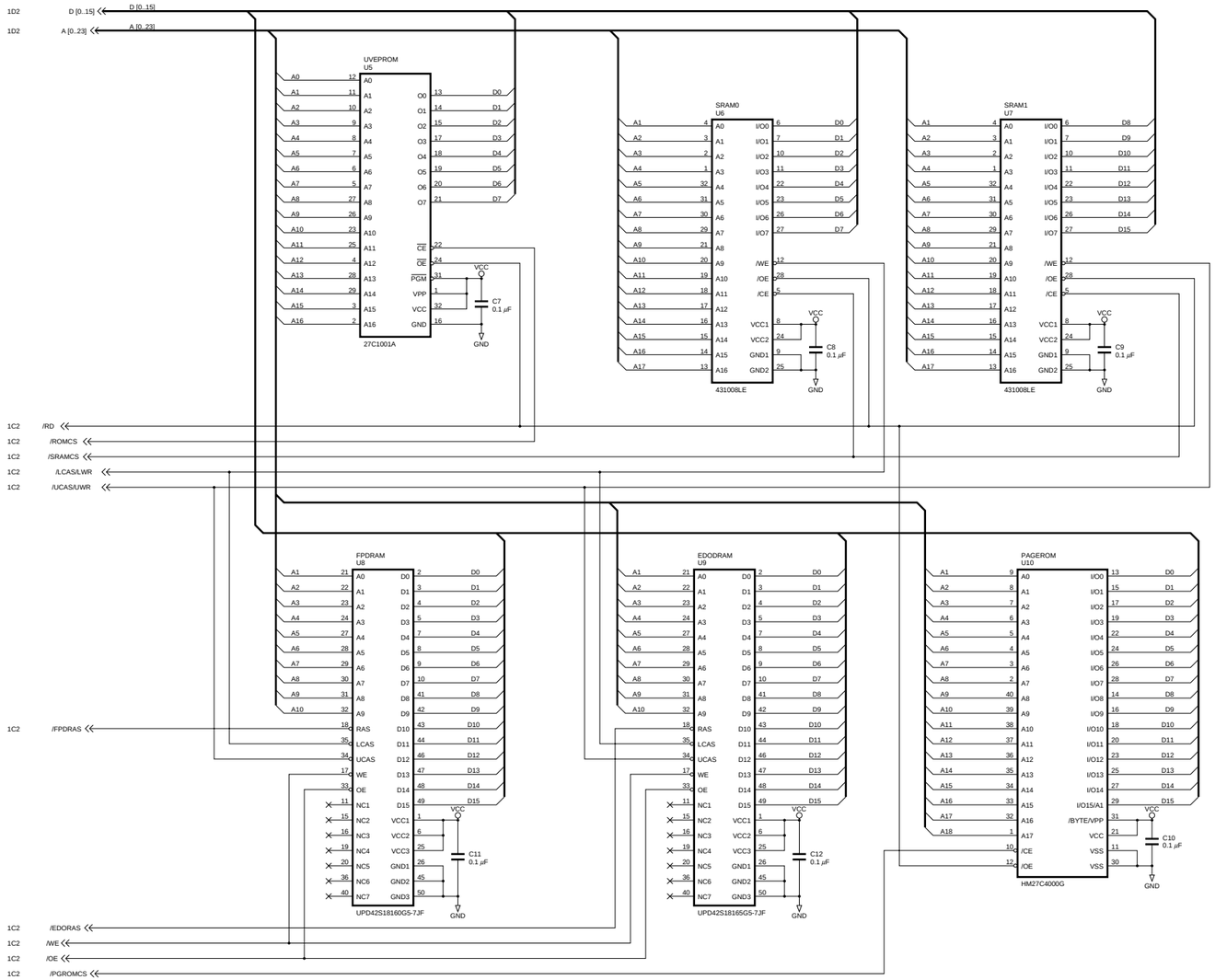


Figure 4-46. SDRAM and RS-232C

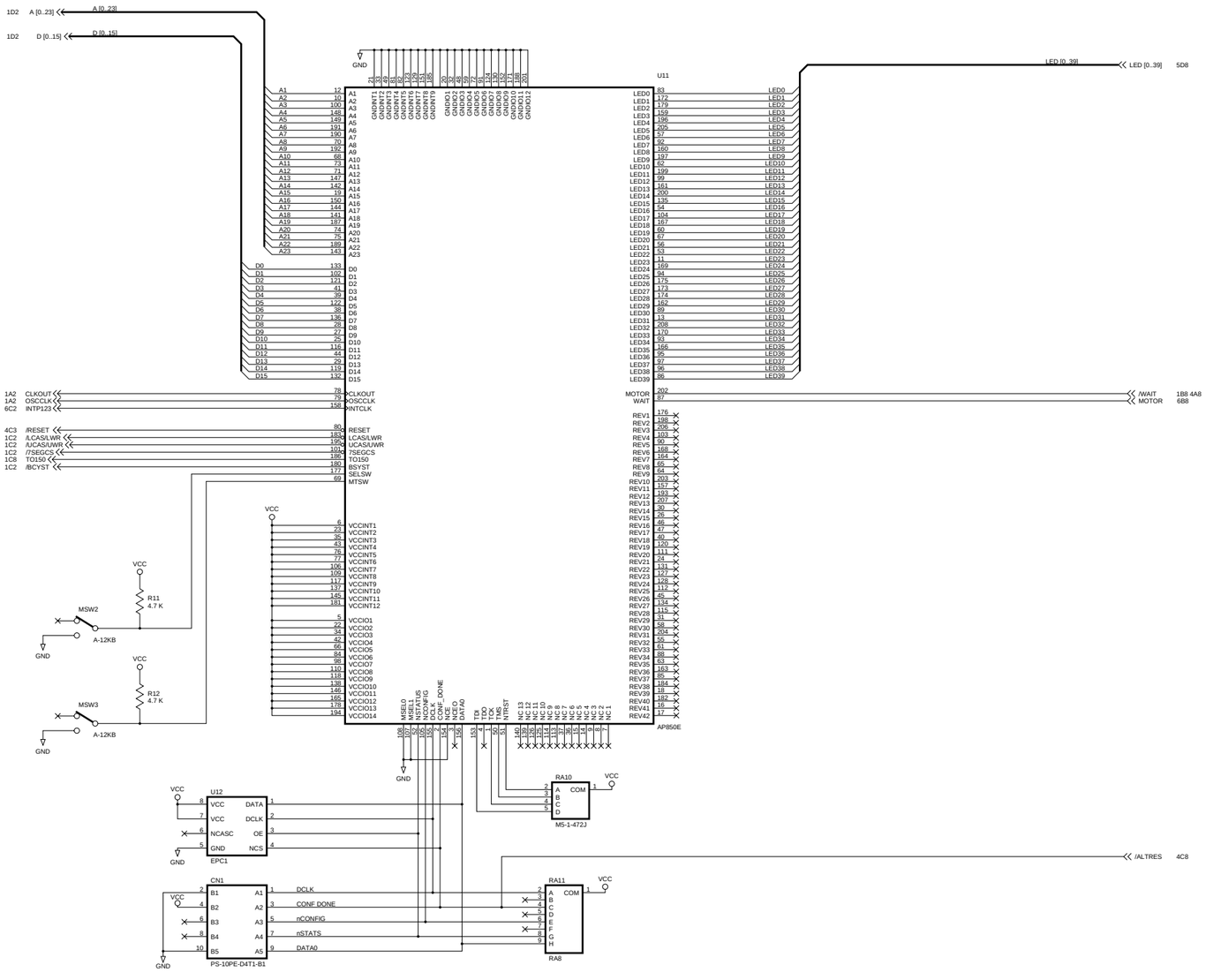


Figure 4-47. Flash Interface and Power

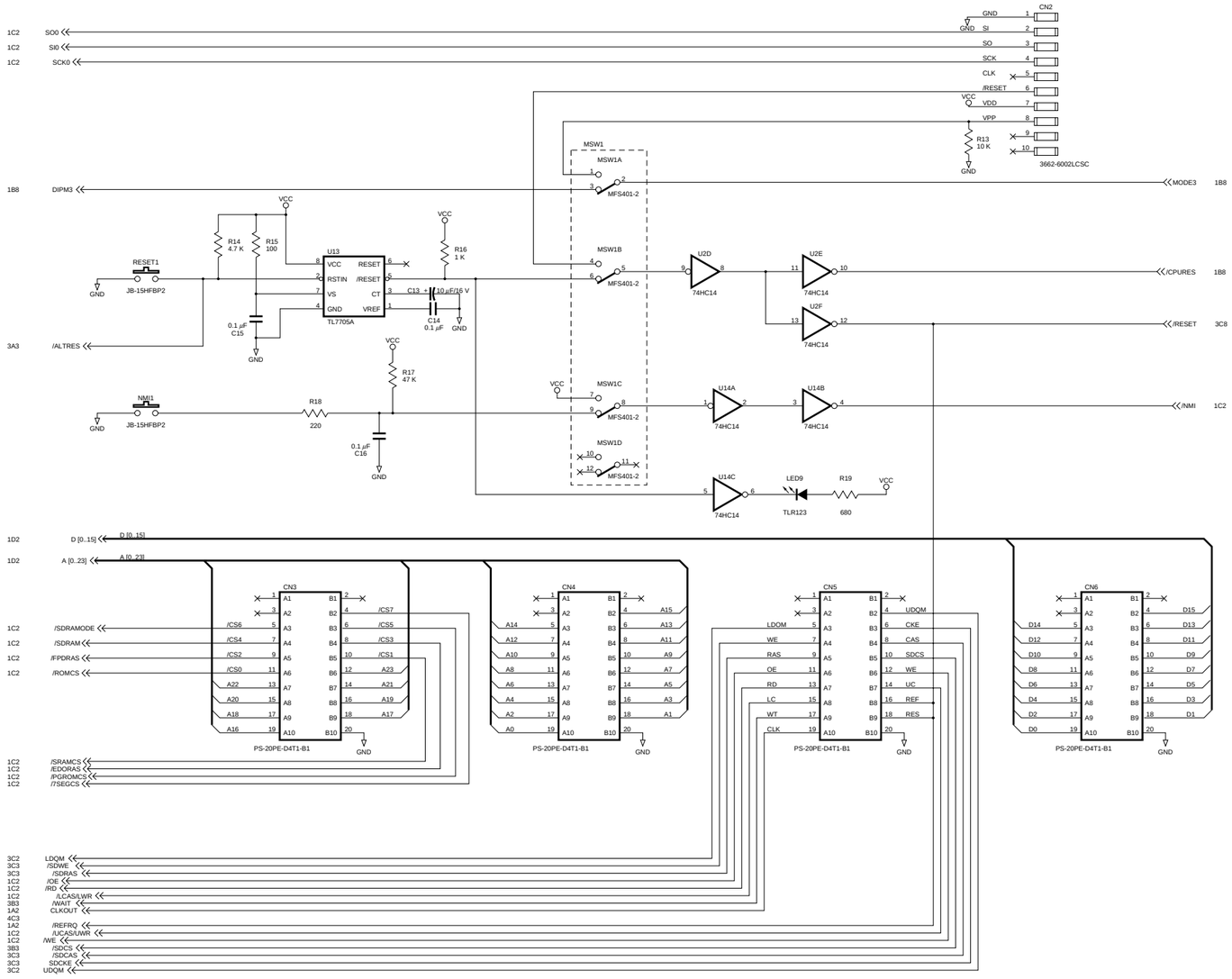


Figure 4-48. 7-Segment LED

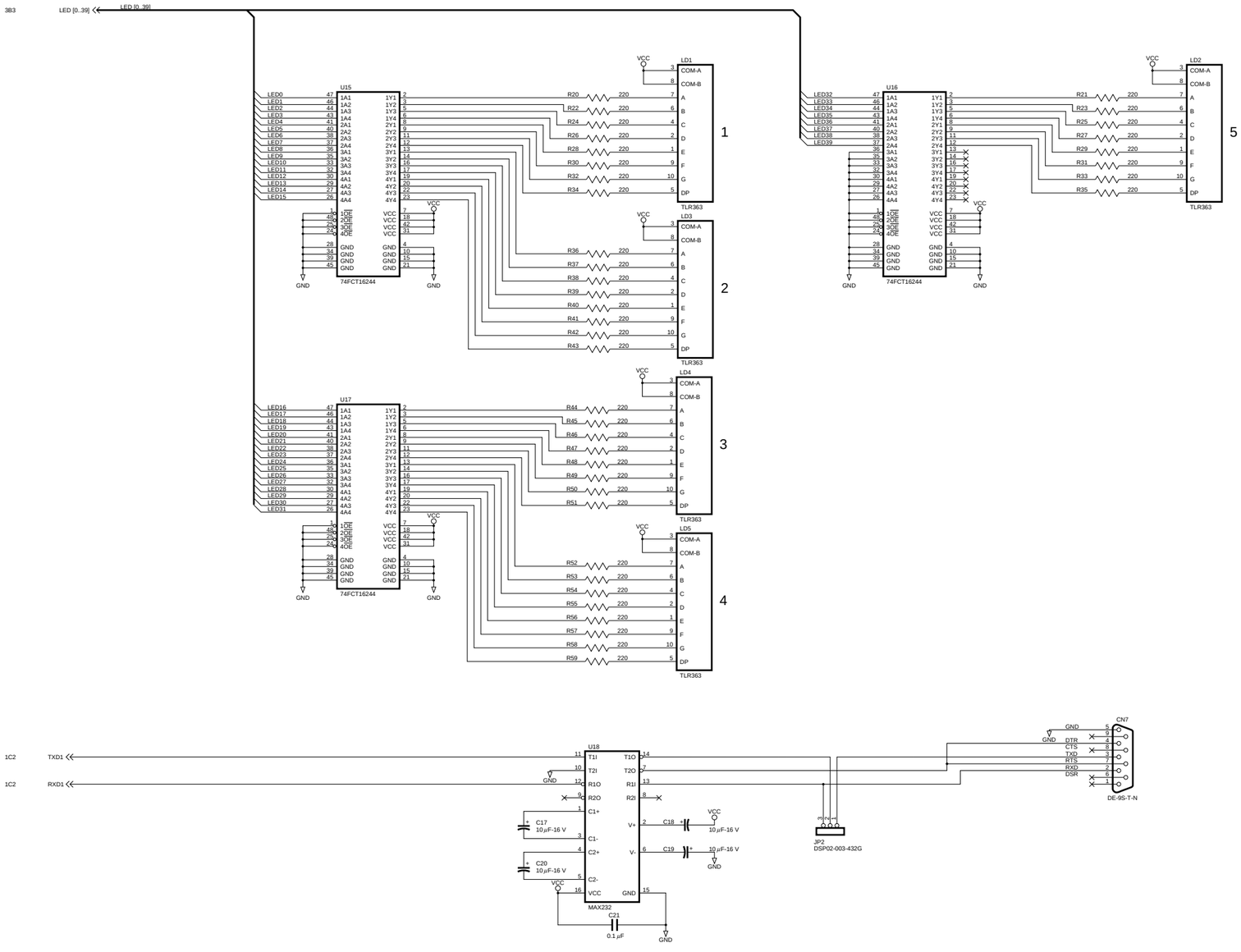
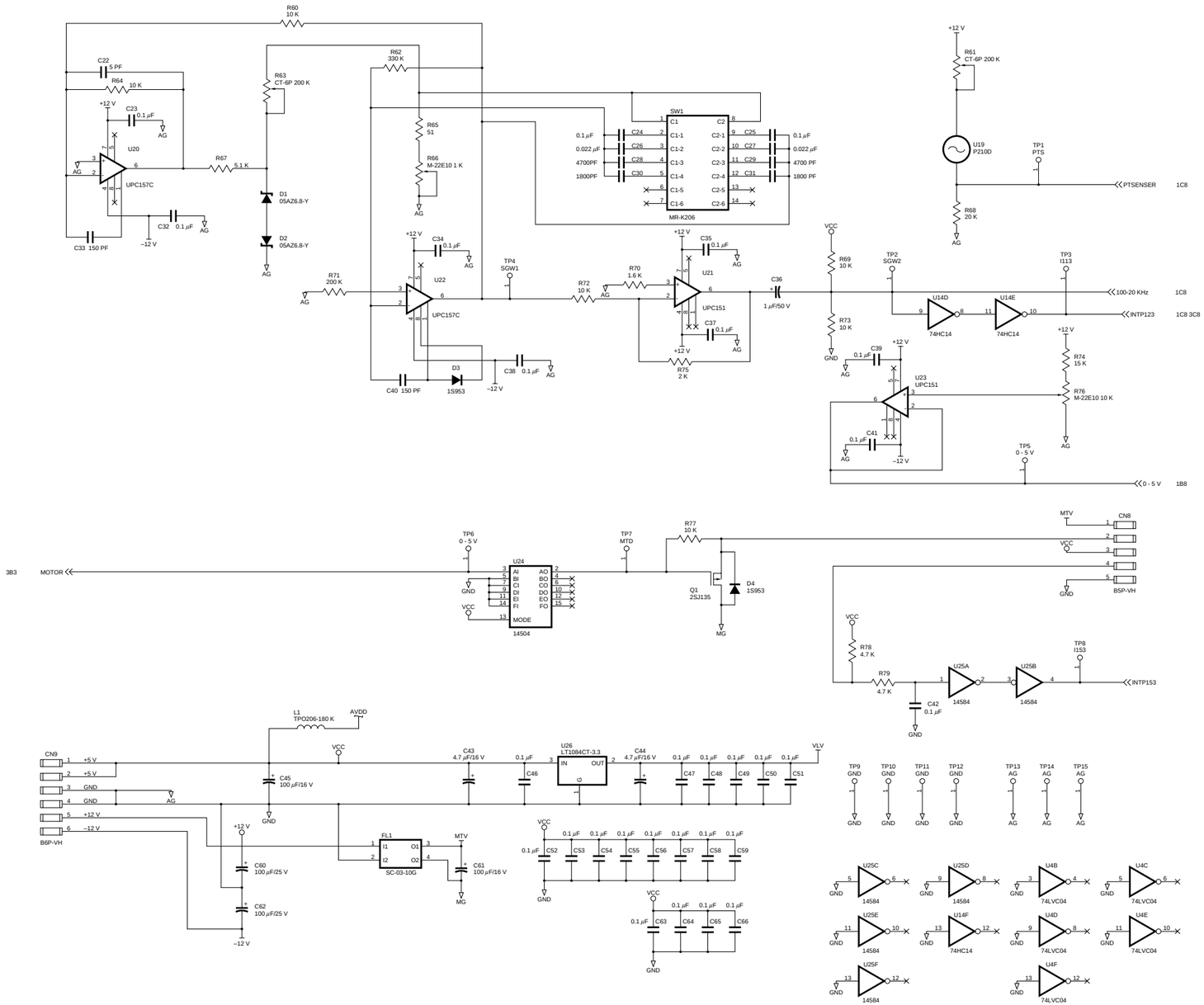


Figure 4-49. Analog Circuits



4.4.3 FPGA lists

The TB-V850E uses one FPGA (Field Programmable Gate Array). The data written to the FPGA is loaded from either the serial EEPROM or the connector (used for debugging) when a reset occurs.

The FPGAs' functions and lists are shown below.

Device used:	EPF10K10QC208-3
Part number in circuit:	U12
Circuit diagrams:	Figure 4-46. SDRAM and RS-232C
Functions:	Controls sine-wave generator's pulse count and 7-segment LED

List 4-1. 7-Segment LED Control (1 of 6)

```
SUBDESIGNfpga (
        clkout          :INPUT;
        reset           :INPUT;
        bcyst           :INPUT;
        a[23..1]        :INPUT;
        d[15..0]        :INPUT;
        lcas            :INPUT;
        ucas            :INPUT;
        intclk          :INPUT;
        oscclk          :INPUT;
        7segcs          :INPUT;
        selsw           :INPUT;
        to150           :INPUT;
        mtsw            :INPUT;
        wait            :OUTPUT;
        led[39..0]      :OUTPUT;
        motor           :OUTPUT;
)
VARIABLE
        cs[5..1]        :NODE;
        cpld[39..0]     :NODE;
        ctld[39..0]     :NODE;
        secres          :DFF;
        lca[3..0]       :DFF;
        lcb[3..0]       :DFF;
        lcc[3..0]       :DFF;
        lcd[3..0]       :DFF;
        lce[3..0]       :DFF;
        lcad[3..0]      :DFF;
        lcbd[3..0]      :DFF;
        lccd[3..0]      :DFF;
        lcdd[3..0]      :DFF;
        lced[3..0]      :DFF;
        coa             :NODE;
        cob             :NODE;
        coc             :NODE;
        cod             :NODE;
        ltca[3..0]      :NODE;
        ltcb[3..0]      :NODE
        ltcc[3..0]      :NODE;
        ltcd[3..0]      :NODE;
        ltce[3..0]      :NODE;
        sec[23..0]      :DFF;
        onesec          :NODE;
```

List 4-1. 7-Segment LED Control (2 of 6)

```
BEGIN

wait                    = vcc;

!csl                    =!7segcs&!a3&!a2&!a1&!lcas&ucas
                        & a23&a22&a21&!a20;

!cs2                    =!7segcs&!a3&!a2& a1&!lcas&ucas
                        & a23&a22&a21&!a20;

!cs3                    =!7segcs&!a3& a2&!a1&!lcas&ucas
                        & a23&a22&a21&!a20;

!cs4                    =!7segcs&!a3& a2& a1&!lcas&ucas
                        & a23&a22&a21&!a20;

!cs5                    =!7segcs& a3&!a2&!a1&!lcas&ucas
                        & a23&a22&a21&!a20;

cpld0                   =DFF (d0,cs1,reset,vcc);
cpld1                   =DFF (d1,cs1,reset,vcc);
cpld2                   =DFF (d2,cs1,reset,vcc);
cpld3                   =DFF (d3,cs1,reset,vcc);
cpld4                   =DFF (d4,cs1,reset,vcc);
cpld5                   =DFF (d5,cs1,reset,vcc);
cpld6                   =DFF (d6,cs1,reset,vcc);
cpld7                   =DFF (d7,cs1,reset,vcc);

cpld8                   =DFF (d0,cs2,reset,vcc);
cpld9                   =DFF (d1,cs2,reset,vcc);
cpld10                  =DFF (d2,cs2,reset,vcc);
cpld11                  =DFF (d3,cs2,reset,vcc);
cpld12                  =DFF (d4,cs2,reset,vcc);
cpld13                  =DFF (d5,cs2,reset,vcc);
cpld14                  =DFF (d6,cs2,reset,vcc);
cpld15                  =DFF (d7,cs2,reset,vcc);

cpld16                  =DFF (d0,cs3,reset,vcc);
cpld17                  =DFF (d1,cs3,reset,vcc);
cpld18                  =DFF (d2,cs3,reset,vcc);
cpld19                  =DFF (d3,cs3,reset,vcc);
cpld20                  =DFF (d4,cs3,reset,vcc);
cpld21                  =DFF (d5,cs3,reset,vcc);
cpld22                  =DFF (d6,cs3,reset,vcc);
cpld23                  =DFF (d7,cs3,reset,vcc);
```

List 4-1. 7-Segment LED Control (3 of 6)

```
cpld24                  =DFF (d0,cs4,reset,vcc);
cpld25                  =DFF (d1,cs4,reset,vcc);
cpld26                  =DFF (d2,cs4,reset,vcc);
cpld27                  =DFF (d3,cs4,reset,vcc);
cpld28                  =DFF (d4,cs4,reset,vcc);
cpld29                  =DFF (d5,cs4,reset,vcc);
cpld30                  =DFF (d6,cs4,reset,vcc);
cpld31                  =DFF (d7,cs4,reset,vcc);

cpld32                  =DFF (d0,cs5,reset,vcc);
cpld33                  =DFF (d1,cs5,reset,vcc);
cpld34                  =DFF (d2,cs5,reset,vcc);
cpld35                  =DFF (d3,cs5,reset,vcc);
cpld36                  =DFF (d4,cs5,reset,vcc);
cpld37                  =DFF (d5,cs5,reset,vcc);
cpld38                  =DFF (d6,cs5,reset,vcc);
cpld39                  =DFF (d7,cs5,reset,vcc);

secres.clk              =oscclk;
secres                  =onesec;

lca[].clk               =intclk;
lca[].clrn              =!secres;
lca[]                   =(lca[]+1) &! (lca[]==9);
!coa                    =(lca[]==9);
lcad[].clk              =!oscclk;
lcad[]                  =lca[];

lcb[].clk               =coa;
lcb[].clrn              =!secres;
lcb[]                   =(lcb[]+1) &! (lcb[]==9);
!cob                    =(lcb[]==9);
lcbd[].clk              =!oscclk;
lcbd[]                  =lcb[];

lcc[].clk               =cob;
lcc[].clrn              =!secres;
lcc[]                   =(lcc[]+1) &! (lcc[]==9);
!coc                    =(lcc[])==9);
lccd[].clk              =!oscclk;
lccd[]                  =lcc[];
```

List 4-1. 7-Segment LED Control (4 of 6)

```
lcd[].clk               =coc;
lcd[].clrn              =!secres;
lcd[]                   =(lcd[]+1) &! (lcd[]==9);
!cod                    =(lcd[]==9);
lcdd[].clk              =!oscclk;
lcdd[]                  =lcd[];

lce[].clk               =cod;
lce[].clrn              =!secres;
lce[]                   =(lce[]+1) &! (lce[]==9);
lced[].clk              =!oscclk;
lced[]                  =lce[];

ltca3                   =DFF (lcad3,onesec,reset,vcc);
ltca2                   =DFF (lcad2,onesec,reset,vcc);
ltca1                   =DFF (lcad1,onesec,reset,vcc);
ltca0                   =DFF (lcad0,onesec,reset,vcc);

ltcb3                   =DFF (lcbd3,onesec,reset,vcc);
ltcb2                   =DFF (lcbd2,onesec,reset,vcc);
ltcb1                   =DFF (lcbd1,onesec,reset,vcc);
ltcb0                   =DFF (lcbd0,onesec,reset,vcc);

ltcc3                   =DFF (lccd3,onesec,reset,vcc);
ltcc2                   =DFF (lccd2,onesec,reset,vcc);
ltcc1                   =DFF (lccd1,onesec,reset,vcc);
ltcc0                   =DFF (lccd0,onesec,reset,vcc);

ltcd3                   =DFF (lcdd3,onesec,reset,vcc);
ltcd2                   =DFF (lcdd2,onesec,reset,vcc);
ltcd1                   =DFF (lcdd1,onesec,reset,vcc);
ltcd0                   =DFF (lcdd0,onesec,reset,vcc);

ltce3                   =DFF (lced3,onesec,reset,vcc);
ltce2                   =DFF (lced2,onesec,reset,vcc);
ltce1                   =DFF (lced1,onesec,reset,vcc);
ltce0                   =DFF (lced0,onesec,reset,vcc);
```

List 4-1. 7-Segment LED Control (5 of 6)

```
TABLE
ltca[3..0]      ⇒     ctld0,    ctld1,    ctld2    ctld3,    ctld4,    ctld5,    ctld6;
H"0"            ⇒       1,        1,        1,        1,        1,        1,        0;
H"1"            ⇒       0,        1,        1,        0,        0,        0,        0;
H"2"            ⇒       1,        1,        0,        1,        1,        0,        1;
H"3"            ⇒       1,        1,        1,        1,        0,        0,        1;
H"4"            ⇒       0,        1,        1,        0,        0,        1,        1;
H"5"            ⇒       1,        0,        1,        1,        0,        1,        1;
H"6"            ⇒       1,        0,        1,        1,        1,        1,        1;
H"7"            ⇒       1,        1,        1,        0,        0,        0,        0;
H"8"            ⇒       1,        1,        1,        1,        1,        1,        1;
H"9"            ⇒       1,        1,        1,        1,        0,        1,        1;
END TABLE;

TABLE
ltcb[3..0]      ⇒     ctld8,    ctld9,    ctld10   ctld11,   ctld12,   ctld13,   ctld14;
H"0"            ⇒       1,        1,        1,        1,        1,        1,        0;
H"1"            ⇒       0,        1,        1,        0,        0,        0,        0;
H"2"            ⇒       1,        1,        0,        1,        1,        0,        1;
H"3"            ⇒       1,        1,        1,        1,        0,        0,        1;
H"4"            ⇒       0,        1,        1,        0,        0,        1,        1;
H"5"            ⇒       1,        0,        1,        1,        0,        1,        1;
H"6"            ⇒       1,        0,        1,        1,        1,        1,        1;
H"7"            ⇒       1,        1,        1,        0,        0,        0,        0;
H"8"            ⇒       1,        1,        1,        1,        1,        1,        1;
H"9"            ⇒       1,        1,        1,        1,        0,        1,        1;
END TABLE;

TABLE
ltcc[3..0]      ⇒     ctld16,   ctld17,   ctld18   ctld19,   ctld20,   ctld21,   ctld22;
H"0"            ⇒       1,        1,        1,        1,        1,        1,        0;
H"1"            ⇒       0,        1,        1,        0,        0,        0,        0;
H"2"            ⇒       1,        1,        0,        1,        1,        0,        1;
H"3"            ⇒       1,        1,        1,        1,        0,        0,        1;
H"4"            ⇒       0,        1,        1,        0,        0,        1,        1;
H"5"            ⇒       1,        0,        1,        1,        0,        1,        1;
H"6"            ⇒       1,        0,        1,        1,        1,        1,        1;
H"7"            ⇒       1,        1,        1,        0,        0,        0,        0;
H"8"            ⇒       1,        1,        1,        1,        1,        1,        1;
H"9"            ⇒       1,        1,        1,        1,        0,        1,        1;
END TABLE;
```

List 4-1. 7-Segment LED Control (6 of 6)

```
TABLE
ltcd[3..0]     ⇒     ctld24,   ctld25,   ctld26   ctld27,   ctld28,   ctld29,   ctld30;
H"0"           ⇒       1,        1,        1,        1,        1,        1,        0;
H"1"           ⇒       0,        1,        1,        0,        0,        0,        0;
H"2"           ⇒       1,        1,        0,        1,        1,        0,        1;
H"3"           ⇒       1,        1,        1,        1,        0,        0,        1;
H"4"           ⇒       0,        1,        1,        0,        0,        1,        1;
H"5"           ⇒       1,        0,        1,        1,        0,        1,        1;
H"6"           ⇒       1,        0,        1,        1,        1,        1,        1;
H"7"           ⇒       1,        1,        1,        0,        0,        0,        0;
H"8"           ⇒       1,        1,        1,        1,        1,        1,        1;
H"9"           ⇒       1,        1,        1,        1,        0,        1,        1;
END TABLE;

TABLE
ltce[3..0]     ⇒     ctld32,   ctld33,   ctld34   ctld35,   ctld36,   ctld37,   ctld38;
H"0"           ⇒       1,        1,        1,        1,        1,        1,        0;
H"1"           ⇒       1,        1,        0,        1,        1,        0,        1;
H"3"           ⇒       1,        1,        1,        1,        0,        0,        1;
H"4"           ⇒       0,        1,        1,        0,        0,        1,        1;
H"5"           ⇒       1,        0,        1,        1,        0,        1,        1;
H"6"           ⇒       1,        0,        1,        1,        1,        1,        1;
H"7"           ⇒       1,        1,        1,        0,        0,        0,        0;
H"8"           ⇒       1,        1,        1,        1,        1,        1,        1;
H"9"           ⇒       1,        1,        1,        1,        0,        1,        1;
END TABLE;

ctld7          =GND
ctld15         =GND
ctld23         =GND
ctld31         =GND
ctld39         =GND

!led[39..0]    =cpld[39..0]& selsw
               #ctld[39..0]&!selsw;

sec[].clk      =oscclk:-- 4MHz
sec[]          = (sec[]+1) &      (sec[]==4000000);
onesec         = (sec[]==4000000);

motor          =mtsw&to150;

END;
```

[MEMO]

APPENDIX INDEX

[R]

[S]

[T]

NEC

Facsimile Message

Although NEC has taken all possible steps to ensure that the documentation supplied to our customers is complete, bug free and up-to-date, we readily accept that errors may occur. Despite all the care and precautions we've taken, you may encounter problems in the documentation. Please complete this form whenever you'd like to report errors or suggest improvements to us.

From:

Name

Company

Tel. FAX

Address

Thank you for your kind support.

North America
NEC Electronics Inc.
Corporate Communications Dept.
Fax: 1-800-729-9288
1-408-588-6130

Europe
NEC Electronics (Europe) GmbH
Technical Documentation Dept.
Fax: +49-211-6503-274

South America
NEC do Brasil S.A.
Fax: +55-11-6462-6829

Hong Kong, Philippines, Oceania
NEC Electronics Hong Kong Ltd.
Fax: +852-2886-9022/9044

Korea
NEC Electronics Hong Kong Ltd.
Seoul Branch
Fax: 02-528-4411

Taiwan
NEC Electronics Taiwan Ltd.
Fax: 02-2719-5951

Asian Nations except Philippines
NEC Electronics Singapore Pte. Ltd.
Fax: +65-250-3583

Japan
NEC Semiconductor Technical Hotline
Fax: 044-435-9608

I would like to report the following error/make the following suggestion:

Document title: _____

Document number: _____ Page number: _____

If possible, please fax the referenced page or drawing.

Document Rating	Excellent	Good	Acceptable	Poor
Clarity	❑	❑	❑	❑
Technical Accuracy	❑	❑	❑	❑
Organization	❑	❑	❑	❑