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Application Note

Inverter Control by V850 Microcontrollers

6-Phase PWM Output Control by Timer Q, Timer Q Option, Timer P, A/D Converters 0 and 1

V850E/IA3
V850E/IA4
V850ES/IK1
V850ES/IE2

Document No. U18600EJ1V0AN00 (1st edition)
Date Published April 2007 N CP(K)

[MEMO]

NOTES FOR CMOS DEVICES

① VOLTAGE APPLICATION WAVEFORM AT INPUT PIN

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (MAX) and V_{IH} (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (MAX) and V_{IH} (MIN).

② HANDLING OF UNUSED INPUT PINS

Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

③ PRECAUTION AGAINST ESD

A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

④ STATUS BEFORE INITIALIZATION

Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

⑤ POWER ON/OFF SEQUENCE

In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current.

The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

⑥ INPUT OF SIGNAL DURING POWER OFF STATE

Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements.

Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

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M8E 02. 11-1

INTRODUCTION

Cautions 1. This Application Note explains a case where the V850E/IA4 (μPD70F3186GC-8EU-A) is used as a representative microcontroller. Use this Application Note for your reference when using the V850E/IA4 (other than the μPD70F3186GC-8EU-A), V850E/IA3, V850ES/IK1, and V850ES/IE2.

2. Download the sample program used in this Application Note from the NEC Electronics Website (http://www.necel.com/).

3. When using sample programs, reference the following startup module and link directive file and adjust them if necessary.

- **Startup module: ia4crt.s**
- **Link directive file: ia4pwm.dir**

4. This sample program is provided for reference purposes only and operations are therefore not subject to guarantee by NEC Electronics Corporation. When using sample programs, customers are advised to sufficiently evaluate this product based on their systems, before use.

Target Readers

This Application Note is intended for users who understand the functions of the V850E/IA3, V850E/IA4, V850ES/IK1, and V850ES/IE2, and who design application systems that use these microcontrollers. The applicable products are shown below.

- V850E/IA3
  μPD703183, 70F3184
- V850E/IA4
  μPD703185, 703186, 70F3186
- V850ES/IK1
  μPD703327, 703329, 70F3329
- V850ES/IE2
  μPD70F3713, 70F3714

Purpose

This Application Note explains, for your reference, how to set a 6-phase PWM output mode and A/D conversion starting trigger timing using 16-bit timer/event counter Q0 (TMQ0), timer Q0 option (TMQOP0), 16-bit timer/event counter P0 (TMP0), and A/D converters 0 and 1 which are necessary for inverter control of a 3-phase motor by the V850E/IA3, V850E/IA4, V850ES/IK1, or V850ES/IE2.

Organization

This Application Note is divided into the following sections.

- Hardware configuration
- Control method
- Program configuration
- File configuration
- Flowchart
- Settings

How to Use This Manual

It is assumed that the reader of this Application Note has general knowledge in the fields of electrical engineering, logic circuits, and microcontrollers.

For details of hardware functions (especially register functions, setting methods, etc.) and electrical specifications

→ See the **V850E/IA3, V850E/IA4 Hardware User's Manual**, **V850ES/IK1 Hardware User's Manual**, and **V850ES/IE2 Hardware User's Manual**.

For details of instruction functions

→ See the **V850E1 Architecture User's Manual** and **V850ES Architecture User's Manual**.

Conventions

Data significance:	Higher digits on the left and lower digits on the right	
Active low representation:	$\overline{xxx}$ (overscore over pin or signal name)	
Memory map address:	Higher addresses on the top and lower addresses on the bottom	
Note:	Footnote for item marked with **Note** in the text	
Caution:	Information requiring particular attention	
Remark:	Supplementary information	
Numeric representation:	Binary ... xxxx or xxxxB	
	Decimal ... xxxx	
	Hexadecimal ... xxxxH	
Prefix indicating the power of 2 (address space, memory capacity):	K (kilo):	$2^{10} = 1,024$
	M (mega):	$2^{20} = 1,024^2$
	G (giga):	$2^{30} = 1,024^3$
Data type:	Word:	32 bits
	Halfword:	16 bits
	Byte:	8 bits

Product Differences

The differences between the V850E/IA4 and the V850E/IA3, V850ES/IK1, and V850ES/IE2 related to 16-bit timer/event counter Q (TMQ), timer Q option (TMQOP), 16-bit timer/event counter P (TMP), and A/D converters 0 and 1 are shown below.

Item		V850E/IA4	V850E/IA3	V850ES/IK1	V850ES/IE2
TMQ	TOQ10 pin	Available	None	Available	
	TRGQ0 pin	Available	Available	None	
	TOQH01 to TOQH03 pins	None	None	Available	
	TOQ00 pin	TOQ00	TOQ00	TOQ00 (CLMER)	
	Count clock	$f_{XX}/2$, $f_{XX}/4$, $f_{XX}/8$, $f_{XX}/16$, $f_{XX}/32$, $f_{XX}/64$, $f_{XX}/128$, $f_{XX}/256$	$f_{XX}/2$, $f_{XX}/4$, $f_{XX}/8$, $f_{XX}/16$, $f_{XX}/32$, $f_{XX}/64$, $f_{XX}/128$, $f_{XX}/256$	f_{XX}, $f_{XX}/2$, $f_{XX}/4$, $f_{XX}/8$, $f_{XX}/16$, $f_{XX}/32$, $f_{XX}/64$, $f_{XX}/128$	
TMQOP	TOQ0T1 to TOQ0T3 pins	Available	Available	None	
	TOQ0B1 to TOQ0B3 pins	Available	Available	None	
	TOQ1T1 to TOQ1T3 pins	Available	None	Available	
	TOQ1B1 to TOQ1B3 pins	Available	None	Available	
	TOQ0OFF	Available	Available	None	
	TOQ1OFF	Available	None	Available	
	TOP3OFF	Available	None	Available	
	TOQH0OFF	None	None	Available	
	Forced output stop function (at overvoltage detection by comparator function of A/D converter block)	Available	Available	None	
TMP	TOP31 pin	Available	None	Available	
	Count clock	$f_{XX}/2$, $f_{XX}/4$, $f_{XX}/8$, $f_{XX}/16$, $f_{XX}/32$, $f_{XX}/64$, $f_{XX}/128$, $f_{XX}/256$	$f_{XX}/2$, $f_{XX}/4$, $f_{XX}/8$, $f_{XX}/16$, $f_{XX}/32$, $f_{XX}/64$, $f_{XX}/128$, $f_{XX}/256$	f_{XX}, $f_{XX}/2$, $f_{XX}/4$, $f_{XX}/8$, $f_{XX}/16$, $f_{XX}/32$, $f_{XX}/64$, $f_{XX}/128$	
A/D converters 0, 1	Analog input	Total of two circuits: 8 ch A/D converter 0: 4 ch A/D converter 1: 4 ch	Total of two circuits: 6 ch A/D converter 0: 2 ch A/D converter 1: 4 ch	Total of two circuits: 8 ch A/D converter 0: 4 ch A/D converter 1: 4 ch	
	Operational amplifier for input level amplification	Total of two circuits: 6 ch A/D converter 0: 3 ch A/D converter 1: 3 ch	Total of two circuits: 5 ch A/D converter 0: 2 ch A/D converter 1: 3 ch	None	
	Overvoltage detection comparator	Total of two circuits: 6 ch A/D converter 0: 3 ch A/D converter 1: 3 ch	Total of two circuits: 5 ch A/D converter 0: 2 ch A/D converter 1: 3 ch	None	
	AV_{DD0}, AV_{DD1}, AV_{REF0}, AV_{REF1}	Alternate-function pin	Alternate-function pin	Independent pin	

Remark f_{XX}: Peripheral clock frequency

Related Documents The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

Documents related to V850E/IA3, V850E/IA4, V850ES/IK1, and V850ES/IE2

Document Name	Document No.
V850E1 Architecture User's Manual	U14559E
V850E/IA3, V850E/IA4 Hardware User's Manual	U16543E
V850ES Architecture User's Manual	U15943E
V850ES/IK1 Hardware User's Manual	U16910E
V850ES/IE2 Hardware User's Manual	U17716E
Inverter Control by V850 Series Vector Control by Hole Sensor Application Note	U17338E
Inverter Control by V850 Series Vector Control by Encoder Application Note	U17324E
Inverter Control by V850 Series 120° Excitation Method Control by Zero-Cross Detection Application Note	U17209E
Manual for Using Sample Program Functions Serial Communication (UARTA) Application Note	U18233E
Manual for Using Sample Program Functions Serial Communication (CSIB) Application Note	U18234E
Manual for Using Sample Program Functions DMA Functions Application Note	U18235E
Manual for Using Sample Program Functions Timer M Application Note	U18236E
Manual for Using Sample Program Functions Watchdog Timer Application Note	U18237E
Manual for Using Sample Program Functions Timer P Application Note	U18238E
Manual for Using Sample Program Functions Timer Q Application Note	U18239E
Manual for Using Sample Program Functions Timer ENC Application Note	U18240E
Manual for Using Sample Program Functions Port Functions Application Note	U18241E
Manual for Using Sample Program Functions Clock Generator Application Note	U18242E
Manual for Using Sample Program Functions Standby Function Application Note	U18243E
Manual for Using Sample Program Functions Interrupt Functions Application Note	U18244E
Manual for Using Sample Program Functions A/D Converters 0 and 1 Application Note	U18245E
Manual for Using Sample Program Functions A/D Converter 2 Application Note	U18246E
Inverter Control by V850 Microcontrollers 6-Phase PWM Output Control by Timer Q, Timer Q Option, Timer P, A/D Converters 0 and 1 Application Note	This document

Documents related to development tools (user's manuals)

Document Name		Document No.
QB-V850EIA4 (In-circuit emulator for V850E/IA3, V850E/IA4, V850ES/IK1)		U17167E
QB-V850ESIX2 (In-circuit emulator for V850ES/IE2)		U17909E
QB-V850MINI (On-chip debug emulator for V850E/IA4)		U17638E
CA850 (Ver. 3.00) (C compiler package)	Operation	U17293E
	C Language	U17291E
	Assembly Language	U17292E
	Link Directive	U17294E
PM+ (Ver. 6.00) (Project manager)		U17178E
ID850 (Ver. 3.00) (Integrated debugger)	Operation	U17358E
ID850QB (Ver. 3.20) (Integrated debugger)	Operation	U17964E
TW850 (Ver. 2.00) (Performance analysis tuning tool)		U17241E
RX850 (Ver. 3.20) (Real-time OS)	Basics	U13430E
	Installation	U17419E
	Technical	U13431E
	Task Debugger	U17420E
RX850 Pro (Ver. 3.20) (Real-time OS)	Basics	U13773E
	Installation	U17421E
	Technical	U13772E
	Task Debugger	U17422E
AZ850 (Ver. 3.30) (System performance analyzer)		U17423E
PG-FP4 Flash Memory Programmer		U15260E

CONTENTS

CHAPTER 1 HARDWARE CONFIGURATION

This chapter describes the hardware configuration of the 3-phase PWM driver.

1.1 Operation

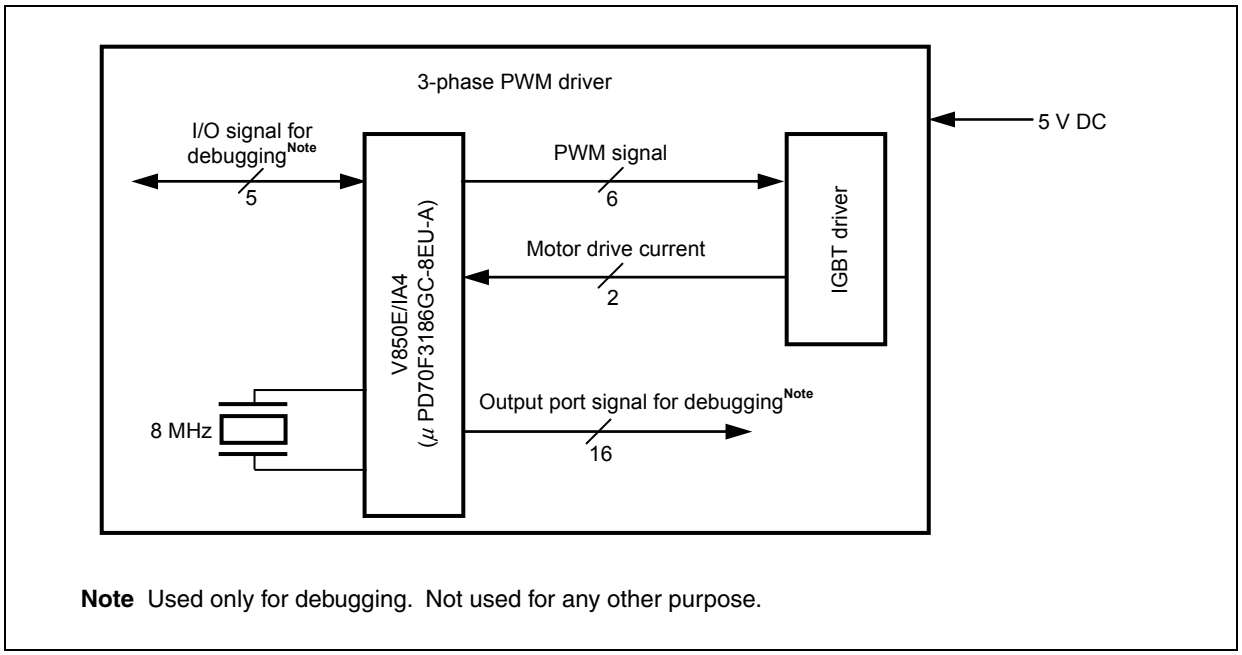
The following shows the main functions of the 3-phase PWM driver.

- Pulse duty for U, V, and W phases can be set freely by specifying the d axis, q axis, and rotational coordinates (θ).
- PWM pulse of the same duty can be continuously output in output lock mode.
- PWM output pins (TOQ0T1 to TOQ0T3, TOQ0B1 to TOQ0B3) can be set to high-impedance state by software.
- The start trigger for conversion of A/D converters 0 and 1 can be generated in synchronization with carrier cycles.

1.2 System Configuration

The system configuration is shown below.

Figure 1-1. System Configuration Diagram



Note Used only for debugging. Not used for any other purpose.

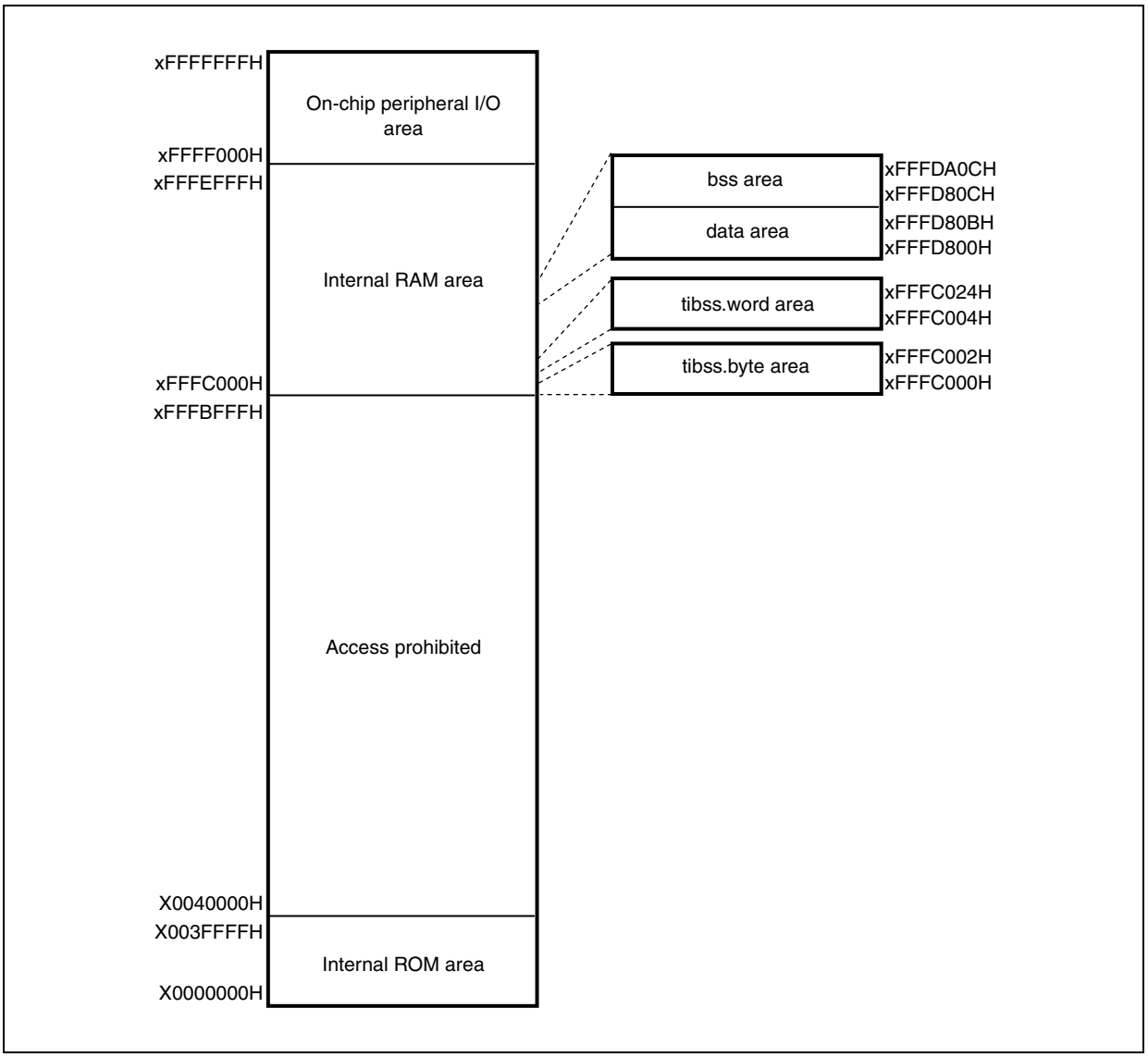
1.3 CPU Block

The 3-phase PWM driver inputs an 8 MHz clock to the V850E/IA4 (μPD70F3186GC-8EU-A) and operates at 64 MHz by multiplying the clock by eight. The internal RAM size of the V850E/IA4 (μPD70F3186GC-8EU-A) can be changed between 6 KB and 12 KB. Set the internal RAM size to 12 KB for the 3-phase PWM driver.

1.3.1 Memory map

The memory map is shown below.

Figure 1-2. Memory Map



1.3.2 Pin assignment

Pin assignments of the V850E/IA4 (μPD70F3186GC-8EU-A) are shown below.

Table 1-1. V850E/IA4 (μPD70F3186GC-8EU-A) Pin Assignment (1/3)

Pin No.	Pin Name	I/O Mode Setting	Signal Name	Active Level
1	ANI00	Input	Motor drive current for A/D converter 0	0 to +5 V
2	ANI01	–	Unused	–
3	ANI02	–		–
4	AIN03	–		–
5	P70	Input		–
6	P71	Input		–
7	P72	Input		–
8	P73	Input		–
9	AV_{DD}	–	Positive power supply for A/D converters 0 to 2	+5 V
10	AV_{SS}	–	Ground potential for A/D converters 0 to 2	GND
11	CMPREF	–	Unused	–
12	AV_{SS}	–	Ground potential for A/D converters 0 to 2	+5 V
13	AV_{DD}	–	Positive power supply for A/D converters 0 to 2	GND
14	P74	Input	Unused	–
15	P75	Input		–
16	P76	Input		–
17	P77	Input		–
18	ANI10	Input	Motor drive current for A/D converter 1	0 to +5 V
19	ANI11	–	Unused	–
20	ANI12	–		–
21	ANI13	–		–
22	P00	Input		–
23	P01	Input		–
24	P02	Input		–
25	P03	Input		–
26	P04	Input		–
27	P05	Input		–
28	P06	Input		–
29	P07	Input		–
30	V_{DD}	–	Positive power supply for internal unit	+2.5 V
31	V_{SS}	–	Ground potential for internal unit	GND
32	P40	Input	Unused	–
33	P41	Input		–
34	P42	Input		–
35	P20	Input		–
36	P21	Input		–
37	P22	Input		–
38	EV_{DD}	–	Positive power supply for external pin	5 V
39	EV_{SS}	–	Ground potential for external pin	GND

Table 1-1. V850E/IA4 (μPD70F3186GC-8EU-A) Pin Assignment (2/3)

Pin No	Pin Name	I/O Mode Setting	Signal Name	Active Level
40	P23	Input	Unused	–
41	P24	Input		–
42	P25	Input		–
43	CV_{DD}	–	Power supply for oscillator and PLL	+2.5 V
44	X2	–	System clock	–
45	X1	Input		–
46	CV_{SS}	–	Ground potential for oscillator and PLL	GND
47	$\overline{RESET}$	Input	System reset input	L
48	P43	Input	Unused	–
49	P44	Input		–
50	V_{DD}	–	Positive power supply for internal unit	+2.5 V
51	V_{SS}	–	Ground potential for internal unit	GND
52	P30	Input	Unused	–
53	P31	Input		–
54	P32	Input		–
55	P33	Input		–
56	P34	Input		–
57	P35	Input		–
58	P36	Input		–
59	P37	Input		–
60	P26	Input		–
61	P27	Input		–
62	PDL0	Input (output in debugging)	Output port for debugging	– (H in debugging)
63	PDL1	Input (output in debugging)		– (H in debugging)
64	V_{DD}	–	Positive power supply for internal unit	+2.5 V
65	V_{SS}	–	Ground potential for internal unit	GND
66	PDL2	Input (output in debugging)	Output port for debugging	– (H in debugging)
67	PDL3	Input (output in debugging)		– (H in debugging)
68	PDL4	Input (output in debugging)		– (H in debugging)
69	PDL5	Input (output in debugging)		– (H in debugging)
70	PDL6	Input (output in debugging)		– (H in debugging)
71	PDL7	Input (output in debugging)		– (H in debugging)
72	EV_{SS}	–	Ground potential for external pin	GND
73	EV_{DD}	–	Positive power supply for external pin	+5 V
74	PDL8	Input (output in debugging)	Output port for debugging	– (H in debugging)
75	PDL9	Input (output in debugging)		– (H in debugging)
76	PDL10	Input (output in debugging)		– (H in debugging)
77	PDL11	Input (output in debugging)		– (H in debugging)
78	PDL12	Input (output in debugging)		– (H in debugging)
79	PDL13	Input (output in debugging)		– (H in debugging)
80	PDL14	Input (output in debugging)		– (H in debugging)

Remark L: low level

H: high level

Table 1-1. V850E/IA4 (μPD70F3186GC-8EU-A) Pin Assignment (3/3)

Pin No	Pin Name	I/O Mode Setting	Signal Name	Active Level
81	PDL15	Input (output in debugging)	Output port for debugging	– (H in debugging)
82	DDI	Input	Debug data input for on-chip debug emulator (used only in debugging)	L
83	DCK	Input	Debug clock input for on-chip debug emulator (used only in debugging)	L
84	DMS	Input	Debug mode select for on-chip debug emulator (used only in debugging)	L
85	V_{SS}	–	Ground potential for internal unit	GND
86	V_{DD}	–	Positive power supply for internal unit	+2.5 V
87	FLMD0	Input	Flash memory programming mode setting pin	H
88	TOQ0T1	Output	U phase output	–
89	TOQ0B1	Output	$\overline{U}$ phase output	–
90	TOQ0T2	Output	V phase output	–
91	EV_{SS}	–	Ground potential for external pin	GND
92	EV_{DD}	–	Positive power supply for external pin	+5 V
93	TOQ0B2	Output	$\overline{V}$ phase output	–
94	TOQ0T3	Output	W phase output	–
95	TOQ0B3	Output	$\overline{W}$ phase output	–
96	P16	Input	Unused	–
97	P17	Input		–
98	DDO	Output	Debug data output for on-chip debug emulator (used only in debugging)	L
99	$\overline{DRST}$	Input	Debug reset input for on-chip debug emulator (used only in debugging)	L
100	PLLSIN	Input	Output frequency select signal input in PLL mode	+5 V

Remark L: low level

H: high level

1.3.3 On-chip peripheral I/O

The following peripheral I/Os are used in the 3-phase PWM driver.

Table 1-2. On-Chip Peripheral I/Os Used

On-Chip Peripheral I/O Function Name (V850E/IA4 (μPD70F3186GC-8EU-A))	Function
PDL0 to PDL15	For debugging (used only for debugging, not used for any other purpose)
Timer Q0 (TMQ0) + TMQ0 option (TMQOP0) + Timer P0 (TMP0)	PWM output
ANI00	Motor drive current for A/D converter 0
ANI10	Motor drive current for A/D converter 1
On-chip debug function	Using on-chip debug unit

(1) Description of on-chip peripheral I/O function

(a) Output ports for debugging

Ports used in program debugging. Do not input/output for any other purpose.

(b) PWM output

- TMQ0: Sets the PWM timer count and duty factor in 6-phase PWM output mode.
- TMQOP0: Appends a dead time to PWM, generated by TMQ0.
- TMP0: Synchronizes TMQ0 and TMP0, and generates the start trigger for conversion of A/D converters 0 and 1.

PWM settings by the 3-phase PWM driver are as follows.

Carrier frequency: 20 kHz
Dead time: 4 μs
Culling rate: 1/1

Table 1-3. PWM Output Pin Output Level

TOQ0T1 to TOQ0T3, TOQ0B1 to TOQ0B3	Output Level
Before execution of CALL instruction for 3-phase PWM	High impedance
While 3-phase PWM driver is operating	High impedance/high level/low level

(c) ANI00

In response to the trigger from TMP0, performs A/D conversion of the ANI00 value. After the A/D conversion completes, generates the A/D0 conversion completion interrupt (INTAD0) of the priority level 4.

ANI00: 0 to +5 V
Synchronization trigger timing: 1 μs after the TMQ0 valley interrupt (INTTQ0OV) of carrier cycle
A/D conversion completion time: 1.94 μs

(d) ANI10

In response to the trigger from TMP0, performs A/D conversion of the ANI10 value. After the A/D conversion completes, generates the A/D1 conversion completion interrupt (INTAD1) of the priority level 4.

ANI10: 0 to +5 V
Synchronization trigger timing: 1 μs after the TMQ0 trough interrupt (INTTQ0OV) of carrier cycle
A/D conversion completion time: 1.94 μs

(e) On-chip debug function

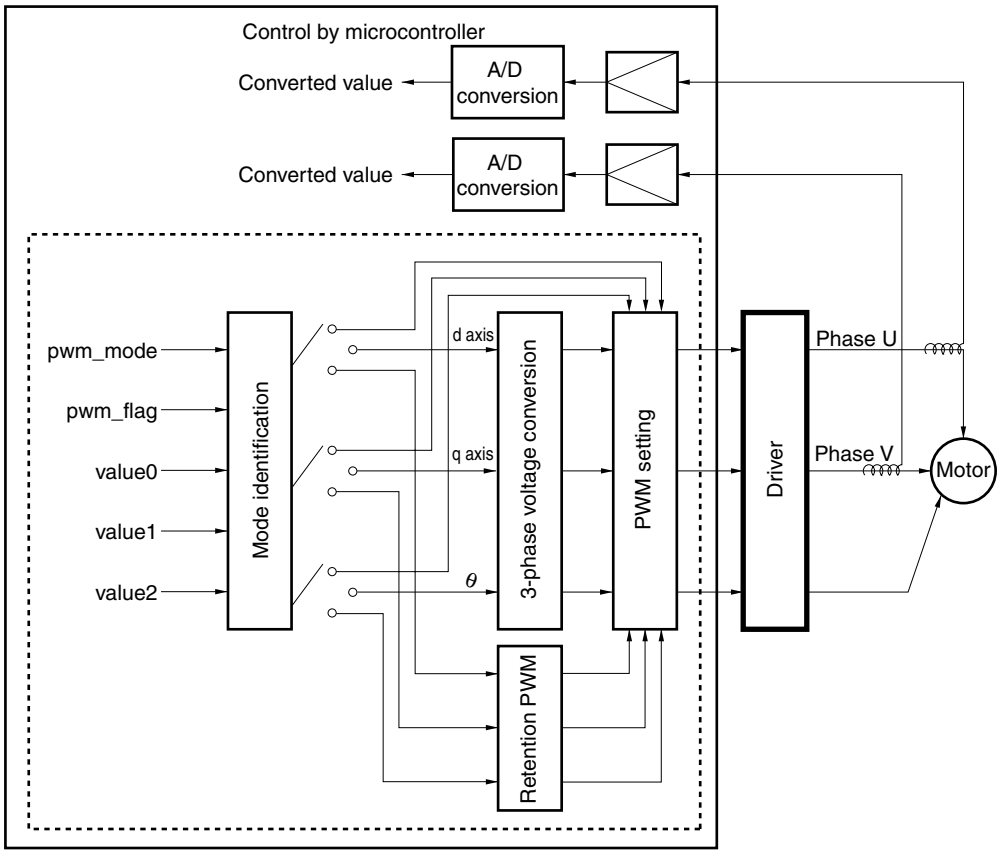
The V850E/IA4 (μPD70F3186GC-8EU-A) includes an on-chip debug unit and implements the on-chip debugging by itself, using the on-chip debug emulator connected.
For how to connect to the on-chip debug emulator, refer to manuals of the debugger used.

CHAPTER 2 CONTROL METHOD

2.1 Control Block

The control block diagram of the 3-phase PWM driver is shown below.

Figure 2-1. 3-Phase PWM Driver Control Block Diagram



Remark Processing enclosed by broken lines indicates the processing by software.
Processing of the driver, denoted by a heavy solid line, varies depending on the driving motor used, so the driver should be designed by users.

(1) Mode identification

Mode of the 3-phase PWM driver can be identified in accordance with the software state.

Modes of the 3-phase PWM driver are as follows.

- Direct mode: PWM duty ratio set by value0 to value2 is used as the PWM voltage.
- dq conversion mode: PWM voltage is determined by d axis voltage, q axis voltage, and rotation position (θ).
- Output lock mode: PWM voltage previously set by the 3-phase PWM driver is output.

(2) 3-phase voltage conversion

Coordinate transformation processing is performed in the dq conversion mode.

(3) Retention PWM

PWM voltage previously set by the 3-phase PWM driver is retained.

(4) PWM setting

PWM voltage is calculated and output to registers of the V850E/IA4 (μPD70F3186GC-8EU-A).

2.2 3-Phase Voltage Conversion

The following shows the formula to convert the dq axes voltage into the 3-phase coordinate.

Phase U voltage = (d axis voltage $\times \sin(\theta + 90°)$) − (q axis voltage $\times \sin(\theta)$)

Phase V voltage = (d axis voltage $\times \sin(\theta + 330°)$) − (q axis voltage $\times \sin(\theta + 240°)$)

Phase W voltage = −Phase U voltage − Phase V voltage

2.3 Register Settings

(1) System wait control register (VSWC)

Set the VSWC register as follows.

VSWC register = 13H

VSWC — Address: FFFFF06EH

	7	6	5	4	3	2	1	0
After reset	0	1	1	1	0	1	1	1
Bit name	–	–	–	–	–	–	–	–
Set value	0	0	0	1	0	0	1	1

Wait for bus access to the on-chip peripheral I/O register
4 waits in 64 MHz operation

Caution Set the VSWC register by using the startup module (ia4crt.s).

(2) Internal memory size switching register (IMS)

Set the IMS register as follows.

IMS register = 01H

IMS — Address: FFFFF9F0H

	7	6	5	4	3	2	1	0
After reset	0	0	0	0	0	0	0	0
Bit name	0	0	0	0	0	0	0	IRAM0
Set value	0	0	0	0	0	0	0	1

IRAM0	Specification of internal RAM size
1	12 KB (FFFC000H to FFFEFFFH)

Caution Set the IMS register by using the startup module (ia4crt.s).

(3) PLL control register (PLLCTL)

Set the PLLCTL register as follows.

PLLCTL register = 03H

PLLCTL Address: FFFFF82CH

	7	6	5	4	3	2	1	0
After reset	0	0	0	0	0	0	0	1
Bit name	0	0	0	0	0	0	SELPLL	1
Set value	0	0	0	0	0	0	1	1

SELPLL	CPU operation clock selection
1	PLL mode

Caution Be sure to set bits 7 to 2 to "0" and set bit 0 to "1".

(4) Processor clock control register (PCC)

Set the PCC register as follows.

PCC register = 00H

PCC Address: FFFFF828H

	7	6	5	4	3	2	1	0
After reset	0	0	0	0	0	0	1	1
Bit name	0	0	0	0	0	0	CK1	CK0
Set value	0	0	0	0	0	0	0	0

CK1	CK0	Clock selection (f_{CLK}/f_{CPU})
0	0	f_{XX}

Cautions 1. The PCC register is a special register. Data can be written to this register only in a combination of specific sequences. For details, refer to 3.4.8 Special registers in the V850E/IA3, V850E/IA4 Hardware User's Manual (U16543E).

2. Be sure to set bits 2 to 7 to "0".

3. Set the PCC register after the PLL mode is selected (PLLCTL.SELPLL bit = 1).

(5) Power save control register (PSC)

Set the PSC register as follows.

PSC register = 00H

PSC — Address: FFFFF1FEH

	7	6	5	4	3	2	1	0
After reset	0	0	0	0	0	0	0	0
Bit name	0	0	0	INTM	0	0	STB	0
Set value	0	0	0	0	0	0	0	0

INTM	Standby mode control by maskable interrupt request (INTxx[Note])
0	Standby mode release by INTxx request enabled

STB	Operation mode selection
0	Normal mode

Note For details, see **Table 17-1 Interrupt Source List** in the **V850E/IA3, V850E/IA4 Hardware User's Manual (U16543E)**.

Cautions 1. The PSC register is a special register. Data can be written to this register only in a combination of specific sequences. For details, refer to 3.4.8 Special registers in the V850E/IA3, V850E/IA4 Hardware User's Manual (U16543E).

2. Be sure to set bits 0, 2, 3, and 5 to 7 to "0".

(6) Power save mode register (PSMR)

Set the PSMR register as follows.

PSMR register = 00H

PSMR — Address: FFFFF820H

	7	6	5	4	3	2	1	0
After reset	0	0	0	0	0	0	0	0
Bit name	0	0	0	0	0	0	0	PSM0
Set value	0	0	0	0	0	0	0	0

PSM0	Operation specification in software standby mode
0	IDLE mode

Cautions 1. Be sure to set bits 1 to 7 to "0".

2. The PSM0 bit is valid only when the PSC.STB bit is 1.

(7) Oscillation stabilization time select register (OSTS)

Set the OSTS register as follows.

OSTS register = 04H

OSTS — Address: FFFFF6C0H

	7	6	5	4	3	2	1	0
After reset	0	0	0	0	0	1	0	0
Bit name	0	0	0	0	OSTS3	OSTS2	OSTS1	OSTS0
Set value	0	0	0	0	0	1	0	0

OSTS3	OSTS2	OSTS1	OSTS0	Selection of oscillation stabilization time (f_X = 8 MHz)
0	1	0	0	$2^{14}/f_X$ (2.05 ms)

Caution Be sure to set bits 4 to 7 to "0".

(8) Clock monitor mode register (CLM)

Set the CLM register as follows.

CLM register = 00H

CLM — Address: FFFFF870H

	7	6	5	4	3	2	1	0
After reset	0	0	0	0	0	0	0	0
Bit name	0	0	0	0	0	0	0	CLME
Set value	0	0	0	0	0	0	0	0

CLME	Clock monitor operation control
0	Clock monitor operation disabled

Caution The CLM register is a special register. Data can be written to this register only in a combination of specific sequences. For details, refer to 3.4.8 Special registers in the V850E/IA3, V850E/IA4 Hardware User's Manual (U16543E).

(9) Port 1 mode control register (PMC1)

Set the PMC1 register as follows.

PMC1 register = 3FH

PMC1 Address: FFFFF442H

	7	6	5	4	3	2	1	0
After reset	0	0	0	0	0	0	0	0
Bit name	PMC17	PMC16	PMC15	PMC14	PMC13	PMC12	PMC11	PMC10
Set value	0	0	1	1	1	1	1	1

PMC17	Specification of operating mode of P17 pin
0	I/O port

PMC16	Specification of operating mode of P16 pin
0	I/O port

PMC15	Specification of operating mode of P15 pin
1	TOQ0B3 output/TRGQ0 input

PMC14	Specification of operating mode of P14 pin
1	TOQ0T3 output/EVTQ0 input

PMC13	Specification of operating mode of P13 pin
1	TOQ0B2 output/TIQ00 input

PMC12	Specification of operating mode of P12 pin
1	TOQ0T2 output/TIQ03 input/TOQ03 output

PMC11	Specification of operating mode of P11 pin
1	TOQ0B1 output/TIQ02 input/TOQ02 output

PMC10	Specification of operating mode of P10 pin
1	TOQ0T1 output/TIQ01 input/TOQ01 output

(10) Port 1 function control register (PFC1), port 1 function control expansion register (PFCE1)

Set the PFC1 and PFCE1 registers as follows.

PFC1 register = C0H

PFCE1 register = 00H

PFCE1 Address: FFFFF702H

	7	6	5	4	3	2	1	0
After reset	0	0	0	0	0	0	0	0
Bit name	0	0	0	0	0	PFCE12	PFCE11	PFCE10
Set value	0	0	0	0	0	0	0	0

PFC1 Address: FFFFF462H

	7	6	5	4	3	2	1	0
After reset	0	0	0	0	0	0	0	0
Bit name	PFC17	PFC16	PFC15	PFC14	PFC13	PFC12	PFC11	PFC10
Set value	1	1	0	0	0	0	0	0

PFC17	Specification of alternate function of P17 pin
1	TIP21 input

PFC16	Specification of alternate function of P16 pin
1	TIP20 input

PFC15	Specification of alternate function of P15 pin
0	TOQ0B3 output

PFC14	Specification of alternate function of P14 pin
0	TOQ0T3 output

PFC13	Specification of alternate function of P13 pin
0	TOQ0B2 output

PFCE12	PFC12	Specification of alternate function of P12 pin
0	0	TOQ0T2 output

PFCE11	PFC11	Specification of alternate function of P11 pin
0	0	TOQ0B1 output

PFCE10	PFC10	Specification of alternate function of P10 pin
0	0	TOQ0T1 output

(11) Pull-up resistor option register 1 (PU1)

Set the PU1 register as follows.

PU1 register = 00H

PU1 Address: FFFFFC42H

	7	6	5	4	3	2	1	0
After reset	0	0	0	0	0	0	0	0
Bit name	PU17	PU16	PU15	PU14	PU13	PU12	PU11	PU10
Set value	0	0	0	0	0	0	0	0

PU1n	Control of on-chip pull-up resistor connection (n = 0 to 7)
0	No connection

(12) TMP0 control register 0 (TP0CTL0)

Set the TP0CTL0 register as follows.

TP0CTL0 register = 00H

TP0CTL0 Address: FFFFF640H

	7	6	5	4	3	2	1	0
After reset	0	0	0	0	0	0	0	0
Bit name	TP0CE	0	0	0	0	TP0CKS2	TP0CKS1	TP0CKS0
Set value	0	0	0	0	0	0	0	0

TP0CE	TMP0 operation control
0	TMP0 operation disabled (TMP0 reset asynchronously[Note])

TP0CKS2	TP0CKS1	TP0CKS0	Internal count clock selection
0	0	0	fxx/2

Note The TP0OPT0.TP0OVF bit and 16-bit counter are reset simultaneously. Moreover, timer outputs (TOP00, TOP01, TOP21, and TOP31 pins) are reset to the TP0IOC0 register set status at the same time as the 16-bit counter.

Caution Be sure to set bits 3 to 6 to "0".

(13) TMP0 control register 1 (TP0CTL1)

Set the TP0CTL1 register as follows.

TP0CTL1 register = 85H

TP0CTL1 Address: FFFFF641H

	7	6	5	4	3	2	1	0
After reset	0	0	0	0	0	0	0	0
Bit name	TP0SYE	TP0EST	TP0EEE	0	0	TP0MD2	TP0MD1	TP0MD0
Set value	1	0	0	0	0	1	0	1

TP0SYE	Operation mode selection
1	Tuning operation mode

TP0EST	Software trigger control
0	No software trigger operation

TP0EEE	Count clock selection
0	Disables operation with external event count input (TIP00 pin). (Performs counting with the count clock selected by the TP0CTL0.TP0CKS0 to TP0CTL0.TP0CKS2 bits.)

TP0MD2	TP0MD1	TP0MD0	Timer mode selection
1	0	1	Free-running timer mode

Caution Be sure to set bits 3 and 4 to “0”.

(14) TMP0 I/O control register 0 (TP0IOC0)

Set the TP0IOC0 register as follows.

TP0IOC0 register = 00H

TP0IOC0 Address: FFFFF642H

	7	6	5	4	3	2	1	0
After reset	0	0	0	0	0	0	0	0
Bit name	0	0	0	0	TP0OL1	TP0OE1	TP0OL0	TP0OE0
Set value	0	0	0	0	0	0	0	0

TP0OL1	TOP01 pin output level setting
0	TOP01 pin starts output at high level.

TP0OE1	TOP01 pin output setting
0	Timer output prohibited • Low level is output from the TOP01 pin.

TP0OL0	TOP00 pin output level setting
0	TOP00 pin starts output at high level.

TP0OE0	TOP00 pin output setting
0	Timer output prohibited • Low level is output from the TOP00 pin.

(15) TMP0 I/O control register 1 (TP0IOC1)

Set the TP0IOC1 register as follows.

TP0IOC1 register = 00H

TP0IOC1 Address: FFFFF643H

	7	6	5	4	3	2	1	0
After reset	0	0	0	0	0	0	0	0
Bit name	0	0	0	0	TP0IS3	TP0IS2	TP0IS1	TP0IS0
Set value	0	0	0	0	0	0	0	0

TP0IS3	TP0IS2	Capture trigger input signal (TIP01 pin) valid edge setting
0	0	No edge detection (capture operation invalid)

TP0IS1	TP0IS0	Capture trigger input signal (TIP00 pin) valid edge setting
0	0	No edge detection (capture operation invalid)

(16) TMP0 I/O control register 2 (TP0IOC2)

Set the TP0IOC2 register as follows.

TP0IOC2 register = 00H

TP0IOC2 Address: FFFFF644H

	7	6	5	4	3	2	1	0
After reset	0	0	0	0	0	0	0	0
Bit name	0	0	0	0	TP0EES1	TP0EES0	TP0ETS1	TP0ETS0
Set value	0	0	0	0	0	0	0	0

TP0EES1	TP0EES0	External event count input signal (TIP00 pin) valid edge setting
0	0	No edge detection (external event count invalid)

TP0ETS1	TP0ETS0	External trigger input signal (TIP00 pin) valid edge setting
0	0	No edge detection (external trigger invalid)

(17) TMP0 option register 0 (TP0OPT0)

Set the TP0OPT0 register as follows.

TP0OPT0 register = 00H

TP0OPT0 Address: FFFFF645H

	7	6	5	4	3	2	1	0
After reset	0	0	0	0	0	0	0	0
Bit name	0	0	TP0CCS1	TP0CCS0	0	0	0	TP0OVF
Set value	0	0	0	0	0	0	0	0

TP0CCS1	TP0CCR1 register capture/compare selection
0	Compare register selected

TP0CCS0	TP0CCR0 register capture/compare selection
0	Compare register selected

TP0OVF	TMP0 overflow detection flag
Reset (0)	0 written to TPnOVF bit or TP0CTL0.TP0CE bit = 0

Caution Be sure to set bits 1 to 3, 6, and 7 to "0".

(18) TMP0 capture/compare register 0 (TP0CCR0)

Set the TP0CCR0 register as follows.

TP0CCR0 register = 0020H

TP0CCR0 Address: FFFFF646H

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
After reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit name	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Set value	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0

Compare register value setting
TMP0 A/D converter 0 conversion start trigger value setting (compare match occurs 1 μs later)

(19) TMP0 capture/compare register 1 (TP0CCR1)

Set the TP0CCR1 register as follows.

TP0CCR1 register = 0020H

TP0CCR1 Address: FFFFF648H

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
After reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit name	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Set value	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0

Compare register value setting
TMP0 A/D converter 1 conversion start trigger value setting (compare match occurs 1 μs later)

(20) TMQ0 control register 0 (TQ0CTL0)

Set the TQ0CTL0 register as follows.

TQ0CTL0 register = 00H

TQ0CTL0 Address: FFFFF5C0H

	7	6	5	4	3	2	1	0
After reset	0	0	0	0	0	0	0	0
Bit name	TQ0CE	0	0	0	0	TQ0CKS2	TQ0CKS1	TQ0CKS0
Set value	0	0	0	0	0	0	0	0

TQ0CE	TMQ0 operation control
0	TMQ0 operation disabled (TMQ0 reset asynchronously[Note])

TQ0CKS2	TQ0CKS1	TQ0CKS0	Internal count clock selection
0	0	0	fxx/2

Note The TQ0OPT0.TQ0OVF bit and 16-bit counter are reset simultaneously. Moreover, timer outputs (TOQ00 to TOQ03 and TOQ10 pins) are reset to the TQ0IOC0 register set status at the same time as the 16-bit counter.

Caution Be sure to set bits 3 to 6 to "0".

(21) TMQ0 control register 1 (TQ0CTL1)

Set the TQ0CTL1 register as follows.

TQ0CTL1 register = 07H

TQ0CTL1 Address: FFFFF5C1H

	7	6	5	4	3	2	1	0
After reset	0	0	0	0	0	0	0	0
Bit name	0	TQ0EST	TQ0EEE	0	0	TQ0MD2	TQ0MD1	TQ0MD0
Set value	0	0	0	0	0	1	1	1

TQ0EST	Software trigger control
0	No software trigger operation

TQ0EEE	Count clock selection
0	Disable operation with external event count input (EVTQ0 pin). Perform counting with the count clock selected by the TQ0CTL0.TQ0CKS0 to TQ0CTL0.TQ0CKS2 bits.)

TQ0MD2	TQ0MD1	TQ0MD0	Timer mode selection
1	1	1	6-phase PWM output mode

Caution Be sure to set bits 3, 4, and 7 to “0”.

(22) TMQ0 I/O control register 0 (TQ0IOC0)

Set the TQ0IOC0 register as follows.

TQ0IOC0 register = 55H

TQ0IOC0 Address: FFFFF5C2H

	7	6	5	4	3	2	1	0
After reset	0	0	0	0	0	0	0	0
Bit name	TQ0OL3	TQ0OE3	TQ0OL2	TQ0OE2	TQ0OL1	TQ0OE1	TQ0OL0	TQ0OE0
Set value	0	1	0	1	0	1	0	1

TQ0OLm	Output level setting of TOQ0m and TOQ0Tb pins (m = 0 to 3, b = 1 to 3)
0	TOQ0m and TOQ0Tb pins start output at high level.

TQ0OEm	Output setting of TOQ0m and TOQ0Tb pins (m = 0 to 3, b = 1 to 3)
1	Timer output enabled (A pulse is output from the TOQ0m and TOQ0Tb pins.)

(23) TMQ0 I/O control register 1 (TQ0IOC1)

Set the TQ0IOC1 register as follows.

TQ0IOC1 register = 00H

TQ0IOC1 Address: FFFFF5C3H

	7	6	5	4	3	2	1	0
After reset	0	0	0	0	0	0	0	0
Bit name	TQ0IS7	TQ0IS6	TQ0IS5	TQ0IS4	TQ0IS3	TQ0IS2	TQ0IS1	TQ0IS0
Set value	0	0	0	0	0	0	0	0

TQ0IS7	TQ0IS6	Capture trigger input signal (TIQ03 pin) valid edge setting
0	0	No edge detection (capture operation invalid)

TQ0IS5	TQ0IS4	Capture trigger input signal (TIQ02 pin) valid edge setting
0	0	No edge detection (capture operation invalid)

TQ0IS3	TQ0IS2	Capture trigger input signal (TIQ01 pin) valid edge setting
0	0	No edge detection (capture operation invalid)

TQ0IS1	TQ0IS0	Capture trigger input signal (TIQ00 pin) valid edge setting
0	0	No edge detection (capture operation invalid)

(24) TMQ0 I/O control register 2 (TQ0IOC2)

Set the TQ0IOC2 register as follows.

TQ0IOC2 register = 00H

TQ0IOC2 Address: FFFFF5C4H

	7	6	5	4	3	2	1	0
After reset	0	0	0	0	0	0	0	0
Bit name	0	0	0	0	TQ0EES1	TQ0EES0	TQ0ETS1	TQ0ETS0
Set value	0	0	0	0	0	0	0	0

TQ0EES1	TQ0EES0	External event count input signal (EVTQ0 pin) valid edge setting
0	0	No edge detection (external event count invalid)

TQ0ETS1	TQ0ETS0	External trigger input signal (TRGQ0 pin) valid edge setting
0	0	No edge detection (external trigger invalid)

(25) TMQ0 option register 0 (TQ0OPT0)

Set the TQ0OPT0 register as follows.

TQ0OPT0 register = 00H

TQ0OPT0 Address: FFFFF5C5H

	7	6	5	4	3	2	1	0
After reset	0	0	0	0	0	0	0	0
Bit name	TQ0CCS3	TQ0CCS2	TQ0CCS1	TQ0CCS0	0	TQ0CMS	TQ0CUF	TQ0OVF
Set value	0	0	0	0	0	0	0	0

TQ0CCSm	TQ0CCRm register capture/compare selection (m = 0 to 3)
0	Compare register selected

TQ0CMS	Compare register rewrite mode selection
0	Batch rewrite mode specified (transfer operation specified)

TQ0CUF	Timer Q0 count up/down flag
0	Timer Q0 is counting up.

TQ0OVF	TMQ0 overflow flag
Reset (0)	0 written to TQ0OVF bit or TQ0CTL0.TQ0CE bit = 0

Caution Be sure to set bit 3 to “0”.

(26) TMQ0 capture/compare register 0 (TQ0CCR0)

Set the TQ0CCR0 register as follows.

TQ0CCR0 register = 031FH

TQ0CCR0 Address: FFFFF5C6H

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
After reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit name	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Set value	0	0	0	0	0	0	1	1	0	0	0	1	1	1	1	1

Compare register value setting
50 μs, 799 counts

(27) TMQ0 capture/compare register 1 (TQ0CCR1)

Set the TQ0CCR1 register as follows.

TQ0CCR1 register = 0320H

TQ0CCR1 Address: FFFFF5C8H

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
After reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit name	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Set value	0	0	0	0	0	0	1	1	0	0	1	0	0	0	0	0

Compare register value setting
800 counts

(28) TMQ0 capture/compare register 2 (TQ0CCR2)

Set the TQ0CCR2 register as follows.

TQ0CCR2 register = 0320H

TQ0CCR2 Address: FFFFF5CAH

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
After reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit name	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Set value	0	0	0	0	0	0	1	1	0	0	1	0	0	0	0	0

Compare register value setting
800 counts

(29) TMQ0 capture/compare register 3 (TQ0CCR3)

Set the TQ0CCR3 register as follows.

TQ0CCR3 register = 0320H

TQ0CCR3 Address: FFFFF5CCH

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
After reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit name	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Set value	0	0	0	0	0	0	1	1	0	0	1	0	0	0	0	0

Compare register value setting
800 counts

(30) TMQ0 option register 1 (TQ0OPT1)

Set the TQ0OPT1 register as follows.

TQ0OPT1 register = 40H

TQ0OPT1 Address: FFFFF5E0H

	7	6	5	4	3	2	1	0
After reset	0	0	0	0	0	0	0	0
Bit name	TQ0ICE	TQ0IOE	0	TQ0ID4	TQ0ID3	TQ0ID2	TQ0ID1	TQ0ID0
Set value	0	1	0	0	0	0	0	0

TQ0ICE	Crest interrupt (INTTQ0CC0 signal) enable
0	Do not use INTTQ0CC0 signal (do not use it as count signal for interrupt culling).

TQ0IOE	Valley interrupt (INTTQ0OV signal) enable
1	Use INTTQ0OV signal (use it as count signal for interrupt culling).

TQ0ID4	TQ0ID3	TQ0ID2	TQ0ID1	TQ0ID0	Number of times of interrupt
0	0	0	0	0	Not culled (all interrupts are output)

(31) TMQ0 option register 2 (TQ0OPT2)

Set the TQ0OPT2 register as follows.

TQ0OPT2 register = 84H

TQ0OPT2 Address: FFFFF5E1H

	7	6	5	4	3	2	1	0
After reset	0	0	0	0	0	0	0	0
Bit name	TQ0RDE	TQ0DTM	TQ0ATM03	TQ0ATM02	TQ0AT03	TQ0AT02	TQ0AT01	TQ0AT00
Set value	1	0	0	0	0	1	0	0

TQ0RDE	Transfer culling enable
1	Culls transfer at the same interval as interrupt culling set by the TQnOPT1 register.

TQ0DTM	Dead-time counter operation mode selection (m = 1 to 3)
0	Dead-time counter counts up normally and, if TOQ0m output of TMQ0 is at a narrow interval (TOQ0m output width < dead-time width), the dead-time counter is cleared and counts up again.

TQ0ATM03	TQ0ATM03 mode selection
0	Outputs A/D trigger signal (TQTADT00) for INTTP0CC1 interrupt while dead-time counter is counting up.

TQ0ATM02	TQ0ATM02 mode selection
0	Outputs A/D trigger signal (TQTADT00) for INTTP0CC0 interrupt while dead-time counter is counting up.

TQ0AT03	A/D trigger output control 3
0	Disables output of A/D trigger signal (TQTADT00) for INTTP0CC1 interrupt.

TQ0AT02	A/D trigger output control 2
1	Enables output of A/D trigger signal (TQTADT00) for INTTP0CC0 interrupt.

TQ0AT01	A/D trigger output control 1
0	Disables output of A/D trigger signal (TQTADT00) for INTTQ0CC0 (crest interrupt).

TQ0AT00	A/D trigger output control 0
0	Disables output of A/D trigger signal (TQTADT00) for INTTQ0OV (valley interrupt).

(32) TMQ0 option register 3 (TQ0OPT3)

Set the TQ0OPT3 register as follows.

TQ0OPT3 register = 00H

TQ0OPT3 Address: FFFFF5E3H

	7	6	5	4	3	2	1	0
After reset	0	0	0	0	0	0	0	0
Bit name	0	0	TQ0ATM13	TQ0ATM12	TQ0AT13	TQ0AT12	TQ0AT11	TQ0AT10
Set value	0	0	0	0	0	0	0	0

TQ0ATM13	TQ0ATM13 mode selection
0	Outputs A/D trigger signal (TQTADT01) of INTTP0CC1 interrupt while dead-time counter is counting up.

TQ0ATM12	TQ0ATM12 mode selection
0	Outputs A/D trigger signal (TQTADT01) of INTTP0CC0 interrupt while dead-time counter is counting up.

TQ0AT13	A/D trigger output control 3
0	Disables output of A/D trigger signal (TQTADT01) for INTTP0CC1 interrupt.

TQ0AT12	A/D trigger output control 2
0	Disables output of A/D trigger signal (TQTADT01) for INTTP0CC0 interrupt.

TQ0AT11	A/D trigger output control 1
0	Disables output of A/D trigger signal (TQTADT01) for INTTQ0CC0 interrupt (crest interrupt).

TQ0AT10	A/D trigger output control 0
0	Disables output of A/D trigger signal (TQTADT01) for INTTQ0OV interrupt (valley interrupt).

(33) TMQ0 I/O control register 3 (TQ0IOC3)

Set the TQ0IOC3 register as follows.

TQ0IOC3 register = FCH

TQ0IOC3 Address: FFFFF5E2H

	7	6	5	4	3	2	1	0
After reset	1	0	1	0	1	0	0	0
Bit name	TQ0OLB3	TQ0OEB3	TQ0OLB2	TQ0OEB2	TQ0OLB1	TQ0OEB1	0	0
Set value	1	1	1	1	1	1	0	0

TQ0OLBm	Setting of TOQ0Bm pin output level (m = 1 to 3)
1	Enables inversion of output of TOQ0Bm pin

TQ0OEBm	Setting of TOQ0Bm pin output
1	Enables TOQ0Bm pin output.

(34) TMQ0 dead-time compare register (TQ0DTC)

Set the TQ0DTC register as follows.

TQ0DTC register = 0080H

TQ0DTC Address: FFFFF5E4H

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
After reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit name	0	0	0	0	0	0	TQ0 DTC9	TQ0 DTC8	TQ0 DTC7	TQ0 DTC6	TQ0 DTC5	TQ0 DTC4	TQ0 DTC3	TQ0 DTC2	TQ0 DTC1	TQ0 DTC0
Set value	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Dead-time value specification
4 μs

(35) High-impedance output control register 00 (HZA0CTL0)

Set the HZA0CTL0 register as follows.

HZA0CTL0 register = 80H/88H

HZA0CTL0 Address: FFFFF5F0H

	7	6	5	4	3	2	1	0
After reset	0	0	0	0	0	0	0	0
Bit name	HZA0DCE0	HZA0DCM0	HZA0DCN0	HZA0DCP0	HZA0DCT0	HZA0DCC0	0	HZA0DCF0
Set value	1	0	0	0	0/1	0	0	0

HZA0DCE0	High-impedance output control
1	Enables high-impedance output control operation.

HZA0DCM0	Condition of clearing high-impedance state by HZA0DCC0 bit
0	Setting of the HZA0DCC0 bit is valid regardless of the TOQ0OFF pin input.

HZA0DCN0	HZA0DCP0	TOQ0OFF pin input edge specification
0	0	No valid edge (setting the HZA0DCF0 bit by TOQ0OFF pin input is prohibited).

HZA0DCT0	High-impedance output trigger bit
0	No operation
1	Pins are made to go into a high-impedance state by software and the HZA0DCF0 bit is set to 1.

HZA0DCC0	High-impedance output control clear bit
0	No operation

HZA0DCF0	High-impedance output status flag
0	Indicates that output of the target pin is enabled. • This bit is cleared to 0 when the HZA0DCE0 bit = 0. • This bit is cleared to 0 when the HZA0DCC0 bit = 1.

(36) A/D converter n mode register 0 (ADAnM0)

Set the ADAnM0 register as follows.

ADAnM0 register = 22H/A2H

ADAnM0 (n = 0, 1)

Address: ADA0M0 FFFFF200H, ADA1M0 FFFFF220H

	7	6	5	4	3	2	1	0
After reset	0	0	0	0	0	0	0	0
Bit name	ADAnCE	0	ADAnMD1	ADAnMD0	ADAnETS1	ADAnETS0	ADAnTMD	ADAnEF
Set value	0/1	0	1	0	0	0	1	0

ADAnCE	A/D conversion operation control
0	Stop conversion operation
1	Start conversion operation

ADAnMD1	ADAnMD0	Operation mode specification
1	0	One-shot select mode

ADAnETS1	ADAnETS0	Specification of external trigger (ADTRGn) valid edge
0	0	No edge detection (external trigger invalid)

ADAnTMD	Trigger mode specification
1	Hardware trigger mode

ADAnEF	Status of A/D converter n
0	A/D conversion stopped

(37) A/D converter n mode register 1 (ADAnM1)

Set the ADAnM1 register as follows.

ADAnM1 register = 01H

ADAnM1 (n = 0, 1) Address: ADA0M1 FFFFF201H, ADA1M1 FFFFF221H

	7	6	5	4	3	2	1	0
After reset	0	0	0	0	0	0	0	0
Bit name	0	0	0	0	0	0	ADAnFR1	ADAnFR0
Set value	0	0	0	0	0	0	0	1

ADAnFR1	ADAnFR0	Specification of number of conversion clocks
0	1	1.94 μs

Caution Be sure to set bits 2 to 7 to "0".

(38) A/D converter n channel specification register (ADAnS)

Set the ADAnS register as follows.

ADAnS register = 00H

ADAnS (n = 0, 1) Address: ADA0S FFFFF202H, ADA1S FFFFF222H

	7	6	5	4	3	2	1	0
After reset	0	0	0	0	0	0	0	0
Bit name	0	0	0	0	0	ADAnS2	ADAnS1	ADAnS0
Set value	0	0	0	0	0	0	0	0

ADAnS2	ADAnS1	ADAnS0	Select mode
0	0	0	ANIn0

Caution Be sure to set bits 3 to 7 to "0".

(39) A/D converter n mode register 2 (ADAnM2)

Set the ADAnM2 register as follows.

ADAnM2 register = 01H

ADAnM2 (n = 0, 1) — Address: ADA0M2 FFFFF203H, ADA1M2 FFFFF223H

	7	6	5	4	3	2	1	0
After reset	0	0	0	0	0	0	0	0
Bit name	ADAnBS	0	0	0	0	0	ADAnTMD1	ADAnTMD0
Set value	0	0	0	0	0	0	0	1

ADAnBS	Buffer mode specification
0	1-buffer mode

ADAnTMD1	ADAnTMD0	Hardware trigger mode specification
0	1	Timer trigger mode 0

(40) Operational amplifier n control register 0 (OPnCTL0)

Set the OPnCTL0 register as follows.

OPnCTL0 register = 00H

OPnCTL0 (n = 0, 1) — Address: OP0CTL0 FFFFF260H, OP1CTL0 FFFFF268H

	7	6	5	4	3	2	1	0
After reset	0	0	0	0	0	0	0	0
Bit name	0	OPnOEN2	OPnOEN1	OPnOEN0	0	0	0	OPnGA0
Set value	0	0	0	0	0	0	0	0

OPnOEN2	Operation control of operational amplifier 2
0	Disables operation

OPnOEN1	Operation control of operational amplifier 1
0	Disables operation

OPnOEN0	Operation control of operational amplifier 0
0	Disables operation

OPnGA0	Gain specification of operational amplifier
0	×2.5

Caution Be sure to set bits 1 to 3 and 7 to “0”.

(41) Operational amplifier n control register 1 (OPnCTL1)

Set the OPnCTL1 register as follows.

OPnCTL1 register = 00H

OPnCTL1 (n = 0, 1) — Address: OP0CTL1 FFFFF261H, OP1CTL1 FFFFF269H

	7	6	5	4	3	2	1	0
After reset	0	0	0	0	0	0	0	0
Bit name	0	OPnCEN2	OPnCEN1	OPnCEN0	0	0	0	OPnCMP
Set value	0	0	0	0	0	0	0	0

OPnCEN2	Operation control of comparator 2
0	Disables operation

OPnCEN1	Operation control of comparator 1
0	Disables operation

OPnCEN0	Operation control of comparator 0
0	Disables operation

OPnCMP	Comparator output status
0	Comparator output = 0 (no overvoltage detection)

(42) Interrupt control register (ADnIC)

Set the ADnIC register as follows.

ADnIC register = 04H

ADnIC — Address: AD0IC FFFFF180H, AD1IC FFFFF182H

	7	6	5	4	3	2	1	0
After reset	0	1	0	0	0	1	1	1
Bit name	ADnIF	ADnMK	0	0	0	ADnPR2	ADnPR1	ADnPR0
Set value	0	0	0	0	0	1	0	0

ADnIF	Interrupt request flag[Note]
0	Interrupt request not issued

ADnMK	Interrupt mask flag
0	Interrupt servicing enabled

ADnPR2	ADnPR1	ADnPR0	Interrupt priority specification bit
1	0	0	Specifies level 4.

Note The interrupt request flag is reset automatically by the hardware if an interrupt request signal is acknowledged.

(43) Interrupt control register (TQ0OVIC)

Set the TQ0OVIC register as follows.

TQ0OVIC register = 01H

TQ0OVIC — Address: FFFFF124H

	7	6	5	4	3	2	1	0
After reset	0	1	0	0	0	1	1	1
Bit name	TQ0OVIF	TQ0OVMK	0	0	0	TQ0OVPR2	TQ0OVPR1	TQ0OVPR0
Set value	0	0	0	0	0	0	0	1

TQ0OVIF	Interrupt request flag[Note]
0	Interrupt request signal not issued

TQ0OVMK	Interrupt mask flag
0	Interrupt servicing enabled

TQ0OVPR2	TQ0OVPR1	TQ0OVPR0	Interrupt priority specification bit
0	0	1	Specifies level 1.

Note The interrupt request flag is reset automatically by the hardware if an interrupt request signal is acknowledged.

(44) Interrupt mask register 0 (IMR0)

Set the IMR0 register as follows.

IMR0 register = FBFFH

IMR0 (IMR0H/IMR0L)

Address: IMR0 FFFFF100H
IMR0L FFFFF100H, IMR0H FFFFF101H

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
After reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit name	TQ1 OVMK	TQ0 CCMK3	TQ0 CCMK2	TQ0 CCMK1	TQ0 CCMK0	TQ0 OVMK	CMP MK1	CMP MK0	PMK7	PMK6	PMK5	PMK4	PMK3	PMK2	PMK1	PMK0
Set value	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1

TQ1OVMK	Interrupt mask flag setting
1	INTTQ1OV interrupt servicing disabled

TQ0CCMK3	Interrupt mask flag setting
1	INTTQ0CC3 interrupt servicing disabled

TQ0CCMK2	Interrupt mask flag setting
1	INTTQ0CC2 interrupt servicing disabled

TQ0CCMK1	Interrupt mask flag setting
1	INTTQ0CC1 interrupt servicing disabled

TQ0CCMK0	Interrupt mask flag setting
1	INTTQ0CC0 interrupt servicing disabled

TQ0OVMK	Interrupt mask flag setting
0	INTTQ0OV interrupt servicing enabled

CMPMK1	Interrupt mask flag setting
1	INTCMP1 interrupt servicing disabled

CMPMK0	Interrupt mask flag setting
1	INTCMP0 interrupt servicing disabled

PMK7	Interrupt mask flag setting
1	INTP7 interrupt servicing disabled

PMK6	Interrupt mask flag setting
1	INTP6 interrupt servicing disabled

PMK5	Interrupt mask flag setting
1	INTP5 interrupt servicing disabled

2/2

PMK4	Interrupt mask flag setting
1	INTP4 interrupt servicing disabled

PMK3	Interrupt mask flag setting
1	INTP3 interrupt servicing disabled

PMK2	Interrupt mask flag setting
1	INTP2 interrupt servicing disabled

PMK1	Interrupt mask flag setting
1	INTP1 interrupt servicing disabled

PMK0	Interrupt mask flag setting
1	INTP0 interrupt servicing disabled

(45) Interrupt mask register 3 (IMR3)

Set the IMR3 register as follows.

IMR3 register = FCFFH

IMR3 (IMR3H/IMR3L)

Address: IMR3 FFFFF106H
IMR3L FFFFF106H, IMR3H FFFFF107H

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
After reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit name	1	1	1	1	TM0EQMK0	AD2MK	AD1MK	AD0MK	CB1TMK	CB1RMK	CB1REMK	UA1TMK	UA1RMK	UA1REMK	CB0TMK	CB0RMK
Set value	1	1	1	1	1	1	0	0	1	1	1	1	1	1	1	1

TM0EQMK0	Interrupt mask flag setting
1	INTTM0EQ0 interrupt servicing disabled

AD2MK	Interrupt mask flag setting
1	INTAD2 interrupt servicing disabled

AD1MK	Interrupt mask flag setting
0	INTAD1 interrupt servicing enabled

AD0MK	Interrupt mask flag setting
0	INTAD0 interrupt servicing enabled

CB1TMK	Interrupt mask flag setting
1	INTCB1T interrupt servicing disabled

CB1RMK	Interrupt mask flag setting
1	INTCB1R interrupt servicing disabled

CB1REMK	Interrupt mask flag setting
1	INTCB1RE interrupt servicing disabled

UA1TMK	Interrupt mask flag setting
1	INTUA1T interrupt servicing disabled

UA1RMK	Interrupt mask flag setting
1	INTUA1R interrupt servicing disabled

UA1REMK	Interrupt mask flag setting
1	INTUA1RE interrupt servicing disabled

CB0TMK	Interrupt mask flag setting
1	INTCB0T interrupt servicing disabled

CB0RMK	Interrupt mask flag setting
1	INTCB0R interrupt servicing disabled

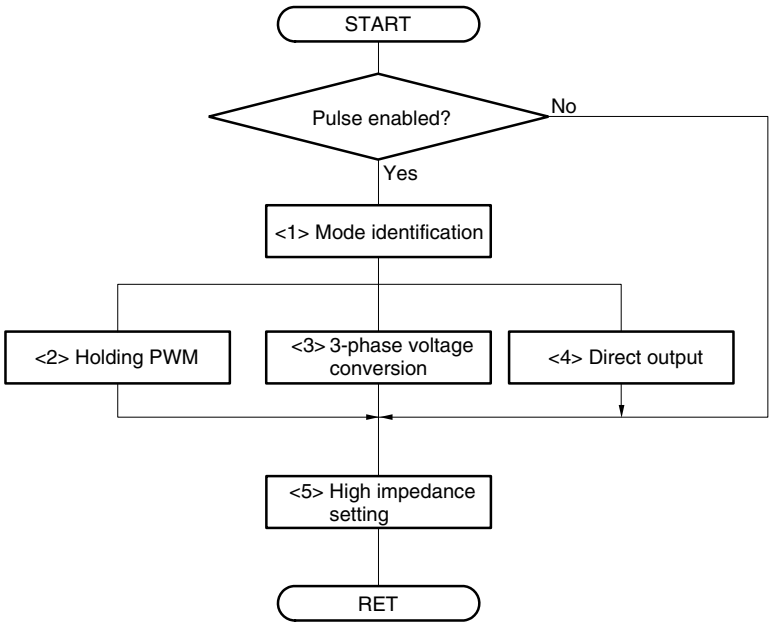
CHAPTER 3 PROGRAM CONFIGURATION

This chapter explains the program configuration of the 3-phase PWM driver. The user should set the PWM pulse.

3.1 Configuration of 3-Phase PWM Driver

The configuration of the 3-phase PWM driver is illustrated below.

Figure 3-1. Phase PWM Driver Configuration (1/2)



◆ <7> A/D converters 0 and 1 conversion completion processing — Refer to **Figure 5-8 A/D Converters 0 and 1 Conversion Completion Processing**.

◆ <8> TMQ0 valley interrupt (INTTQ0OV) processing (for debugging)[Note] — Refer to **5-7 TMQ0 Valley Interrupt (INTTQ0OV) Processing**.

<6> sin calculation processing — Refer to **Figure 5-9 sin2 Calculation Processing** and **Figure 5-10 sins Calculation Processing**.

Note This processing is used only for debugging and is not usually used.

Remark ◆: A program must be developed by the user.

Figure 3-1. 3-Phase PWM Driver Configuration (2/2)

<1> Mode identification: Identifies the operation mode of the 3-phase PWM driver.
<2> Holding PWM: Sets in the output lock mode the PWM duty ratio previously set by the 3-phase PWM driver.
<3> 3-phase voltage conversion: Performs 3-phase voltage conversion in the dq conversion mode.
<4> Direct output: Individually sets values of phases U, V, and W.
<5> High impedance setting: Switches the port state of the U, $\overline{U}$, V, $\overline{V}$, W, and $\overline{W}$ phase pins between the high-impedance state and PWM output state.
<6> sin calculation processing: sin calculation by Taylor's expansion. Called by <3>.
<7> A/D converters 0 and 1 conversion completion processing: Interrupt servicing that occurs after completion of conversion by A/D converters 0 and 1
<8> TMQ0 valley interrupt (INTTQ0OV) processing: TMQ0 valley interrupt (INTTQ0OV) processing. Used for debugging.

3.2 Global Variables

The global variables used for the 3-phase PWM driver are listed below.

Table 3-1. Global Variables

Symbol	No.	Type	Usage	Set Value
bk_hi_z	(1)	unsigned char	Flag holding high-impedance state	0: PWM output pin is in a high-impedance state. 1: PWM output pin is ready for PWM output.
bk_phase_u	(2)	signed int	Holds duty ratio of phase U.	0 to 800
bk_phase_v	(3)	signed int	Holds duty ratio of phase V.	0 to 800
bk_phase_w	(4)	signed int	Holds duty ratio of phase W.	0 to 800
test_pwm_mode	(5)	unsigned char	For debugging (usually commented out)	0: Direct mode 1: dq conversion mode 2: Output lock mode
test_pwm_flag	(6)	unsigned char	For debugging (usually commented out)	0: PWM output disabled 1: PWM output enabled
test_value0	(7)	signed int	For debugging (usually commented out)	In direct mode: 0 to 800 In dq conversion mode: –400 to 400
test_value1	(8)	signed int	For debugging (usually commented out)	In direct mode: 0 to 800 In dq conversion mode: –400 to 400
test_value2	(9)	signed int	For debugging (usually commented out)	In direct mode: 0 to 800 In dq conversion mode: –400 to 400

[Explanation of global variables]

(1) bk_hi_z
This variable holds the status of the PWM output pin when the 3-phase PWM driver was previously driven.

(2) bk_phase_u
This variable holds the set value of the TQ0CCR1 register (U-phase duty ratio) when the 3-phase PWM driver was previously driven in the output lock mode.

(3) bk_phase_v
This variable holds the set value of the TQ0CCR2 register (V-phase duty ratio) when the 3-phase PWM driver was previously driven in the output lock mode.

(4) bk_phase_w
This variable holds the set value of the TQ0CCR3 register (W-phase duty ratio) when the 3-phase PWM driver was previously driven in the output lock mode.

(5) test_pwm_mode
This variable is a RAM area that is used for debugging the 3-phase PWM driver. It specifies pwm_mode to the pwm function in the tmp_zero() function. It is usually commented out.

(6) test_pwm_flag
This variable is a RAM area that is used for debugging the 3-phase PWM driver. It specifies pwm_flag to the pwm function in the tmp_zero() function. It is usually commented out.

(7) test_value0
This variable is a RAM area that is used for debugging the 3-phase PWM driver. It specifies pwm_value0 to the pwm function in the tmp_zero() function. It is usually commented out.

(8) test_value1
This variable is a RAM area that is used for debugging the 3-phase PWM driver. It specifies pwm_value1 to the pwm function in the tmp_zero() function. It is usually commented out.

(9) test_value2
This variable is a RAM area that is used for debugging the 3-phase PWM driver. It specifies pwm_value2 to the pwm function in the tmp_zero() function. It is usually commented out.

3.3 Definitions of Constants

The constants used for the 3-phase PWM driver are listed in the following table.

Table 3-2. Constants

Symbol	No.	Usage	Constant
MAXPULSE	(1)	Resolution of motor rotation angle	10,000
SGETA	(2)	sin jack-up constant	14
CARRIERPULSE	(3)	Carrier frequency (set value of TQ0CCR0 register)	799

[Explanation of constants]

(1) MAXPULSE

This constant indicates the resolution of the motor rotation angle, and is used with the sin2 function.
It expresses 0° to 360° at a resolution of 10,000.

(2) SGETA

This is a jack-up constant for the sins function.

(3) CARRIERPULSE

This is a set value of carrier frequency.
The TMQ0 count clock period can be calculated by the expression below.

$$\text{TMQ0 count clock period} = \frac{2}{f_{XX}}$$

Remark fxx: Peripheral clock

The carrier period can be calculated by this expression.

Carrier period = (Set value of TQ0CCR0 register + 1) × 2 × TMQ0 count clock period

Example: Set value of carrier frequency where the carrier frequency is 20 kHz (carrier period: 50 μs) and the peripheral clock (fxx) is 64 MHz

$$\begin{aligned}\text{Set value of TQ0CCR0 register} &= \{(\text{Carrier period} \times f_{XX}) / (2 \times 2)\} - 1\\ &= (50 \times 64) / 4 - 1\\ &= 3200 / 4 - 1\\ &= 800 - 1\\ &= 799\end{aligned}$$

Therefore, TQ0CCR0 = CARRIERPULSE = 799.

3.4 Setting Dead Time

The dead time is set by using the TQ0DTC register and is calculated by the following expression.

Dead time = Set value of TQ0DTC register × TMQ0 count clock period

Example: Set value of the TQ0DTC register when the dead time is 4 μs and the peripheral clock (fxx) is 64 MHz

TQ0DTC = Dead time × fxx / 2
= 4 × 64 / 2
= 256 / 2
= 128

Therefore, TQ0DTC = 128.

3.5 Determining PWM Pulse

The relationship between the duty ratios of phase U, V, and W, and the values of the TQ0CCR1 to TQ0CCR3 registers is shown below.

(1) Calculating output width of upper-arm phase

The output widths of phases U, V, and W are calculated by the following expressions (including dead time).

U-phase output width = {(TQ0CCR0 + 1 – TQ0CCR1) × 2 – TQ0DTC} × TMQ0 count clock period

V-phase output width = {(TQ0CCR0 + 1 – TQ0CCR2) × 2 – TQ0DTC} × TMQ0 count clock period

W-phase output width = {(TQ0CCR0 + 1 – TQ0CCR3) × 2 – TQ0DTC} × TMQ0 count clock period

(2) Calculating output width of lower-arm phase

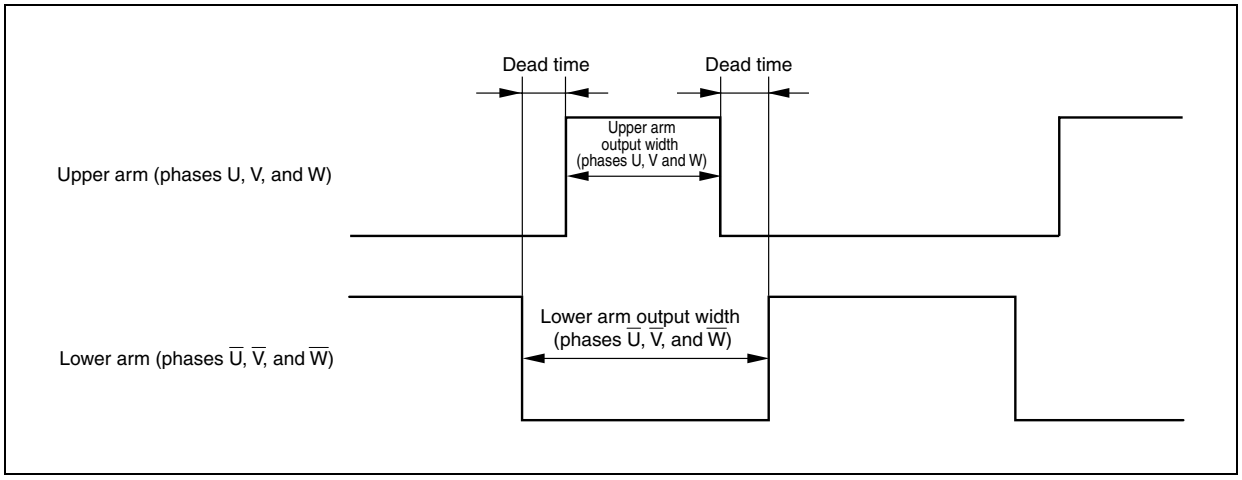
The output widths of phases $\overline{U}$, $\overline{V}$, and $\overline{W}$ are calculated by the following expressions (including dead time).

$\overline{U}$-phase output width = {(TQ0CCR0 + 1 − TQ0CCR1) × 2 + TQ0DTC} × TMQ0 count clock period

$\overline{V}$-phase output width = {(TQ0CCR0 + 1 − TQ0CCR2) × 2 + TQ0DTC} × TMQ0 count clock period

$\overline{W}$-phase output width = {(TQ0CCR0 + 1 − TQ0CCR3) × 2 + TQ0DTC} × TMQ0 count clock period

Figure 3-2. Pulse Calculation in 6-Phase PWM Output Mode



3.6 A/D Conversion

3.6.1 Conversion start trigger timing of A/D converters 0 and 1 for synchronization operation

The 3-phase PWM driver implements a synchronization operation by using TMQ0, TMQOP0, and TMP0. Therefore, any timing can be set for the conversion start trigger of A/D converters 0 and 1. Because the timing of comparison match of TMP0 during a synchronization operation is synchronized with the operating clock of TMQ0, it is calculated by using the TMQ0 count clock period.

The timing of the conversion start trigger of A/D converters 0 and 1 can be calculated by the following expression.

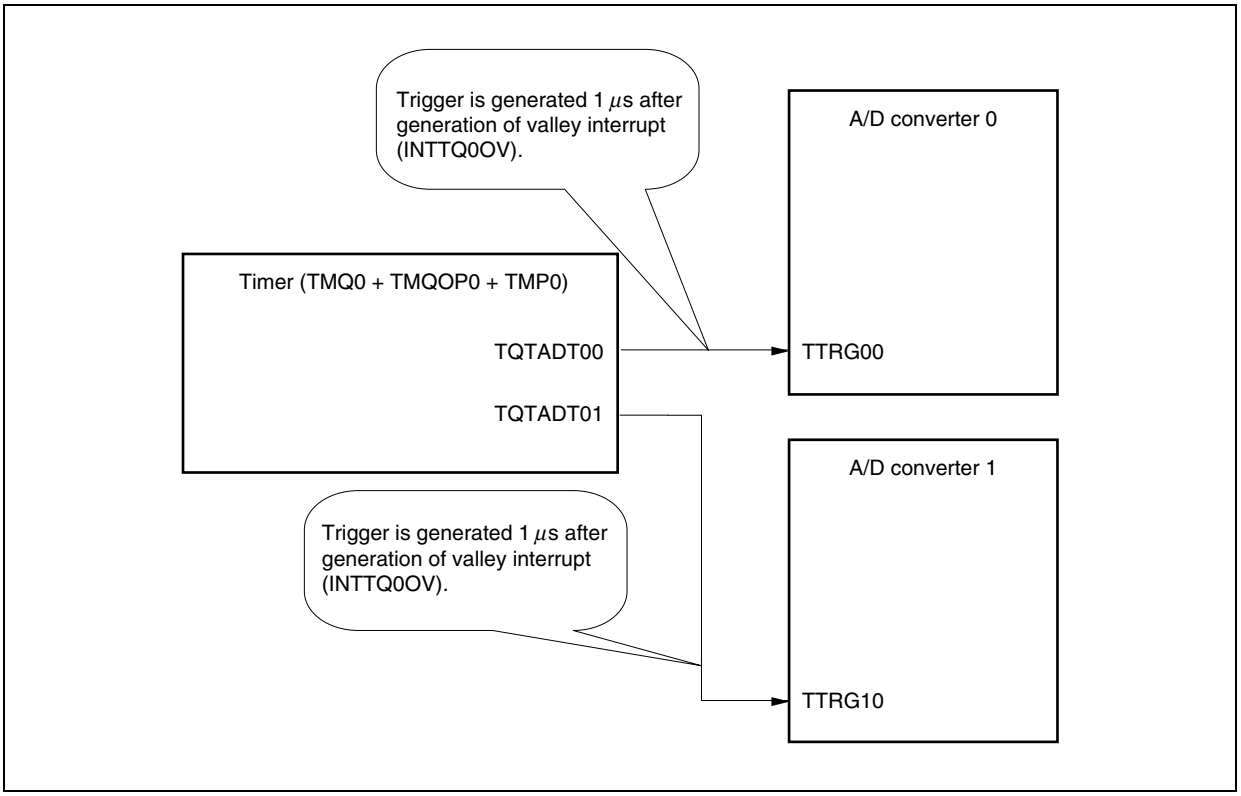
Conversion start trigger timing of A/D converter n = TP0CCRn × TMQ0 count clock period

Remark n = 0 or 1

Example: TMP0 comparison match timing where the timing of the conversion start trigger of A/D converter n is 1 μs after the TMQ0 valley interrupt (INTTQ0OV) of carrier period and the peripheral clock (fxx) is 64 MHz

Set value of TP0CCRn register = (Conversion start trigger timing of A/D converter n × fxx) / 2
= (1 × 64) / 2
= 32

Figure 3-3. Conversion Start Trigger Source of A/D Converters 0 and 1 of 3-Phase PWM Driver



With the 3-phase PWM driver, the timing of conversion start trigger of A/D converters 0 and 1 is the same. To change the conversion start time, set the TP0CCR0 and TP0CCR1 registers in accordance with the above expression.

3.6.2 A/D conversion completion time

With the 3-phase PWM driver, the ADA0M1 register is set as follows.

```
ADA0M1 = 0x01; /*A/D0 conversion clock 124 (1.94 us)*/
```

The A/D conversion clock time is 124 clocks and the A/D conversion completion time is 1.94 μs.

3.7 Arguments

The arguments used in the 3-phase PWM driver are listed in the table below.

Table 3-3. Arguments

Symbol	No.	Type	Usage	Set Value
pwm_mode	(1)	unsigned char	Sets 3-phase PWM mode.	0: Direct mode 1: dq conversion mode 2: Output lock mode[Note]
pwm_flag	(2)	unsigned char	PWM output flag	0: PWM output disabled (high-impedance state) 1: PWM output enabled (PWM output)
value0	(3)	signed int	Set value 0	In direct mode: 0 to 800 In dq conversion mode: –400 to 400
value1	(4)	signed int	Set value 1	In direct mode: 0 to 800 In dq conversion mode: –400 to 400
value2	(5)	signed int	Set value 2	In direct mode: 0 to 800 In dq conversion mode: 0 to MAXPULSE

Note If the output is locked in the output lock mode at a high pulse duty ratio, the IGBT driver may generate heat and be damaged. Therefore, set the output lock mode after thoroughly evaluating the pulse duty ratio in the overall system.

[Explanation of arguments]

(1) pwm_mode

This argument sets a mode of the 3-phase PWM driver.

(2) pwm_flag

This argument sets the output status of the PWM output pin.

(3) value0

This argument is a set value in each mode.

In direct mode: U-phase output width. Set this value in a range of 0 to 800 (CARRIERPULSE + 1).

In dq conversion mode: Executes 3-phase voltage conversion used for vector calculation. This value is equivalent to d-axis current in the dq conversion mode.
This value is set in a range of (–400 to 400)[Note].

In output lock mode: None
This argument is not used in the output lock mode.

Remark Refer to the next page for **Note**.

(4) value1

This argument is a set value in each mode.

In direct mode: V-phase output width. Set this value in a range of 0 to 800 (CARRIERPULSE + 1).

In dq conversion mode: Executes 3-phase voltage conversion used for vector calculation. This value is equivalent to q-axis current in the dq conversion mode.
This value is set in a range of (–400 to 400)[Note].

In output lock mode: None
This argument is not used in the output lock mode.

(5) value2

This argument is a set value in each mode.

In direct mode: W-phase output width. Set this value in a range of 0 to 800 (CARRIERPULSE + 1).

In dq conversion mode: Executes 3-phase voltage conversion used for vector calculation. This value is equivalent to the rotation coordinate (θ).
This value is set in a range of (0 to MAXPULSE – 1)[Note].

In output lock mode: None
This argument is not used in the output lock mode.

Note The PWM pulse duty ratio may exceed 100% in the dq conversion mode, depending on the d and q axes and the rotation coordinate (θ). Therefore, thoroughly evaluate the values of value0, value1, and value2.

CHAPTER 4 FILE CONFIGURATION

This chapter explains the file configuration of the 3-phase PWM driver.

4.1 File Configuration

The 3-phase PWM driver consists of the following 10 files.

(1) Source files

<1> main.c: MAIN processing
<2> pt_unit.c: 3-phase PWM driver file
<3> init.c: Initialization processing
<4> common.c: Definitions of constants and global variable declaration
<5> sin2.c: sin calculation processing

(2) Include file

common.h: This is a header file that allows other files to access the global variables defined by common.c by using the EXTERN instruction.
Read this header file to use definitions of constants and global variables with the other file by dividing the file.
If definitions of constants or a global variable is used, the user should define both the common.c and common.h files.

(3) Project-related files

<1> libm.a: Mathematic library[Note]
<2> libc.a: Standard library[Note]
<3> ia4crt.s: Startup module of 3-phase PWM driver
<4> ia4pwm.dir: Link directive file of 3-phase PWM driver

Note libm.a and libc.a are libraries that are automatically allocated by the project manager when a project is generated.

4.2 Explanation of Source Files

Source File Name	Function Name	Explanation
main.c	main()	MAIN processing. Nothing is written in the main routine of the 3-phase PWM driver.
	ad0_function()	Conversion completion processing of A/D converter 0
	ad1_function()	Conversion completion processing of A/D converter 1
	tmq_zero()	Interrupt servicing of carrier period
pt_unit.c	pwm()	Driver that performs 3-phase PWM control
	hi_z()	Driver that controls the output pin for 3-phase PWM
Init.c	hinit()	Initializes the on-chip peripheral I/O of the V850E/IA4 (μPD70F3186GC-8EU-A).
	ainit()	Initializes the global variables used for the 3-phase PWM driver.
common.c	–	Defines constants and declares a global variable area.
sin2.c	sin2()	Executes sin calculation.
	sins()	Executes sin calculation.

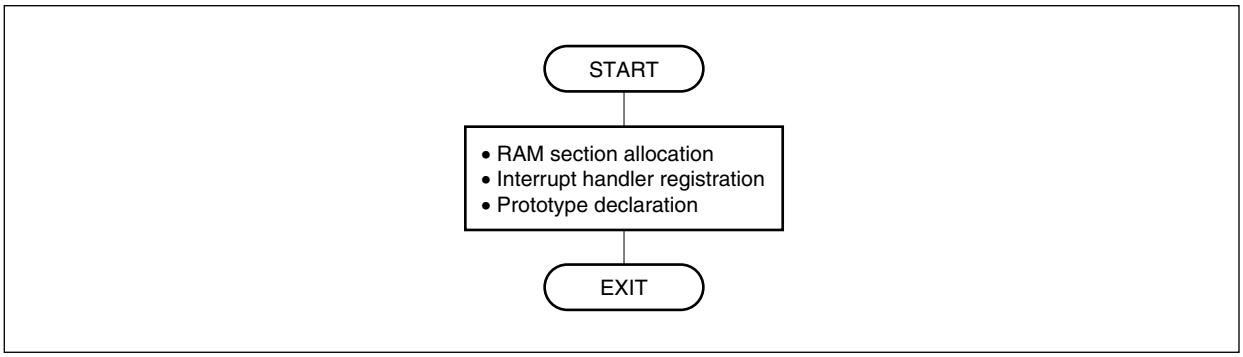
CHAPTER 5 FLOWCHART

This chapter explains each processing of the 3-phase PWM driver by using flowcharts.

5.1 Initialization Processing

The flowchart of the initialization processing is shown below.

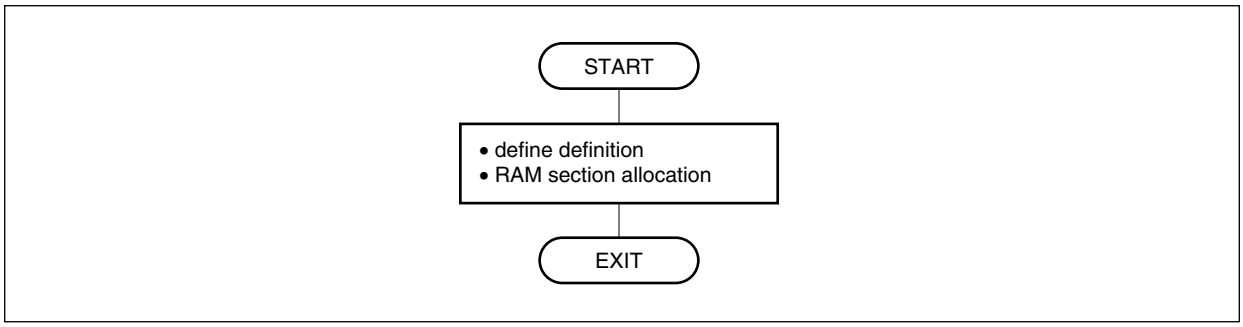
Figure 5-1. Initialization Processing



5.2 Global Variable Processing (common.c)

The flowchart of the global variable processing (common.c) is shown below.

Figure 5-2. Global Variable Processing (common.c)

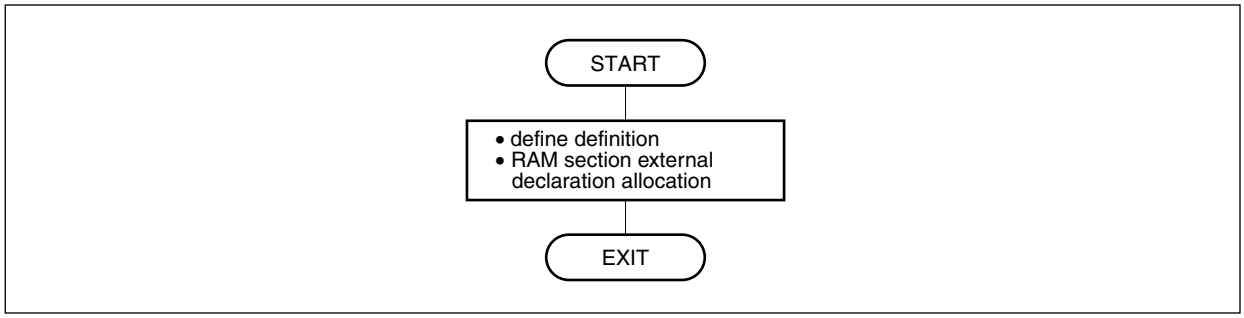


5.3 Global Variable Processing (common.h)

common.h is externally defined by the EXTERN instruction. common.h is called by main.c, pt_unit.c, init.c, and sin2.c.

The flowchart of global variable processing (common.h) is shown below.

Figure 5-3. Global Variable Processing (common.h)

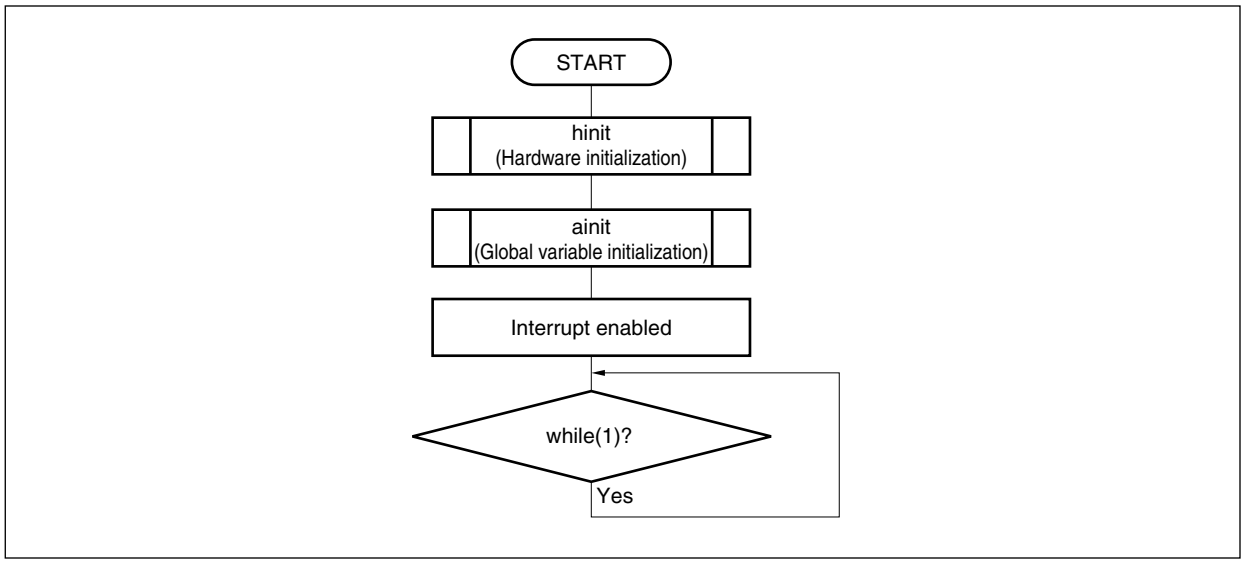


5.4 MAIN Processing

The MAIN processing initializes the hardware and global variables of the 3-phase PWM driver.

The following flowchart illustrates the MAIN processing.

Figure 5-4. MAIN Processing

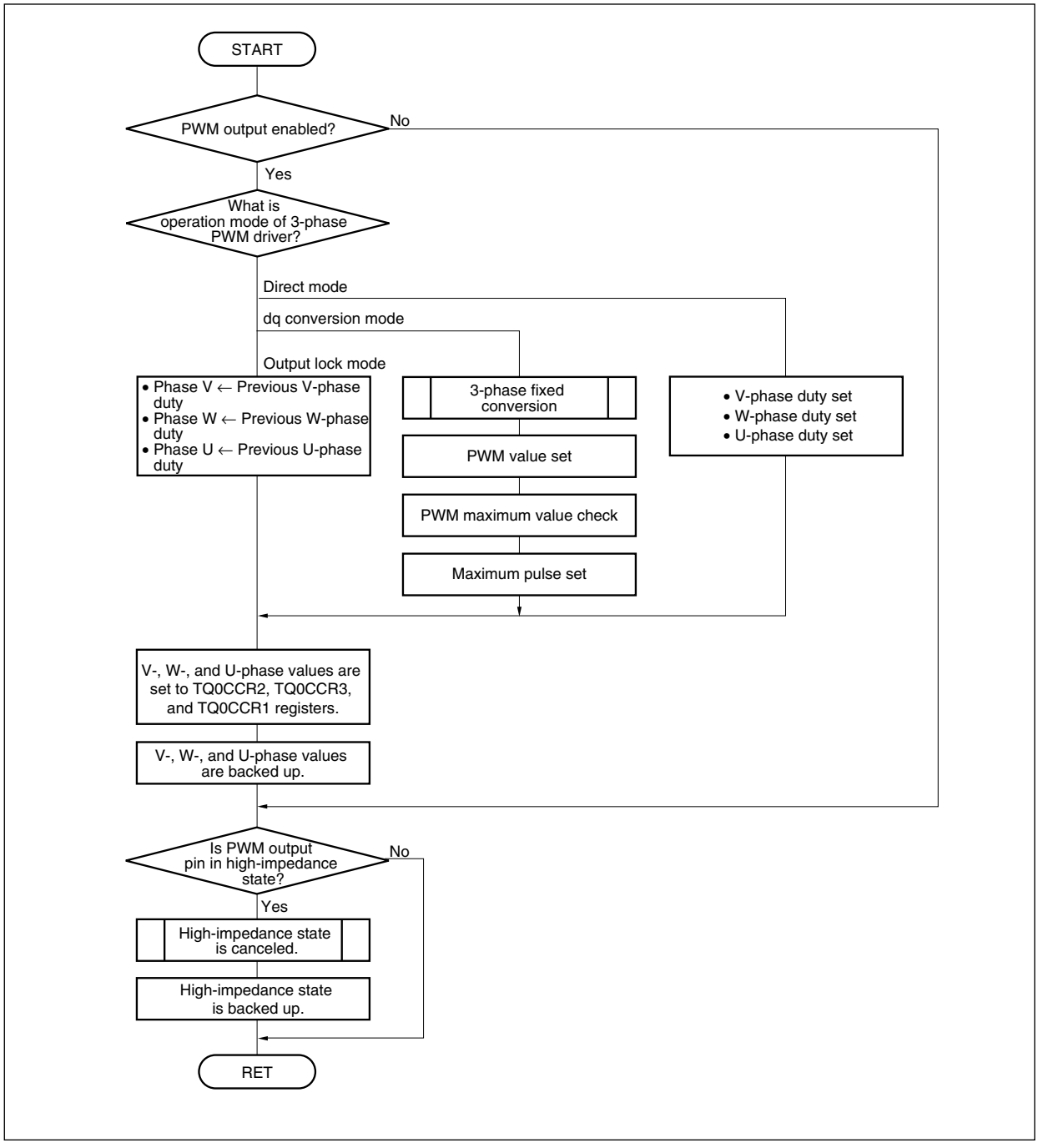


5.5 PWM Processing

Three modes of PWM processing are available: direct mode, dq conversion mode, and output lock mode. The 3-phase PWM driver writes the TQ0CCR0 to TQ0CCR3, TQ0OPT1, TP0CCR0, and TP0CCR1 registers all at once when the TMQ0 valley interrupt (INTTQ0OV) is generated after the TQ0CCR1 register is written. Therefore, be sure to call the PWM processing with the tmq_zero processing when setting the registers in the PWM processing (after the TQ0CCR1 register is written, the next writing of a register is prohibited until the TMQ0 valley interrupt (INTTQ0OV) is generated).

The flowchart of the PWM processing is shown below.

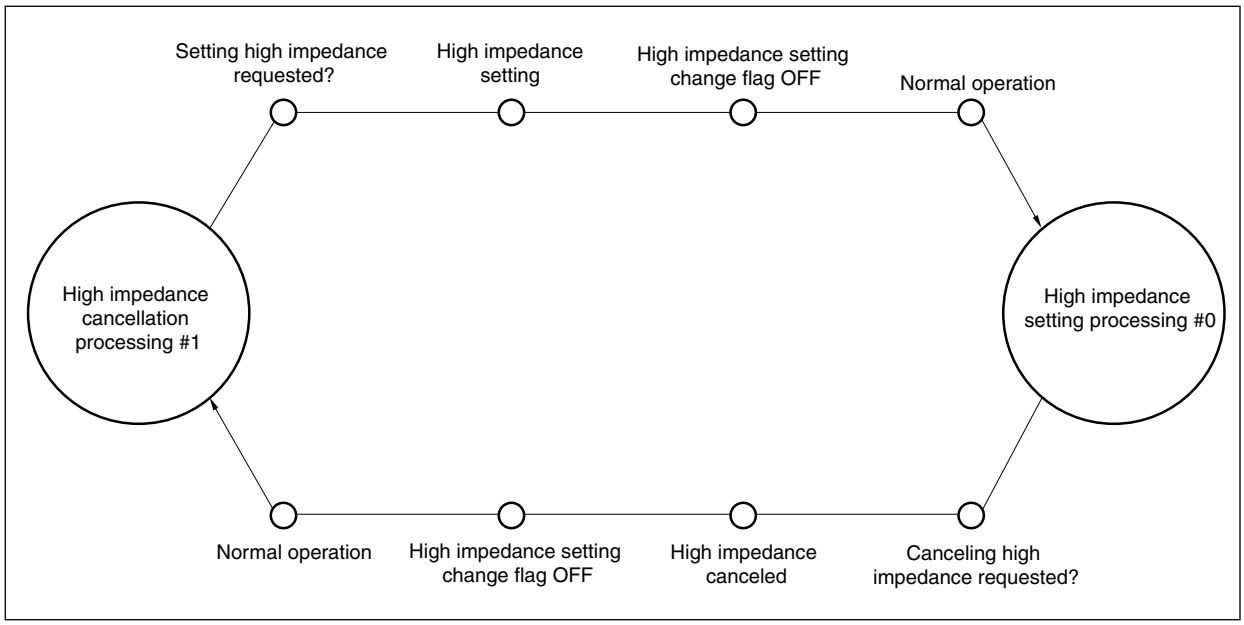
Figure 5-5. PWM Processing



5.6 High-Impedance Setting Processing

The flowchart of high-impedance setting processing is shown below.

Figure 5-6. High-Impedance Setting Processing



5.7 TM0 Valley Interrupt (INTTQ0OV) Servicing

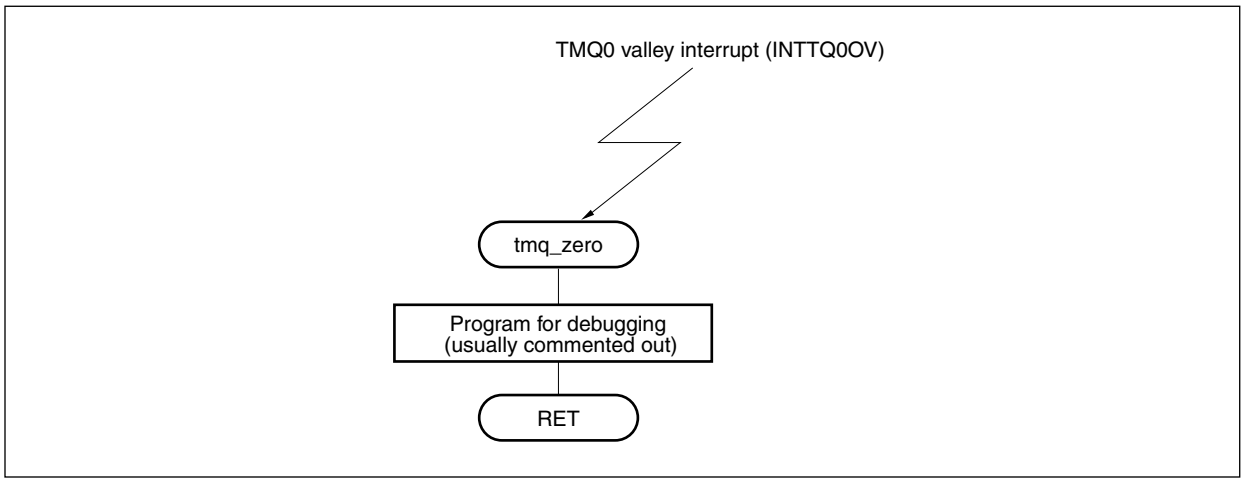
This processing is performed when the TM0 valley interrupt (INTTQ0OV) of carrier period is generated. It is used by the 3-phase PWM driver only for debugging and is not usually used. Therefore, program description is commented out.

When using the 3-phase PWM driver, delete the program for debugging.

Note that the priority level of the TMQ0 valley interrupt (INTTQ0OV) is 1.

The following flowchart illustrates the TMQ0 valley interrupt (INTTQ0OV) servicing.

Figure 5-7. MQ0 Valley Interrupt (INTTQ0OV) Servicing



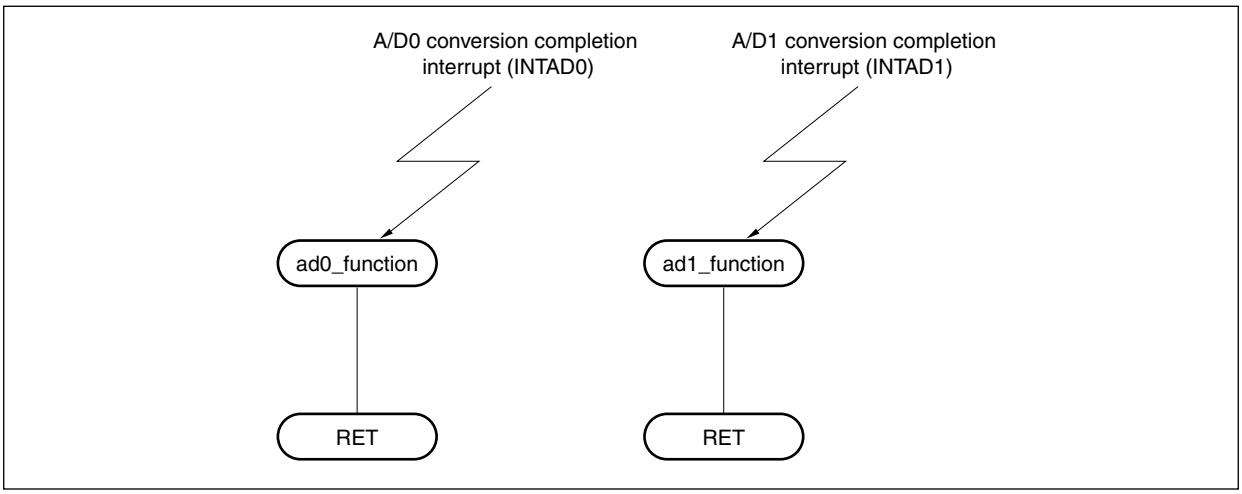
5.8 A/D Converters 0 and 1 Conversion Completion Processing

This function is called after conversion by A/D converters 0 and 1 is completed. The 3-phase PWM driver programs nothing in the function.

The priority level of the A/Dn conversion completion interrupt (INTADn) is 4 (n = 0 or 1).

The following flowchart illustrates the A/D converters 0 and 1 conversion completion processing.

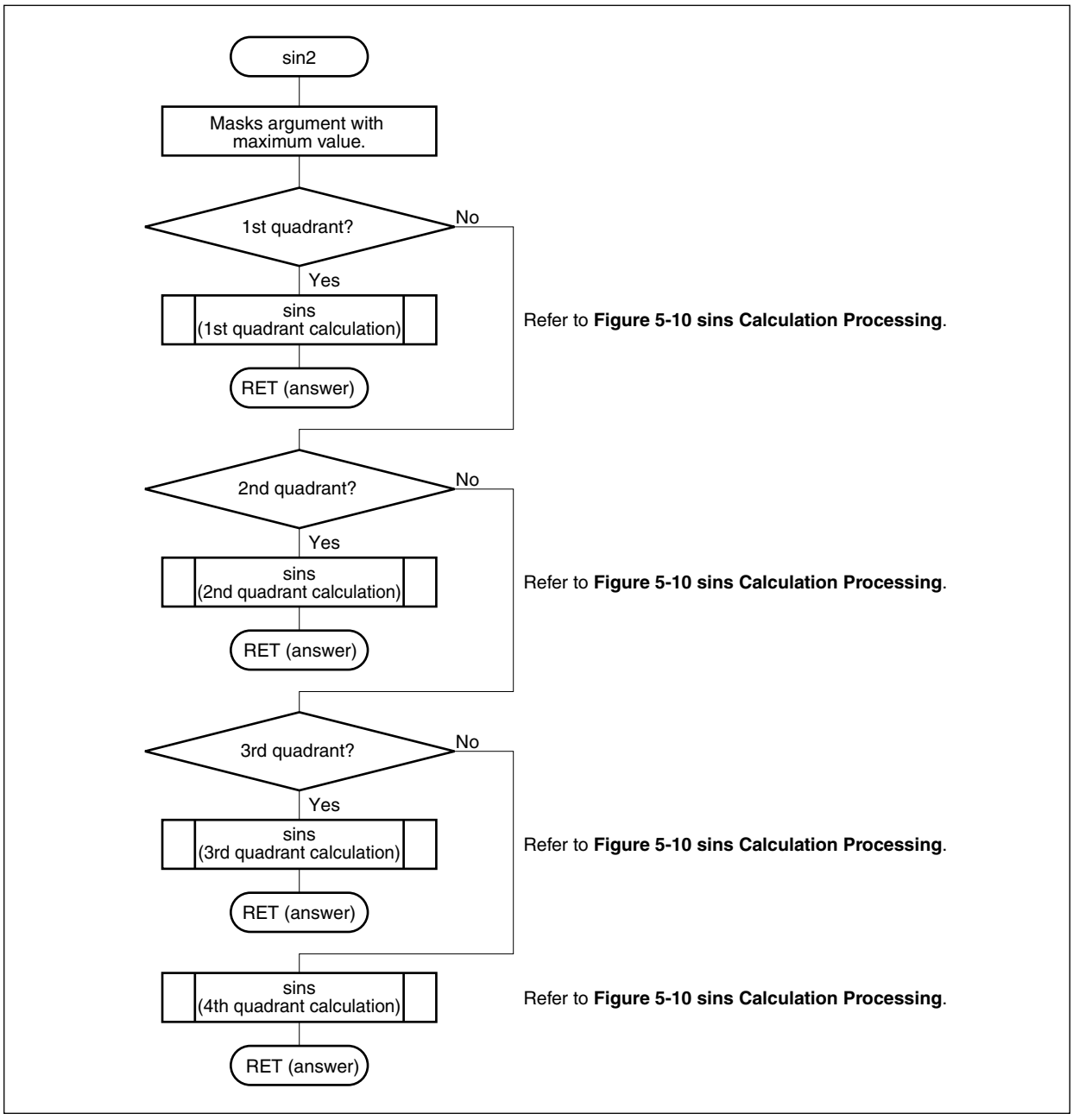
Figure 5-8. A/D Converters 0 and 1 Conversion Completion Processing



5.9 sin2 Calculation Processing

This function executes sin calculation by Taylor's expansion.
The following flowchart illustrates the sin2 calculation processing.

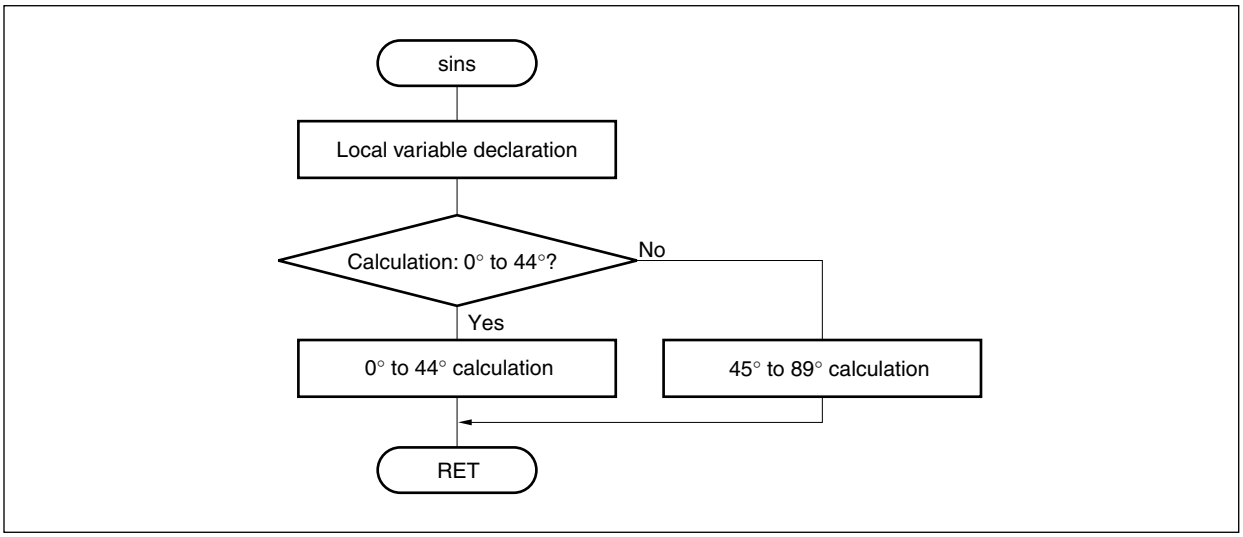
Figure 5-9. sin2 Calculation Processing



5.10 sins Calculation Processing

This function executes sins calculation by Taylor's expansion. It is called by sin2.
The following flowchart illustrates the sins calculation processing.

Figure 5-10. sins Calculation Processing



CHAPTER 6 SETTINGS

6.1 Settings of 3-Phase PWM Driver

The settings of the 3-phase PWM driver are shown below.

Table 6-1. Settings of 3-Phase PWM Driver

Parameter	Set Value
Operating clock of microcontroller	64 MHz (input clock: 8 MHz)
PWM output pin	TOQ0T1 to TOQ0T3, TOQ0B1 to TOQ0B3
Carrier frequency	20 kHz
Culling rate	1/1
Dead time	4 μs
A/D conversion start trigger timing of ANI00	1 μs after TMQ0 valley interrupt (INTTQ0OV) of carrier period
A/D conversion start trigger timing of ANI10	1 μs after TMQ0 valley interrupt (INTTQ0OV) of carrier period
A/D conversion completion time of ANI00	1.94 μs
A/D conversion completion time of ANI10	1.94 μs
Priority level of A/D0 conversion completion interrupt (INTAD0) of ANI00	Level 4
Priority level of A/D1 conversion completion interrupt (INTAD1) of ANI10	Level 4
Buffer mode of A/D converters 0 and 1	1-buffer mode
Synchronization operation	Performed

APPENDIX A INTERFACE BETWEEN MODULES

The following table shows the interfaces between the modules of the 3-phase PWM driver.

Table A-1. Interfaces Between Modules of 3-phase PWM Driver (1/2)

Transmission Module	Interface	Type	Symbol	Explanation	Reception Module
main()	Mode setting	B	pwm_mode	For setting 3-phase PWM mode 0x00: Direct mode 0x01: dq conversion mode 0x02: Output lock mode	pwm()
	Output enable	B	pwm_flag	Enables PWM output. 0x00: Changes mode of PWM output pin to high-impedance mode. 0x01: Changes mode of PWM output pin to PWM output mode.	
	Set 0	W	value0	Control value 0 In direct mode: U-phase duty (0 to 800) In dq conversion mode: d-axis current (−400 to 400)	
	Set 1	W	value1	Control value 1 In direct mode: V-phase duty (0 to 800) In dq conversion mode: q-axis current (−400 to 400)	
	Set 2	W	value2	Control value 2 In direct mode: W-phase duty (0 to 800) In dq conversion mode: Rotor rotation position (0 to 9,999)	
	x	LW	x	Passes x value of sin2 calculation processing. 0 to 9,999	sin2()

Remark B: Byte type
W: Word type
LW: Local word type

Table A-1. Interfaces Between Modules of 3-phase PWM Driver (2/2)

Transmission Module	Interface	Type	Symbol	Explanation	Reception Module
pwm()	pt_unit status	W	pwm() output	Passes status after pwm processing. 0x00 to 0x03, 0xff: Return value from hi-z function	main()
	x	LW	x	Passes x value of sin2 calculation processing. 0 to 9,999	sin2()
	High-impedance mode setting	B	hi_mode	Enables high-impedance mode. 0x00: High-impedance mode 0x01: Cancels high-impedance mode.	hi_z()
	hi_z flag	B	hi_flag	High-impedance mode setting change flag 0x00: High-impedance state is not changed. 0x01: Changing high-impedance state is enabled.	
Hi_z()	High-impedance state	W	hi_z() output	Passes status after high-impedance processing. 0x00: High-impedance state 0x01: Cancels high-impedance state. 0x02: None 0x03: Other mode	main() pwm()
sin2()	sin2answer	LW	sin2() output	Returns sin2 calculation result. Maximum value: 0x3fff Minimum value: 0xffffc001	main() pwm()
	x	LW	x	Passes x value for sins calculation processing. 0 to 2,499	sins()
sins()	sinanswer	LW	sins	Returns sins calculation result.	sin2()
				Maximum value: 0x3fff	
				Minimum value: 0xffffc001	

Remark B: Byte type
W: Word type
LW: Local word type

For further information, please contact:

NEC Electronics Corporation
1753, Shimonumabe, Nakahara-ku,
Kawasaki, Kanagawa 211-8668,
Japan
Tel: 044-435-5111
http://www.necel.com/

[America]

NEC Electronics America, Inc.
2880 Scott Blvd.
Santa Clara, CA 95050-2554, U.S.A.
Tel: 408-588-6000
800-366-9782
http://www.am.necel.com/

[Europe]

NEC Electronics (Europe) GmbH
Arcadiastrasse 10
40472 Düsseldorf, Germany
Tel: 0211-65030
http://www.eu.necel.com/

Hanover Office
Podbielskistrasse 166 B
30177 Hannover
Tel: 0 511 33 40 2-0

Munich Office
Werner-Eckert-Strasse 9
81829 München
Tel: 0 89 92 10 03-0

Stuttgart Office
Industriestrasse 3
70565 Stuttgart
Tel: 0 711 99 01 0-0

United Kingdom Branch
Cygnus House, Sunrise Parkway
Linford Wood, Milton Keynes
MK14 6NP, U.K.
Tel: 01908-691-133

Succursale Française
9, rue Paul Dautier, B.P. 52
78142 Velizy-Villacoublay Cédex
France
Tel: 01-3067-5800

Sucursal en España
Juan Esplandiu, 15
28007 Madrid, Spain
Tel: 091-504-2787

Tyskland Filial
Täby Centrum
Entrance S (7th floor)
18322 Täby, Sweden
Tel: 08 638 72 00

Filiale Italiana
Via Fabio Filzi, 25/A
20124 Milano, Italy
Tel: 02-667541

Branch The Netherlands
Steijgerweg 6
5616 HS Eindhoven
The Netherlands
Tel: 040 265 40 10

[Asia & Oceania]

NEC Electronics (China) Co., Ltd
7th Floor, Quantum Plaza, No. 27 ZhiChunLu Haidian
District, Beijing 100083, P.R.China
Tel: 010-8235-1155
http://www.cn.necel.com/

NEC Electronics Shanghai Ltd.
Room 2511-2512, Bank of China Tower,
200 Yincheng Road Central,
Pudong New Area, Shanghai P.R. China P.C:200120
Tel: 021-5888-5400
http://www.cn.necel.com/

NEC Electronics Hong Kong Ltd.
Unit 1601-1613, 16/F., Tower 2, Grand Century Place,
193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: 2886-9318
http://www.hk.necel.com/

NEC Electronics Taiwan Ltd.
7F, No. 363 Fu Shing North Road
Taipei, Taiwan, R. O. C.
Tel: 02-8175-9600
http://www.tw.necel.com/

NEC Electronics Singapore Pte. Ltd.
238A Thomson Road,
#12-08 Novena Square,
Singapore 307684
Tel: 6253-8311
http://www.sg.necel.com/

NEC Electronics Korea Ltd.
11F., Samik Lavied'or Bldg., 720-2,
Yeoksam-Dong, Kangnam-Ku,
Seoul, 135-080, Korea
Tel: 02-558-3737
http://www.kr.necel.com/