

V850E2/MN4

APPLICATION NOTE

DMA Control

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Introduction

This application note explains how to set up the DMA (Direct Memory Access) and also gives an outline of the operation and describes the procedures for using a sample program. The sample program supports DMA transfer between locations in internal memory and between the internal memory and the internal peripheral I/O.

Target Device

V850E2/MN4 Microcontrollers

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1. Overview

This sample program illustrates the usage examples of the DMAC (Direct Memory Access Controller) and DTFR (DMA Trigger Factor Register).

The parameters required for the transfer of data are stored in the DMAC, which transfers data in response to DMA transfer requests. As an example of software DMA transfer requests, the main points in the operation of the software to transfer data between locations in internal memory are illustrated below.

See section 4.1 "Flow Charts" for the details of the individual operations.



Figure 1.1 Example of Software DMA Transfer Request



The DTFR (DMA Trigger Factor Register) is used to select the interrupt signal which becomes the trigger for DMA from among all interrupt signals. Requests from the DTFR for the DMA transfer of data are handled by the DMAC. Specifically, the signal to be used as a DMA transfer request is selected from among the 128 input interrupt signals by the setting in DTFRn (n = 15 to 0). As an example of a hardware DMA transfer request, the main points in transferring data with a timer interrupt as the trigger are illustrated below. The data from internal RAM are output via port P0.

See section 4.1 "Flow Charts" for the details of the individual operations.



Figure 1.2 Example of Hardware DMA Transfer Request



1.1 Initialization

The general registers and functional pins are initialized.

<Port setup>

- Port n function control expansion registers (PFCEn)
- Port n function control registers (PFCn)
- Port n mode control registers (PMCn)
- Port n mode register (PMn)

1.2 DMAC Setup

The parameters required for the transfer of data are set in the DMAC. See section 4.2 for details.

- A transfer source address, a transfer destination address, and a transfer data size
- Chip select signals for a transfer source and a transfer destination
- A next transfer source address, a next transfer destination address, and a next transfer data size (as necessary)

1.3 DTFR Setup

The interrupt signal which will act as the DMA transfer factor is set.

1.4 DMAC Start

DMA transfer is enabled and the software request bit is set at the same time to start the DMAC transferring data in response to a software transfer request.

DMA transfer is enabled to start the DMAC transferring data in response to hardware transfer requests. Actual data transfer only starts when a request for transfer from the DTFR is triggered by an interrupt signal.

1.5 Wait for End of Transfer and End of Transfer

A transfer end interrupt generated after the DMA transfer indicates the end of transfer. Clearing the DMA transfer end status bit completes DMA transfer. The next address setting function can be used to automatically set the parameters for the next transfer.



2. Usage Environment

This section explains the circuit diagram and development environment to run this sample program.

2.1 Circuit Diagram

See "V850E2/MN4 Target Board User Manual: QB-V850E2MN4DUAL-TB (R20UT0683XJ)" for the details of the circuit diagram.

During data transfer between the internal memory and the internal peripheral I/O, the P0 port is set as the destination for transfer and acts as the output for the data.

The LEDs are connected to port 13. The P13_7 pin is used for LED1. The P13_6 pin is used for LED2.

2.2 Development Environment

It is necessary to install the tools that are listed below to run the sample program.

• CubeSuite+

The integrated development environment CubeSuite+ from Renesas Electronics provides various software development tools that are necessary for the user to develop applications. The user can use these tools seamlessly and easily in various development stages including coding, assembly, compilation, debugging using an emulator or simulator, and flash programming.

• MINICUBE

MINICUBE is a general-purpose in-circuit emulator from Renesas Electronics which adopts the JTAG interface system. It allows the user to debug an onboard real processor and provides highly transparent and stable emulation functionalities. An adapter is required to connect a TB board to MINICUBE.

• Multi

Green Hills software, Inc. integrated development tool suit.

IAR Embedded Workbench

IAR Systems integrated development tool suit.



3. Software

This section describes the organization of the compressed files to be downloaded.

3.1 File Organization

The compressed files to be downloaded consist of the files that are listed below.

File Name (Tool Structure)	Description	Common Source File	CubeSuite+ File	Multi File
crtE.s	Hardware initialization processing		•	
startup.s				•
V850E2MN4.dir	Link directive file		•	
V850E2_MN4 DMA.ld				•
vector.s	Vector table			•
dma.h	Variable and function declarations	•		
main.c	Main processing	•		
initial.c	Software initialization processing	•		
dma_control.c	DMA control	•		
taua0_control.c	Timer control as DMA start trigger	•		
interrupt.c	Interrupt processing	•		



4. Sample Application

This section explains how to set up the DMAC and the DTFR.

4.1 Flow Charts

The flow charts of this sample program are given below.

4.1.1 Main Processing

The main processing transfers data between locations in internal memory and between the internal RAM and internal peripheral I/O, after which processing ends.

See sections 4.1.2 and 4.1.3 for the details of the individual transfer processing.



Figure 4.1 Main Processing Flowchart



4.1.2 Inter-Memory Transfer Processing

This inter-memory transfer processing transfers data of specified size from the specified transfer source address to the transfer destination address. In this example, DMA transfer is started by the software.



Figure 4.2 Inter–Memory Transfer Processing



4.1.3 Memory-to-Peripheral I/O Transfer Processing Flow

This memory-to-peripheral I/O transfer processing transfers data from the transfer source address to peripheral I/O. In this example, DMA transfer is started by a timer interrupt.



Figure 4.3 Memory-to-Peripheral I/O Transfer Processing Flow



4.1.4 Interrupt Processing

The V850E2/MN4 is able to generate an interrupt when DMA transfer ends or the transfer count matches.

In the case of data transfer between locations in internal RAM, an interrupt signal (INTDMACT0) is generated when the amount of data transferred corresponds to the transfer count setting in the transfer number compare register (DTCC). LED1 is then turned on by the transfer number match interrupt function, int_dmact0.

In the case of data transfer between the internal RAM and the internal peripheral I/O, a transfer completion interrupt signal (INTDMA1) is generated when DMA transfer has been executed the number of times specified by the transfer count register (DTC). The transfer end interrupt function, int_dma1, clears the transfer end flag and then turns LED2 on.



Figure 4.4 Interrupt Processing



4.2 Register Setup

This section explains how to set up the relevant registers according to the flow charts shown in section 4.1. The registers described below must be configured to control the DMAC.

4.2.1 Port Setup

In this sample program, during data transfer between the internal memory and the internal peripheral I/O, the P0 port is set as the destination for transfer and acts as the output for the data. The LEDs are connected to port 13. The pertinent control registers must be set up as summarized in the table below. The P13_7 pin is used for LED1. The P13_6 pin is used for LED2.

Macro	Pin	PMC	PFCE	PFC	PM	Corresponding function
PORT	P0_0 to 15	0	0	0	0	Port mode, output
	P13_6	0	0	0	0	Port mode, output
	P13_7	0	0	0	0	Port mode, output

Setting example:

/* P0: io,output */ PFCE0 = 0x0000; PFC0 = 0x0000; PMC0 = 0x0000; PM0 = 0x0000; /* P13_6,7: LEDs,io,OUTPUT */ PFCE13 = 0x0000; PFC13 = 0x0000; PMC13 = 0x0000; PM13 = 0x0000;



4.2.2 DMA Transfer Status Register (DTSn)

The DTSn register has the DMA transfer end status, the DMA transfer status, the DMA transfer error flag, and the hardware DMA transfer request flag. This register enables or disables DMA transfer by using the DTE bit. This register starts and stops software DMA transfer by using the SR bit.

	Access		Ŭ.,				8- or 1-bit			
	ddress al Value	DTS1 DTS9 DTS6 DTS3 DTS0	2: FF : FF : FF : FF	FFF 75FA, FF 756A _H , FF 745A _H ,	, DTS11 DTS8: I DTS5: I	1: FFFF 753 FFFF 753 FFFF 742	765A _H , DT3 75CA _H , DTS7 3A _H , DTS7 2A _H , DTS4 9A _H , DTS1 3 <u>DTSnER</u> R	810: FFFF FFFF 74 FFFF 73	² 759A _H , 8A _H , FA _H , 6A _H , 1	0 DTSnDTE R/W
1997 - 1997 - 1997 - 1997 - 1997 - 1997 - 1997 - 1997 - 1997 - 1997 - 1997 - 1997 - 1997 - 1997 - 1997 - 1997 -	-		reg	Ister cont	ents (1/	<u> </u>	_			
Bit position	Bit n	ame					Function			
7	DTSnT		This clear man 0:		that DM ding "1" fr ch as CL ar not con	rom it. It i R1. npleted	r has been c s recommen			
6	DTSnD		This DM/ required com also 0:	transfer is est is issue pleted. If th	s that a D in progre d. This b e DTSnD at the san ar reques	ss. It is n it is cleare TE bit is " ne time as t acknowle	ier request h ot set (to "1" ed (to "0") wit o", this bit ca the DTSnD edged) when only hen DMA tra in be cleare	a DMA tra ansfer has l	nsfer been
3	DTSnEl		This clea read 0:		s that a D when the nsfer erro	DTRCx.D	er error has TRCxERR b			
2	DTSnD		This clear oper softv softv regis 0:	red (to "0") v ates regard vare DMA tr	s that cha when the l less of th ransfer re ransfer re nat this bi e DMA to	nnel n ha hardware e status o quest, or l quest is s t is read-o ansfer req	s a hardwar DMA transfe f the DTSnD by a hardwa elected by the nly. puest	er request is)TE bit. It is re DMA tra	deasserter s not set (to nsfer reque	d. This bit "1") by a st when a
1	DTSnSl		This required bit a (to "I DM/ 0:	est is select nd the DTS	a software ed by the nDTE bit MA transfe DMA tra	e DMA tra DMA tran starts DM er has bee nsfer requ	nster reques ster request A transfer. en complete uest	t select regi This bit is a	ster, writing utomatically	"1" to this cleared

Figure 4.5 DTSn Register Format (1/2)



Bit position	Bit name	Function
0	DTSnDTE	DMA transfer enable This bit enables or disables DMA transfer. DMA transfer is executed if "1" is written to this bit and a DMA transfer request is issued. This bit is automatically cleared (to "0") if the MLE bit is "0" when DMA transfer has been completed. DMA transfer is aborted if "0" is written to this bit during DMA transfer. 0: Disables DMA transfer 1: Enables DMA transfer



Setting examples

DTS0DTE = 0x0;	/* prohibit DMA trasnfer */
DTS0DTE = 0x1;	/* permit DMA transfer */
DTS0SR = 0x1;	/* transfer start */
,	



4.2.3 DMA Source Address Registers (DSAnL and DSAnH)

These registers set a DMA transfer source address.

	Access	This	regist	er can be	e read or w	vritten in 1	6-bit unit	s.		
A	ddress				4 _H , DSA1					
					H, DSA8L					
					H, DSA5L					
		DSA	3L: FF	FF 73A4	H, DSA2L	FFFF 7	374 _H , DS	A1L: FFF	F 7344	4.
		DSA	OL: FF	FF 7314	н					
Initia	il Value	0000	н							
		1	5	14	13	12	11	10	9	8
		SA	15	SA14	SA13	SA12	SA11	SA10	SAS	SA
		R/	W	R/W	R/W	R/W	R/W	R/W	R/W	R/V
		7	7	6	5	4	3	2	1	0
		SA	17	SA6	SA5	SA4	SA3	SA2	SAT	SA
		R/		R/W	R/W	R/W	R/W	R/W	R/W	
1.01.01	e 10-11	DSA	nL re	gister co	ontents					
Bit position 15:0	e 10-11 Bit na SA15 to	me	DMA Thes this n to be	source a e bits set egister is transferre	the lower 1 referenced ed next can	6 bits of the during DM be read. \	A transfer, When refer	the addre	ass from v is register	which data r, it is
Bit position	Bit na	me	DMA Thes this n to be recon NSA	source ar e bits set egister is transferre nmended / bit of the pleted, the	ddress the lower 1 referenced	6 bits of th during DM be read. V his register register is n	e transfer s A transfer, When refer together v iot set (to "	the addre encing the with DSAn 1*) when I	ass from v is register H in 32-b DMA tran	vhich data r, it is it units. If t sfer has be
Bit position 15:0	Bit na	1. W 2. Se or	DMA Thes this n to be recon NSAV comp starte riting to TSn.D arante at an a der to	source ar e bits set egister is transferre mmended / bit of the oleted, the ad. these bits DTSnDTE aed. address b	ddress the lower 1 referenced ed next can to access t DNSAnH r	6 bits of the during DM be read. \ his register is n hese bits re ited while If they are ng in 32-b	e transfer a A transfer, When refer together v oot set (to " atum to the DMA tran a written, it units w	the addre encing the with DSAr 1°) when I e values we asfer is e the open hile the D	ess from v is register H in 32-b DMA tran- then DMA nabled ation is r	which data r, it is it units. If t sfer has be transfer w not E bit is "0"
Bit position 15:0	Bit na SA15 to	I. W (D gu 2. Se or co 3. Di ad an Th	DMA Thes this n to be recon NSAV comp starte triting f TSn.D arante at an a der to omplete MA tra ddress ny bit).	source ar e bits set egister is transferre mmended / bit of the bleted, the ed. these bits DTSnDTE aed. address b avoid da ely set. correspo	ddress the lower 1 referenced ed next can to access t DNSAnH r values of t values of t s is prohib E bit = 1).	6 bits of the during DM be read. 1 his register is n hese bits re ited while If they are ng in 32-b ransferred d data is n the transfe	e transfer a A transfer, When refer together v oot set (to " eturn to the DMA tran owritten, it units wi from an ot suppor or data siz	the addre encing the with DSAr 1°) when I avalues we the open hile the D address ted. The	ess from v is register H in 32-b DMA tran- then DMA nabled ation is r DTSnDTR that has a lower 4 follows (which data r, it is it units. If t sfer has be transfer w transfer w tot E bit is "0" not been bits of ar (x indicate
Bit position 15:0	Bit na SA15 to	I. W (D gu 2. Se or co 3. Di ad an Th	DMA Thes this n to be recon NSAV comp starte triting f TSn.E arante at an a der to omplete MA tra idress of y bit). ne ope	source ar e bits set egister is transferre mmended / bit of the bleted, the ed. these bits DTSnDTE aed. address b avoid da ely set. correspo	ddress the lower 1 referenced ad next can to access t 2 DNSAriH I values of t values of t s is prohib E bit = 1). ny accessi ta being to misaligned onding to t not guara	6 bits of the during DM be read. 1 his register register is n hese bits re ited while if they are ng in 32-b ransferred d data is n the transfe nteed if a	e transfer s A transfer, When refer together v tot set (to " etum to the DMA tran a written, it units wi from an ot suppor er data siz	the addre encing th vith DSAr 1") when I values w sfer is e the open hile the D address ted. The se are as her than	ess from v is register H in 32-b DMA tran- then DMA nabled ation is r DTSnDTR that has a lower 4 follows (which data r, it is it units. If t sfer has be transfer w transfer w tot E bit is "0" not been bits of ar (x indicate
Bit position 15:0	Bit na SA15 to	I. W (D gu 2. Se or co 3. Di ad an Th ma	DMA Thes this n to be recon NSAV comp starte triting f TSn.E arante at an a der to omplete MA tra idress of y bit). ne ope	source ar e bits set egister is transferre nmended / bit of the bleted, the ed. these bits DTSnDTE eed. address b avoid da ely set. unsfer of r correspondent	ddress the lower 1 referenced ad next can to access t 2 DNSAriH I values of t values of t s is prohib E bit = 1). ny accessi ta being to misaligned onding to t not guara	6 bits of the during DM be read. V his register register is n hese bits re ited while If they are ng in 32-b ransferred d data is n the transfe nteed if a	e transfer s A transfer, When refer together v tot set (to " etum to the DMA tran a written, it units wi from an ot suppor er data siz	the addre encing th vith DSAr 1") when I values w sfer is e the open hile the D address ted. The se are as her than	ess from v is register H in 32-b DMA tran- then DMA nabled ation is n DTSnDTR that has a lower 4 follows (the follo	which data r, it is it units. If t sfer has be transfer w not E bit is "0" not been bits of ar (x indicate wing is
Bit position 15:0	Bit na SA15 to	I. W (D gu 2. Se or co 3. Di ad an Th ma 8	DMA Thes this n to be recon NSAV comp starte riting f TSn.D arante at an a der to omplete MA tra idress by bit). ne ope ade.	source ar e bits set egister is transferre nmended / bit of the bleted, the ed. these bits DTSnDTE eed. address b avoid da ely set. unsfer of r correspondent	ddress the lower 1 referenced ad next can to access t 2 DNSAriH I values of t values of t s is prohib E bit = 1). ny accessi ta being to misaligned onding to t not guara	6 bits of the during DM be read. 1 his register register is n hese bits re ited while If they are ng in 32-b ransferred d data is n the transfe nteed if a	e transfer a A transfer, When refer together v iot set (to " eturn to the DMA tran a written, it units wi from an ot suppor er data siz setting ot	the addre encing the with DSAr 1°) when I e values we asfer is e the open hile the D address ted. The address ted. The her than	ess from v is register iH in 32-b DMA tran- then DMA nabled ation is r DTSnDTR that has a lower 4 follows (the follo SA1	which data r, it is it units. If t sfer has be transfer w not bits of ar bits of ar (x indicate wing is SA0
Bit position 15:0	Bit na SA15 to	I. W SA0 1. W (D gu 2. Se or co 3. Di ad an Th ma 8 10	DMA Thes this n to be recon NSAV comp starte TSn.D arante at an a der to mplet MA tra ddress ny bit). ne ope ade.	source ar e bits set egister is transferre nmended / bit of the bleted, the ed. these bits DTSnDTE eed. address b avoid da ely set. unsfer of r correspondent	ddress the lower 1 referenced ad next can to access t 2 DNSAriH I values of t values of t s is prohib E bit = 1). ny accessi ta being to misaligned onding to t not guara	6 bits of the during DM be read. 1 his register register is n hese bits re ited while If they are ng in 32-b ransferred d data is n the transfe nteed if a	e transfer s A transfer, When refer together v tot set (to " etum to the DMA trans of set (to " etum to the DMA trans of support of support of support of support setting of A3 S ×	the addre encing the vith DSAr 1") when I e values we asfer is e the open hile the D address ted. The se are as her than address	ass from v is register H in 32-b DMA trans then DMA nabled ation is r DTSnDTH that has a lower 4 follows the follo SA1 ×	which data r, it is it units. If the sfer has be transfer we not E bit is "0" not been bits of ar (x indicate wing is SA0 ×
Bit position 15:0	Bit na SA15 to	I. W SA0 I. W (D gu 2. Se or co 3. Dh ad an Th ma 8 10 33	DMA Thes this n to be recorn NSAV comp starte TSn.D arante at an a der to ompleti WA tra idress by bit). ne ope ade.	source ar e bits set egister is transferre nmended / bit of the bleted, the ad. these bits DTSnDTE aed. address b avoid da ely set. 	ddress the lower 1 referenced ad next can to access t 2 DNSAriH I values of t values of t s is prohib E bit = 1). ny accessi ta being to misaligned onding to t not guara	6 bits of the during DM be read. V his register register is n hese bits re lited while If they are ng in 32-b ransferred d data is n the transfe nteed if a	e transfer a A transfer, When refer together v oot set (to " eturn to the DMA tran e written, it units wi from an ot suppor er data siz setting ot A3 S ×	the addre encing the with DSAr 1°) when I e values we asfer is e the oper- hile the D address ted. The ted. The ted are as her than	ass from v is register H in 32-b DMA tran- then DMA nabled ation is r DTSnDTR that has o lower 4 follows the follo SA1 × ×	which data r, it is it units. If the ster has be transfer we not bits of ar (x indicate wing is SA0 × 0



	Access	This	regis	ter can be	e read or v	written in 1	6-bit units	5.		
A	ddress	DSA	15H:	FFFF 76	66 _H , DSA	14H: FFFF	7636 _H , D	SA13H: F	FFF 760	B _H ,
		DSA	12H:	FFFF 75	D6 _H , DSA	11H: FFF	F 75A6 _H ,	DSA10H:	FFFF 757	6 _H ,
		DSA	9H: F	FFF 754	6 _H , DSA8	H: FFFF 7	516H, DS	A7H: FFF	F 7466 _H ,	
						H: FFFF 7				
		DSA	3H: F	FFF 73A	6 _H , DSA2	H: FFFF 7	376 _H , DS	A1H: FFF	F 7346 _H ,	
		DSA	OH: F	FFF 731	Бн					
Initia	al Value	0000	н							
		1	5	14	13	12	11	10	9	8
		0	1	0	0	SA28	SA27	SA26	SA25	SA2
		F	3	R	R	R/W	R/W	R/W	R/W	R/W
		7		6	5	4	3	2	1	0
		SA	23	SA22	SA21	SA20	SA19	SA18	SA17	SA1
		R/	W	R/W	B/W	R/W	R/W	R/W	R/W	R/V
Tabl	e 10-12	DSA	nH re	egister c						
Tabl	e 10-12 Bit na	10.000	nH re				unction			
and the second second		me			ontents					
Bit position	Bit na	me	DM/ The	egister co A source a se bits set	ontents ddress the higher	F 13 bits of ti	unction he transfer	source add	iress of cha	innel n.
Bit position	Bit na	me	DM/ The this	egister co A source a se bits set register is	ontents ddress the higher referenced	F 13 bits of th during DM	unction he transfer A transfer,	source add	Iress of cha	innel n.
Bit position	Bit na	me	DM/ The this to be reco	egister co A source a se bits set register is e transferm	ddress the higher referenced ed next can to access	F 13 bits of th during DM be read. 1 this register	unction he transfer A transfer, When refer r together v	source add the addres encing this vith DSAnL	Iress of cha s from whic register, it in 32-bit ur	unneln. hdata is nits. If t
Bit position	Bit na	me	DM/ The this to be reco	A source a se bits set register is e transferm mmended W bit of the	ddress the higher referenced ed next can to access DNSAnH	F 13 bits of th during DM be read. 1 this register register is r	unction he transfer A transfer, When refer t together v	source add the addres encing this vith DSAnL 1") when DI	Iress of cha s from whic register, it in 32-bit ur MA transfer	innel n. ih data is hits. If t has be
Bit position	Bit na	me	DM/ The this to be reco	A source a se bits set register is e transferre mmended W bit of the pleted, the	ddress the higher referenced ed next can to access DNSAnH	F 13 bits of th during DM be read. 1 this register	unction he transfer A transfer, When refer t together v	source add the addres encing this vith DSAnL 1") when DI	Iress of cha s from whic register, it in 32-bit ur MA transfer	innel n. h data i is hits. If ti has be
Bit position	Bit na	me	DM/ The this to be reco NS/ com	A source a se bits set register is e transferre mmended W bit of the pleted, the	ddress the higher referenced ed next can to access DNSAnH	F 13 bits of th during DM be read. 1 this register register is r	unction he transfer A transfer, When refer r together v hot set (to "	source add the addres encing this vith DSAnL 1") when DI	Iress of cha s from whic register, it in 32-bit ur MA transfer	innel n. h data i is hits. If ti has be
Bit position 12:0	Bit na SA28 to	me SA16	DM/ The this to b reco NS/ com start	egister co A source a se bits set register is e transferm mmended W bit of the pleted, the ted.	ddress the higher referenced ed next can to access DNSAnH values of t	F 13 bits of th during DM be read. 1 this register register is r these bits re	unction he transfer A transfer, When refer r together v hot set (to " eturn to the	source add the addres encing this vith DSAnL 1") when DP values wh	Iress of cha s from whic register, it in 32-bit ur MA transfer en DMA tra	innel n. h data i is hits. If ti has be
Bit position 12:0	Bit na	me SA16	DM/ The this to be reco NS/ com start	egister co A source a se bits set register is e transferm mmended V bit of the pleted, the ted.	ddress the higher referenced ed next can to access DNSAnH values of t	F 13 bits of th during DM be read. 1 this register register is r these bits re these bits re	unction he transfer A transfer, When refer r together v hot set (to " eturn to the DMA tran	source add the addres encing this vith DSAnL 1") when DP values whe ster is ena	Iress of cha s from whic register, it i in 32-bit ur MA transfer en DMA tra abled	innel n. h data i is hits. If ti has be
Bit position 12:0	Bit na SA28 to	me SA16 1. W (D	DM/ The this to be reco NSA com start	egister co A source a se bits set register is e transferm mmended V bit of the pleted, the ted.	ddress the higher referenced ed next can to access DNSAnH values of t	F 13 bits of th during DM be read. 1 this register register is r these bits re	unction he transfer A transfer, When refer r together v hot set (to " eturn to the DMA tran	source add the addres encing this vith DSAnL 1") when DP values whe ster is ena	Iress of cha s from whic register, it i in 32-bit ur MA transfer en DMA tra abled	innel n. h data i is hits. If t has be
Bit position 12:0	Bit na SA28 to	1. W 2. Se	DM/ The this to b reco NS/ com start riting (TSn. aran)	A source a se bits set register is e transferm mmended V bit of the pleted, the ted. these bit DTSnDTf teed. address t	ddress the higher referenced ed next can to access DNSAnH values of t values of t s is prohib E bit = 1).	F 13 bits of th during DM be read. 1 this register register is r these bits n ited while if they and ing in 32-b	unction he transfer A transfer, When refer together v hot set (to " eturn to the DMA tran e written, f	source add the addres encing this with DSAnL 1") when DI values wh ster is ena the operat	Iress of cha s from whic register, it i in 32-bit ur MA transfer en DMA tra abled ion is not 'SnDTE b	innel n. h data is nits. If t has be nsfer w
Bit position 12:0	Bit na SA28 to	1. W (D gu 2. Se	DM/ The this to b reco NSA com start riting TSn. jaran at an der to	A source a se bits set register is e transferm mmended V bit of the pleted, the ted. these bit DTSnDTf teed. address t	ddress the higher referenced ed next can to access DNSAnH values of t values of t s is prohib E bit = 1).	F 13 bits of th during DM be read. 1 this register register is r these bits n these bits n these bits n these bits n	unction he transfer A transfer, When refer together v hot set (to " eturn to the DMA tran e written, f	source add the addres encing this with DSAnL 1") when DI values wh ster is ena the operat	Iress of cha s from whic register, it i in 32-bit ur MA transfer en DMA tra abled ion is not 'SnDTE b	innel n. h data i hits. If th has be nsfer w it is "0"

Figure 4.8 DSAnH Register Format

Setting example

DSA0 = 0x1EDFA000; /* set transfer source address */



4.2.4 DMA Destination Address Register (DDAnL DDAnH)

These registers set a DMA transfer destination address.

	Access		register can						104 4	
	lddress		15L: FFFF 7 12L: FFFF 7 6L: FFFF 7 6L: FFFF 7 3L: FFFF 7 0L: FFFF 7	5E4 _H , DDA 54 _H , DDA8 44 _H , DDA5 84 _H , DDA2	11L: FFFF .: FFFF 75 .: FFFF 74	75B4 _H , 524 _H , DD 414 _H , DD	DDA10L A7L: FF A4L: FF	FF 7474	7584 _H 4 _H , 4 _H ,	
Initia	al Value	0000	Ън							
		1	5 14	13	12	11	10		9	в
		DA	15 DA14	DA13	DA12	DA11	DA10	D D	A9	DA8
		R	W R/W	R/W	R/W	R/W	R/W	R	w	R/W
		-	7 6	5	4	3	2		1	0
		D	A7 DA6	DA5	DA4	DA3	DA2	D	A1	DAO
		R	W R/W	R/W	R/W	R/W	R/W	R	w	R/W
Tab	le 10-17	DDA	nL register	contents						
Bit position	Bit na	ame	1		F	unction				
15:0	DA15 to	DAo	These bits a channel n. which data i it is recomm	ation address pecify the low If this register s to be transfe ended to acc t of the DND	ver 16 bits of is reference erred next cl ess this reg	ed during an be read ister toget	DMA tran 1. When her with [nsfer, the referenci DDAnH in	e addres ng this n 32-bit	ss to register units. I
15:0	DA15 to		These bits : channel n. which data i it is recomm the NDAV b been compl transfer was	pecify the low if this register is to be transfe ended to account t of the DND/ eted, the value started.	ver 16 bits of is reference erred next cleass this reg AnH registe es of these	ed during an be read ister toget r is not se bits return	DMA tran i. When the her with [t (to "1") to to the w	nsfer, the referenci DDAnH ir when DN alues wh	e addres ng this n 32-bit MA trans ien DM	ss to register units. I sfer has
15:0		1. W (E gu 2. Sé or oc 3. If	These bits a channel n. which data i it is recomm the NDAV b been completence transfer was riting these DTSn.DTSnE uaranteed. at an address der to avoid ompletely se an error occorrite cycle is n	pecify the low if this register is to be transfe ended to account it of the DND/ eted, the value started. Dits is prohib (TE bit = 1). Is by access data being the urs in the transference of executed	ver 16 bits of is reference arred next class this reg AnH registe es of these vited while If they are ing in 32-b ransferred nsfer targe	ed during an be read ister toget r is not se bits return DMA tra e written, oit units w I from an et in the r estination	DMA trai t. When i her with 0 t (to "1") ' n to the vi nsfer is (the ope hile the address ead cycl address	nster, the referenci DDAnH ir when DN alues wh enabled ration is DTSnD s that ha le of DW s is upd	e addree ng this n 32-bit MA trans en DM s not TE bit is not ts not t MA tran lated.	ss to register units. I sfer has A is "0" ir been usfer, th
15:0	DA15 to	1. W (D gu 2. Se or oc 3. If w 4. Di ac ar	These bits a channel n. which data i it is recomm the NDAV b been completence (Transfer was riting these (TSn.DTSnE uaranteed.) at an address der to avoid ompletely se an error occorrite cycle is in MA transfer iddress corre by bit). The correct made.	pecify the low if this register is to be transfe ended to account it of the DND/ eted, the value started. Dits is prohib (TE bit = 1). Is by access data being to burs in the transfer to executed of misaligne sponding to peration is r	ver 16 bits of is reference arred next class this reg AnH registe es of these bited while If they are ing in 32-b ransferred nsfer targe but the de d data is n the transfe of guaran	ed during an be read ister toget r is not se bits return DMA tra e written, of units w I from an et in the r estination tot suppo er data si teed if a s	DMA trai t. When i her with 0 t (to "1") 'n to the vi noter is o the ope hile the address ead cycl address rted. Th ze are a setting o	nster, the referenci DDAnH ir when DN alues wh enabled ration is DTSnD s that ha le of DN s is upd he lower s follow: wher tha	a addressing this in 32-bit MA transion DM is not TE bit is not ta not ta transion (A transion (A transion (A transion (A transion) (A	is "0" in been isfer, th of an dicates
15:0	DA15 to	1. W (D gu 2. Se or oc 3. If w 4. Di ac ar is	These bits a channel n. which data i it is recomm the NDAV b been completence (Triting these (TSn.DTSnE uaranteed. at an address der to avoid ompletely se an error occo rite cycle is no MA transfer ddress corre by bit). The completence made.	pecify the low if this register is to be transfe ended to account it of the DND/ eted, the value started. Dits is prohib (TE bit = 1). Is by access data being to bot executed of misaligne sponding to	ver 16 bits of is reference arred next class this reg AnH registe es of these bited while If they are ing in 32-b ransferred but the de d data is n the transfe tot guaran	ed during an be read ister toget r is not se bits return DMA tra e written, bit units w d from an et in the r estination not suppo er data si teed if a s	DMA trai i. When ther with 0 t (to "1") to the with not the ope the	nster, the referenci DDAnH ir when DN alues wh enabled ration is DTSnD s that ha le of DN s is upd he lower s follow: ther tha	a addressing this in 32-bit MA transien DM is not TE bit is not TE bit is not MA transient MA transient is not taked. A bits is (x incompared in the f	is "0" in been of an dicates followin
15:0	DA15 to	1. W (D gu 2. Se or oc 3. If w 4. Di ac ar is 8	These bits a channel n. which data i it is recomm the NDAV b been completence (TSn.DTSnE uaranteed. at an address der to avoid ompletely se an error occor rite cycle is i MA transfer iddress corre by bit). The cor made.	pecify the low if this register is to be transfe ended to account it of the DND/ eted, the value started. Dits is prohib (TE bit = 1). Is by access data being to burs in the transfer to executed of misaligne sponding to peration is r	ver 16 bits of is reference erred next class this reg AnH registe es of these bited while If they are ing in 32-b ransferred nsfer targe but the de d data is n the transfe tot guaran	ed during an be read ister toget r is not se bits return DMA tra e written, of units w I from an et in the r estination toot suppo er data si teed if a s	DMA trai t. When i her with 0 t (to "1") 'n to the vi- insfer is o the ope hile the address ead cycl address rted. Th ze are a setting o DA2 ×	nsfer, the referenci DDAnH ir when DM alues wh enabled ration is DTSnD s that ha le of DM s is upd he lower s follow: wher tha DA1 ×	addree ng this n 32-bit AA transen DM s not TE bit as not tas not t tA trans ated. r 4 bits s (× inc in the f	ss to register units. I sfer has A is "0" ir been usfer, th of an dicates followin
15:0	DA15 to	1. W (D gu 2. Sé or oc 3. If w 4. Di ac ar is	These bits a channel n. which data i it is recomm the NDAV b been completence Triting these DTSn.DTSnE uaranteed. at an address der to avoid ompletely se an error occorrite cycle is n MA transfer iddress corre by bit). The c made. Data bits 6 bits	pecify the low if this register is to be transfe ended to account it of the DND/ eted, the value started. Dits is prohib (TE bit = 1). Is by access data being to burs in the transfer to executed of misaligne sponding to peration is r	ver 16 bits of is reference erred next class this reg AnH registe es of these vited while If they are ing in 32-b ransferred but the data d data is no the transfer to guaran	ed during an be read ister toget r is not se bits return DMA tra e written, bit units w l from an et in the r estination tot suppo ar data si teed if a se NA3	DMA trai i. When i her with 0 t (to "1") 'n to the vi- insfer is (the ope hile the address ead cycle address rted. The ze are a setting of DA2 × ×	nster, the referenci DDAnH ir when DM alues wh enabled ration is DTSnD s that ha le of DM s is upd he lower s follower s follower ther tha DA1 ×	addree ng this n 32-bit AA transien DM s not TE bit is not ta tran ated. r 4 bits s (× inc in the f	ss to register units. I sfer has A is "0" ir been usfer, th of an dicates followin
15:0	DA15 to	1. W (D gu 2. Se or cc 3. If 4. Di ac ar is 8 1 3	These bits a channel n. which data i it is recomm the NDAV b been completence (TSn.DTSnE uaranteed. at an address der to avoid ompletely se an error occor rite cycle is i MA transfer iddress corre by bit). The cor made.	pecify the low if this register is to be transfe ended to account it of the DND/ eted, the value started. Dits is prohib (TE bit = 1). Is by access data being to burs in the transfer to executed of misaligne sponding to peration is r	ver 16 bits of is reference erred next class this reg AnH registe es of these vited while If they are ing in 32-b ransferred but the de d data is n the transfe tot guaran	ed during an be read ister toget r is not se bits return DMA tra e written, of units w I from an et in the r estination toot suppo er data si teed if a s	DMA trai t. When i her with 0 t (to "1") 'n to the vi- insfer is o the ope hile the address ead cycl address rted. Th ze are a setting o DA2 ×	nsfer, the referenci DDAnH ir when DM alues wh enabled ration is DTSnD s that ha le of DM s is upd he lower s follow: wher tha DA1 ×	addree ng this n 32-bit AA transen DM s not TE bit as not tA translated. A translated.	is "0" in been of an dicates followin



A	ddress	DDA DDA DDA DDA	12H: 9H: F 6H: F 3H: F	FFFF 75 FFF 755 FFF 744	E6 _H , DDA 6 _H , DDA8 6 _H , DDA5 6 _H , DDA2	14H: FFFF 11H: FFFF H: FFFF 7 H: FFFF 7 H: FFFF 7	F 75B6 _H , 1 526 _H , DD 416 _H , DD	DDA10H: A7H: FFF A4H: FFF	FFFF 758 F 7476 _H , F 73E6 _H ,	
Initia	al Value	0000	н							
		1	5	14	13	12	11	10	9	8
		0)	0	0	DA28	DA27	DA26	DA25	DA2
		F	3	R	R	R/W	R/W	R/W	R/W	R/W
		7	1	6	5	4	3	2	1	0
		DA	23	DA22	DA21	DA20	DA19	DA18	DA17	DA1
		R/	W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit position	e 10-18 Bit na			agister co	ontents	F	unction			
	1	ame	DMA The char whic it is r	A destinations se bits spe nel n. If ti th data is to recommen	on address cify the hig his register b be transfe ded to acc	her 13 bits is reference arred next class this reg	of the tran ed during I an be read. jister togeth	When refe er with DD	er, the addr erencing thi AnL in 32-1	ress to s registe bit units.
Bit position	Bit na	ame	DM/ Thes char whic it is i If the beer	A destinations se bits spe nel n. If the recomment a NDAV bit	on address cify the hig his register b transfe ded to acc of the DND d, the valu	her 13 bits is reference	of the tran ed during I an be read. jister togett er is not se	OMA transfe When refe ner with DD t (to "1") wh	er, the addr erencing thi AnL in 32-1 ien DMA tra	ress to s regist bit units ansfer h

Figure 4.10 DDAnH Register Format

Setting example

DDA0 = 0x1EDFB000; /* set transfer destination address */



4.2.5 DMA Source Chip Select Register (DSCn)

This register specifies an area to be selected as a transfer source of channel n.

P	CCess	This re	gister can	be read	or written	in 16-bit uni	ts.		
Ad	ddress	DSC12 DSC9: DSC6: DSC3:	2: FFFF 75 FFFF 754 FFFF 743	5D8 _H , DS 48 _H , DSC 38 _H , DSC A8 _H , DSC	C11: FFF 8: FFFF 7 5: FFFF 7	F 7638 _H , DS F 75A8 _H , DS 7518 _H , DSC7 7408 _H , DSC4 7378 _H , DSC	SC10: FFF 7: FFFF 74 4: FFFF 73	F 7578 _H , 68 _H , D8 _H ,	
Initial	l Value	0001 _H							
		15	14	13	12	11	10	9	8
		0	0	0	0	0	0	0	0
		R	R	R	R	R	R	R	R
		7	6	5	4	3	2	1	0
			0	0	0	0	SCS1	SCS0	SCSE
		0	0	· ·					
Table	9 10-13	R	R R	R	R	R	R/W	R/W	R/W
Table Bit position 2 1 0	Bit na SCS1 SCS0 SCSE	R DSCn me	R register o	R contents e chip sele	ct	R Function selected as th			R/W
Bit position	Bit na SCS1 SCS0	R DSCn me	R register o	R contents e chip sele	ct	Function		ource of ch	R/W
Bit position	Bit na SCS1 SCS0	R DSCn me	R register o DMA source These bits s	R contents e chip sele specify an	ct area to be	Function	ne transfer s Selected mory area, F	ource of ch area 2-bus periph	R/W
Bit position	Bit na SCS1 SCS0	R DSCn me	R register o DMA source These bits s SCS1	R contents e chip sele specify an SCS0	ct area to be SCSE	Function selected as th	ne transfer s Selected mory area, F bus periphe	ource of ch area D-bus periph ral I/O area	R/W annel n.
Bit position	Bit na SCS1 SCS0	R DSCn me	R register o DMA source These bits s SCS1 0	R contents specify an SCS0 0 1	ct area to be SCSE 1	Function selected as th External mer area, and H-	ne transfer s Selected mory area, F bus periphe memory ar	ource of ch area D-bus periph ral I/O area	R/W annel n.

Figure 4.11 DSCn Register Format

Setting example

DSC0 = 0x0002; /* set DMA source is inner RAM */



4.2.6 DMA Destination Chip Select register (DDCn)

This register specifies an area to be selected as a transfer destination of channel n.

,									
	Access	This regi	ster can b	e read or	written in	16-bit unit	s.		
A	ddress	DDC12: DDC9: F	FFFF 75E FFF 7558	8 _H , DDC1 _H , DDC8:	11: FFFF FFFF 75	7648 _H , DD 75B8 _H , DD 28 _H , DDC7	0C10: FFF 7: FFFF 74	F 7588 _H , 78 _H ,	
						18 _H , DDC4 88 _H , DDC1			
			FFF 7328			оон, ооо		н,	
Initia	al Value	0001 _H							
		15	14	13	12	11	10	9	8
		0	0	0	0	0	0	0	0
		R	R	R	R	R	R	R	R
		7	6	5	4	3	2	1	0
		0	0	0	0	0	DCS1	DCS0	DCSE
		R	R	R	R	R	R/W	R/W	R/W
Tabl	e 10-19	DDCn re	gister co	ntents					
Ditmonition									
Bit position	Bit na	me				Function			
2 1 0	Bit na DCS1 DCS0 DCSE	DM	1A destinati ese bits spe	ion chip sel acify an are	lect	Function lected as th	e transfer d	estination o	f channel
2	DCS1 DCS0	DM	IA destinati ese bits spe DCS1	ion chip sel acify an are DCS0	lect		e transfer d Selected		f channel
2	DCS1 DCS0	DM	ese bits spe	ecify an are	lect sa to be se	lected as th		1 area a, P-bus per	ripheral
2	DCS1 DCS0	DM	DCS1	DCS0	ect a to be se DCSE	lected as th External m I/O area, a	Selected	1 area a, P-bus per eripheral V(ripheral D area
2	DCS1 DCS0	DM	DCS1	DCS0 0 1	ect a to be se DCSE 1	lected as th External m I/O area, a	Selected nemory area and H-bus p sh memory	1 area a, P-bus per eripheral V(ripheral D area
2	DCS1 DCS0	DM	DCS1 0	DCS0 0 1	ect a to be se DCSE 1	lected as th External m VO area, a Internal fla	Selected nemory area and H-bus p sh memory	1 area a, P-bus per eripheral V(ripheral D area
2 1 0	DCS1 DCS0 DCSE	DM The n.	DCS1 0 0 Other tha g these bit	DCS0 0 1 n above ts is prohil E bit = 1).	DCSE 1 0 bited while If they a	External m I/O area, a Internal fla Setting pro	Selected nemory area and H-bus p sh memory ohibited nsfer is ena the operat	d area a, P-bus per eripheral I/C and interna abled ion is not	ripheral O area al RAM
2 1 0	DCS1 DCS0 DCSE	DM The n. 1. Writing (DTSn guarar 2. Set the	DCS1 0 0 Other tha DTSnDT nteed. e DCS0 ar	DCS0 0 1 n above ts is prohil E bit = 1).	DCSE 1 0 bited while If they a bits so that	lected as th External m VO area, a Internal fla Setting pro	Selected memory area and H-bus p sh memory ohibited msfer is ena the operat of them is	d area a, P-bus per eripheral I/C and interna abled ion is not	ripheral O area al RAM
2 1 0	DCS1 DCS0 DCSE	DM The n. 1. Writing (DTSn guarar 2. Set the bits an	DCS1 0 0 Other tha DTSnDT nteed. e DCS0 ar	DCS0 0 1 n above ts is prohit E bit = 1).	DCSE 1 0 bited while bits so the ation is no	External m I/O area, a Internal fla Setting pro	Selected memory area and H-bus p sh memory ohibited msfer is ena the operat of them is	d area a, P-bus per eripheral I/C and interna abled ion is not	ripheral O area al RAM

Figure 4.12 DDCn Register Format

Setting examples

DDC0 = 0x0002;	/* set DMA destination is inner RAM */
DDC1 = $0x0001;$	/* set DMA destination is IO */



4.2.7 DMA Transfer Count Register (DTCn)

This register specifies the number of times of DMA transfers (DMA transfer count). When this register is referenced during DMA transfer, the remaining number of times of DMA transfer to be executed can be read.

DCT DCT DCT			This register can be read or written in 16-bit units. DCT15: FFFF 7682 _H , DCT14: FFFF 7652 _H , DCT13: FFFF 7622 _H , DCT12: FFFF 75F2 _H , DCT11: FFFF 75C2 _H , DCT10: FFFF 7592 _H , DCT9: FFFF 7562 _H , DCT8: FFFF 7532 _H , DCT7: FFFF 7482 _H , DCT6: FFFF 7452 _H , DCT5: FFFF 7422 _H , DCT4: FFFF 73F2 _H , DCT3: FFFF 73C2 _H , DCT2: FFFF 7392 _H , DCT1: FFFF 7362 _H ,							
			FFF 7332 _H			H		-Hi		
Initia	il Value	0000 _H								
		15	14	13	12	11	10	9	8	
		0	DTC14	DTC13	DTC12	DTC11	DTC10	DTC9	DTCa	
		R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
		7	6	5	4	3	2	1	0	
		DTC7	DTC6	DTC5	DTC4	DTC3	DTC2	DTC1	DTC	
1100 C 200	-		egister conte	ents						
Bit position 14:0	Bit na DTC14 b	o Dł	MA transfer co		90 - 72	unction				
and the second second		o DM Th for rer	MA transfer co lese bits speci r channel n. W maining numb ICV bit of the l hen DMA trans	fy the nur Vhen this er of time DNTCn re	mber of tim register is i s DMA trar egister is n	es of DMA referenced sfer to be o of set (to "1	during DM/ executed ca "), these bit	A transfer, t an be read.	the If the	
and the second second	DTC14 b	o DM Th for rer	ese bits speci r channel n. W maining numb ICV bit of the I	fy the nur Vhen this er of time DNTCn re	mber of tim register is i s DMA trar egister is n	es of DMA referenced aster to be ot set (to "1 eted (0000f	during DM/ executed ca "), these bit	A transfer, t an be read.	the If the	
and the second second	DTC14 b	o DM Th for rer	ese bits speci r channel n. W maining numb ICV bit of the I ben DMA trans	ify the nur Vhen this er of time DNTCn re sfer has b	nber of tim register is i s DMA trar egister is no een comple r executed	es of DMA referenced isfer to be o ot set (to "1 eted (0000) The op	during DM/ executed ca '), these bit I).	A transfer, t an be read. ts hold the	the If the values	
and the second second	DTC14 b	o DM Th for rer	ese bits speci r channel n. W maining numb ICV bit of the l hen DMA trans	ify the nur Vhen this er of time DNTCn re sfer has b Transfe transfe	nber of tim register is n s DMA tran egister is n een comple r executed r	es of DMA referenced isfer to be (ot set (to "1 eted (0000) The op 32,768 tim	during DM/ executed ca "), these bit 1). eration	A transfer, 1 an be read. ts hold the completion	the If the values of	
and the second second	DTC14 b	o DM Th for rer	ese bits speci r channel n. W maining numb ICV bit of the l nen DMA trans DTC[14:0] 0000H 0001H	fy the nur Vhen this er of time DNTCn re sfer has b Transfe transfe 	nber of tim register is n egister is no een comple r executed r r executed	es of DMA referenced state to be (ot set (to "1 eted (0000) The op 32,768 tim once or tra	during DM/ executed ca "), these bit 4). es or until o unsfer to be	A transfer, an be read, ts hold the completion executed (the If the values of once	
and the second second	DTC14 b	o DM Th for rer	ese bits speci r channel n. W maining numb ICV bit of the l pen DMA trans DTC[14:0] 0000H	fly the nur Vhen this er of time DNTCn re sfer has b Transfe transfe Transfe 	nber of tim register is n egister is no een comple r executed r r executed	es of DMA referenced state to be (ot set (to "1 eted (0000) The op 32,768 tim once or tra	during DM/ executed ca "), these bit 4). eration es or until o	A transfer, an be read, ts hold the completion executed (the If the values of once	

Figure 4.13 DTCn Register Format

Setting examples

DTC0	= 0x0004;	/* set times of DMA transfer */	
DTC1	= 0x0001;	/* set times of DMA transfer */	



4.2.8 DMA Transfer Control Register (DTCTn)

This register specifies parameters, such as DMA transfer data size.

A	Address	DTCT1 DTCT9 DTCT6 DTCT3	5: FFFF 76 2: FFFF 756 3: FFFF 756 3: FFFF 745 3: FFFF 73C 3: FFFF 73C	F8 _H , DTC 8 _H , DTCT 8 _H , DTCT 8 _H , DTCT	T11: FFFF 8: FFFF 75 5: FFFF 74	75C8 _H , I 38 _H , DT(28 _H , DT(OTCT10: F CT7: FFFF CT4: FFFF	FFF 759 7488 _H , 73F8 _H ,	
Initia	al Value	0000 _H							
		15	14	13	12	11	10	9	8
		0	DS1	DSo	MLE	0	0	0	0
		R	R/W	R/W	R/W	R	R	R	R
		7	6	5	4	3	2	1	0
		SACM	1 SACMO	DACM1	DACMO	0	0	0	DSM
		R/W	R/W	R/W	R/W	R	R	B	R/W
Tabl Bit position	le 10-26 Bit na	111	register co	ontents (nction			_
14 13	DS1 DS0		MA transfer hese bits spe	ecity the D	MA transfer d		f channel n sfer data si		
			1151	1150		Irans	sier data si	78	
			DS1 0	DS0	8 bits	trans	sier data si	ze	
			10000	0.0820	8 bits 16 bits	Iran	sier data si	ze	
			0	0		Iran	sier data si	28	_
			0	0	16 bits	Iran	sier data si	ze	_
12	MLE	T if e	0 0 1 1 Multi-link enab this bit specifi the DTSnTC this bit is set of DMA transfe executed if a I 0: Clears DT 1: Does not	0 1 0 1 bit is not c t (to "1"), th er. Even if DMA transf "SnDTE bit clear DTS:	16 bits 32 bits 128 bits r to acknowle leared (to "0" ne DTSn.DTS the DTSnTC er request is t upon comple DTE bit upon	edge the n) after DM nDTE bit bit is not issued. etion of D n complet	ext DMA tra A transfer h is not clean cleared, DM MA transfer ion of DMA	ansfer requ las been c ed upon co MA transfe	ompleted ompletion
12 7 6	MLE SACM1 SACM0	T if e E T	0 1 1 Multi-link enable This bit specifi The DTSnTC this bit is set of DMA transference of DMA transference the DTSnTC this bit is set of DMA transference the DTSnTC this bit specified the DTSnTC the DTSnTC this bit specified the DTSnTC this bit specified the DTSnTC the	0 1 0 1 ble bit is not o t (to "1"), th er. Even if DMA transf "SnDTE bit clear DTS source add actify the di	16 bits 32 bits 128 bits table ared (to "0" be DTSn.DTS the DTSn.TC er request is t upon comple hDTE bit upor dress counting	edge the n) after DM nDTE bit bit is not issued. etion of D n complet g direction	ext DMA tra A transfer h is not clean cleared, DM MA transfer ion of DMA	ansfer requ as been c ed upon co MA transfe transfer.	ompleted ompletion r is
7	SACM1	T if e E T	0 0 1 1 Multi-link enab this bit specifi the DTSnTC this bit is set of DMA transfe executed if a I 0: Clears DT 1: Does not 0) MA transfer These bits specified	0 1 0 1 ble bit is not o t (to "1"), th er. Even if DMA transf "SnDTE bit clear DTS source add actify the di	16 bits 32 bits 128 bits table ared (to "0" be DTSn.DTS the DTSn.TC er request is t upon comple hDTE bit upor dress counting	edge the n) after DM nDTE bit bit is not issued. etion of D n complet g direction ch the trai	ext DMA tra A transfer h is not clean cleared, DM MA transfer ion of DMA	ansfer requ as been c ed upon co MA transfe transfer. e address (ompleted ompletion r is
7	SACM1	T if e E T	0 0 1 1 Multi-link enable the DTSnTC this bit is set of DMA transfer executed if a D 0: Clears DT 1: Does not 0: Clears DT 1: Does not 0: Clears bit is set is to be cour	0 1 0 1 bit is not o t (to "1"), th er. Even if DMA transf "SnDTE bit clear DTS: source add acity the di nted.	16 bits 32 bits 128 bits table ared (to "0" be DTSn.DTS the DTSn.TC er request is t upon comple hDTE bit upor dress counting	edge the n) after DM nDTE bit bit is not issued. etion of D n complet g direction ch the trai	ext DMA tra A transfer h is not clean cleared, DM MA transfer ion of DMA n sfer source	ansfer requ as been c ed upon co MA transfe transfer. e address (ompleted ompletion r is
7	SACM1	T if e E T	0 0 1 1 1 Aulti-link enab this bit specific the DTSnTC this bit is set f DMA transfer 0: Clears DT 1: Does not 0: Clears DT 0: Clears DT 0: Clears DT	0 1 0 1 bit is not of t (to "1"), th er. Even if DMA transl Clear DTSr source ado ecity the di inted. SACMO	16 bits 32 bits 128 bits 128 bits r to acknowle leared (to "0" be DTSn.DTS the DTSn.DTS the DTSn.TC er request is t upon comple DTE bit upo dress counting rection in white Incremented Decremented	edge the n) after DM nDTE bit bit is not issued. etion of D n complet g direction ch the trai Count	ext DMA tra A transfer h is not clean cleared, DM MA transfer ion of DMA n sfer source	ansfer requ as been c ed upon co MA transfe transfer. e address (ompleted ompletion r is
7	SACM1	T if e E T	0 0 1 1 Multi-link enable this bit specific the DTSnTC this bit is set of DMA transfer executed if a I 0: Clears DT 1: Does not 0: Clears DT 0: C	0 1 0 1 0 1 0 1 0 1 0 0 0 1 0 1 0 1 0 0 1 1 1 1 1 1 1 1 1 1 1 1 1	16 bits 32 bits 128 bits r to acknowle leared (to "0" be DTSn.DTS the DTSn.DTS the DTSnTC er request is t upon comple DTE bit upo dress counting rection in white Incremented	edge the n) after DM nDTE bit bit is not issued. etion of D n complet g direction ch the trai Coun d ed	ext DMA tra A transfer h is not clean cleared, DM MA transfer ion of DMA n sfer source	ansfer requ as been c ed upon co MA transfe transfer. e address (ompleted ompletion r is

Figure 4.14 DTCTn Register Format (1/2)



Bit position	Bit name		Function					
5 4	DACM1 DACM0	DMA transfer destination address counting direction These bits specify the direction in which the transfer destination addre channel n is to be counted.						
		DACM1	DACM0	Counting direction				
		0	0	Incremented				
		0	1	Decremented				
		1	0	Fixed				
		1	1	Setting prohibited				
		This bit specifies the output timing for the DMAAK[0:5] and DMATC[0:5] output pins. 0: Read cycle 1: Write cycle The DSM bit is provided only for the DTCD0 to DTCD5 registers. The DTCD6 DTCD15 registers do not have this bit.						
Ca	(D gu 2. Th are	TSn.DTSnDT aranteed.	E bit = 1) annot be hibited sta					

Figure 4.15 DTCTn Register Format (2/2)

Setting examples

DTCT0 = 0x1000; /* 8bit data size;donot clear DTE; increment at tranfer source; increment at tranfer destination; output at read cycle */	
DTCT1 = 0x3000; /* 16bit data size;donot clear DTE; increment at tranfer source; increment at tranfer destination; output at read cycle */	



4.2.9 DMA Transfer Request Select Register (DTRSn)

This register specifies assignment of a DMA transfer request. A software DMA transfer request or a hardware DMA transfer request can be selected as a DMA transfer request.

	Access	This r	egister	can b	e read o	r written i	n 16-bit	units.			
A	DTRS DTRS DTRS DTRS	This register can be read or written in 16-bit units. DTRS15: FFFF 7660 _H , DTRS14: FFFF 7630 _H , DTRS13: FFFF 7600 _H , DTRS12: FFFF 75D0 _H , DTRS11: FFFF 75A0 _H , DTRS10: FFFF 7570 _H , DTRS9: FFFF 7540 _H , DTRS8: FFFF 7510 _H , DTRS7: FFFF 7460 _H , DTRS6: FFFF 7430 _H , DTRS5: FFFF 7400 _H , DTRS4: FFFF 73D0 _H , DTRS3: FFFF 73A0 _H , DTRS2: FFFF 7370 _H , DTRS1: FFFF 7340 _H , DTRS0: FFFF 7310 _H									
Initia	al Value	0000	н								
		15	5	14	13	12	1	1	10	9	8
		0		0	0	0	0)	0	0	0
		R	1	R	R	R	F	1	R	R	R
		7		6	5	4		3	2	1	0
		0		0	0	0	DT	R3	DTR2	DTR1	DTRo
		R		R	R	R	. R/	W	R/W	R/W	R/W
Tabl Bit position 3:0	e 10-10 Bit na DTR3 to	ime	DMA tra	ansfer i		ssignment					
	DTRo		These b	its spe	cify assi	gnment of	a DMA tr	ansfer	r request t	o channel r	1.
			DTR	3 [DTR2	DTR1	DTRo		DMA tra	nsfer requ	est
			0		0	0	0	Soft	ware DMA	transfer re	quest
			0		0	0	1	Hardware DMA transfer reques		equest	
			Other than above Setting prohib						ing prohib	ited	
L	autions	1. Wr				nibited wh			sfer is ena		

Figure 4.16 DTRSn Register Format

Setting examples

DTRS0 = 0x0000;	/* software transfer request */	
DTRS1 = 0x0001;	/* hardware transfer request */	



4.2.10 DTFR Control Register (DTFRn)

This register enables or disables the operation of the DMA source selector of channel n and selects the transfer source.

A	Access	This r	This register can be read or written in 16-bit units.									
A	ddress	DTFR DTFR DTFR DTFR	DTFR0: FFFF 7B00 _H , DTFR1: FFFF 7B02 _H , DTFR2: FFFF 7B04 _H , DTFR3: FFFF 7B06 _H , DTFR4: FFFF 7B08 _H , DTFR5: FFFF 7B0A _H , DTFR6: FFFF7B0C _H , DTFR7: FFFF 7B0E _H , DTFR8: FFFF 7B10 _H , DTFR9: FFFF 7B12 _H , DTFR10: FFFF 7B14 _H , DTFR11: FFFF 7B16 _H , DTFR12: FFFF 7B18 _H , DTFR13: FFFF 7B1A _H , DTFR14: FFFF 7B1C _H , DTFR15: FFFF 7B1E _H									
Initia	l Value	0000 _F	H									
		15	i i	14	13	12	11	10	9	8		
		REQEN		0	0	0	0	0	0	0		
	F		N	R	R	R	R	R	R	R		
				6	5	4	3	2	1	0		
		0					IFCn6-0					
		R		R/W	R/W	R/W	R/W	R/W	R/W	R/W		
Table	9 10-29	DTFR	In re	gister co	ntents							
Bit position	Bit na	me				F	unction					
15	REQEN		This bit enables or disables operation of the DMA source selector of channel n. 1: Enables operation of source selector 0: Stops operation of source selector. Does not issue DMA transfer request (DMARQ). The settings of IFCn6 to IFCn0 are valid. Requests are always sampled.									
6:0	IFCn6 to IFCn0					sfer source. in <i>Table 10</i>	-	tart source	s (0 to 63)"			

Figure 4.17 DTFRn Register Format

Setting example

DTFR0 = 0x0000;	/* software transfer request */
DTFR1 = 0x8020;	/* set hardware transfer request of dmac1 is taua0i0*/



DTFRn.IFCn[6:0]	Interrupt to start DMA
0	INTPO
1	INTP1
2	INTP2
3	INTP3
4	INTP4
5	INTP5
6	INTP6
7	INTP7
8	INTP8
9	INTP9
10	INTP10
11	INTP11
12	INTP12
13	INTP13
14	INTP14
15	INTP15
16	INTP16
17	INTP17
18	INTP18
19	INTP19
20	INTP20
21	INTP21
22	INTP22
23	INTP23
24	INTP24
25	INTP25
26	INTP26
27	INTP27
28	INTADCA0I0
29	INTADCA0I1
30	INTADCA012
31	INTADCA0ILLT

DTFRn.IFCn[6:0]	Interrupt to start DMA
32	INTTAUA0I0
33	INTTAUA011
34	INTTAUA012
35	INTTAUA0I3
36	INTTAUA0I4
37	INTTAUA015
38	INTTAUA016
39	INTTAUA017
40	INTTAUA018
41	INTTAUA019
42	INTTAUA0I10
43	INTTAUA0I11
44	INTTAUA0I12
45	INTTAUA0I13
46	INTTAUA0I14
47	INTTAUA0I15
48	INTTAUA110
49	INTTAUA111
50	INTTAUA112
51	INTTAUA113
52	INTTAUA114
53	INTTAUA115
54	INTTAUA116
55	INTTAUA117
56	INTTAUA118
57	INTTAUA119
58	INTTAUA1110
59	INTTAUA1111
60	INTTAUA1112
61	INTTAUA1113
62	INTTAUA1114
63	INTTAUA1115



DTFRn.IFCn[6:0]	Interrupt to start DM/
64	INTTAUA2I2
65	INTTAUA2I3
66	INTTAUA2I4
67	INTTAUA215
68	INTTAUA3I0
69	INTTAUA3I1
70	INTTAUA3I2
71	INTTAUA3I3
72	INTTAUA3I4
73	INTTAUA315
74	INTTAUA3I6
75	INTTAUA3I7
76	INTTAUA3I8
77	INTTAUA319
78	INTTAUA3I10
79	INTTAUA3I11
80	INTTAUA3I12
81	INTTAUA3I13
82	INTTAUA3I14
83	INTTAUA3I15
84	INTTAUJOIO
85	INTTAUJ011
86	INTTAUJ012
87	INTTAUJ0I3
88	INTENCA0IOV
89	INTENCA0IUD
90	INTENCA0I0
91	INTENCA011
92	INTENCA0IEC
93	INTENCA1OV
94	INTENCAIIUD
95	INTENCA1I0

Table 4.2 DMA Start Sources (2/2)

Interrupt to start DMA
INTENCA111
INTENCALIEC
INTTAPAOIPEKO
INTTAPAOIVLYO
INTTAPA2ADOUT0
INTTAPA0ADOUT0
INTTAPA0ADOUT1
INTTAPA1IPEK0
INTTAPA1IVLY0
INTTAPA3ADOUT0
INTTAPA1ADOUT0
INTTAPA1ADOUT1
INTCSIHOIR
INTCSIHOIC
INTCSIHIIR
INTCSIH1IC
INTCSIH2IR
INTCSIH2IC
INTCSIH3IR
INTCSIH3IC
INTCSIG0IR
INTCSIG0IC
INTCSIG1IR
INTCSIG1IC
INTCSIG2IR
INTCSIG2IC
INTCSIG3IR
INTCSIG3IC
INTCSIG4IR
INTCSIG4IC
INTCSIGSIR
INTCSIGSIC



4.3 Function Specifications

This section describes the specifications for the functions that are used by the sample program.

4.3.1 Main Processing (main.c)

[Function Name]	main ()
[Function]	Calls necessary initialization functions before entering an infinite loop.
[Arguments]	None
[Return Value]	None
[Startup Method]	Enters the main function after hardware initialization.
[SFRs Used]	DTS0SR, TAUA0TS
[Calling Function]	None
[Variables]	None
[File name]	main.c
[Notes]	None

4.3.2 Software Initialization Processing (initial.c)

[Function Name] [Function] [Arguments] [Return Value] [Startup Method] [SFRs Used] [Calling Function] [Variables] [File Name]	port_initial() Sets up ports and their mode. None Call PFCE0, PFC0, PMC0, PM0, PFCE13, PFC13, PMC13, PM13 main() None initial.c
[Notes]	None

[Function Name]	cg_initial()
[Function]	Initializes the special clock frequency control register.
[Arguments]	None
[Return Value]	None
[Startup Method]	Call
[SFRs Used]	SFRCTL3
[Calling Function]	main()
[Variables]	None
[File Name]	initial.c
[Notes]	None
• •	None



DMA Control

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[Function Name]	hbus_initial()
[Function]	Initializes the AHB bus.
[Arguments]	None
[Return Value]	None
[Startup Method]	Call
[SFRs Used]	ETARCFG0, ETARADRS0, ETARMASK0
[Calling Function]	main()
[Variables]	None
[File Name]	initial.c
[Notes]	None

[Function Name] [Function] [Arguments] [Return Value] [Startup Method] [SFRs Used] [Calling Function] [Variables] [File Name]	board_initial() Sets up the initial state of the LEDs. None Call P13 main() None initial.c
[Notes]	None

[Function Name]	ram_initial()
[Function]	Sets up the initial state of the internal RAM.
[Arguments]	None
[Return Value]	None
[Startup Method]	Call
[SFRs Used]	None
[Calling Function]	main()
[Variables]	DMA_source, DMA_IO
[File Name]	initial.c
[Notes]	None

4.3.3 DMA Control Processing (dma_control.c)

[Function Name]	dma0_initial()
[Function]	Sets up the operation of the DMA.
[Arguments]	None
[Return Value]	None
[Startup Method]	Call
[SFRs Used]	ICDMA0, ICDMACT0, DTS0, DSA0, DDA0, DSC0, DDC0, DTC0, DTCC0, DTCT0,
	DTRS0
[Calling Function]	main()
[Variables]	None
[File Name]	dma_control.c
[Notes]	None



DMA Control

V850E2/MN4

[Function Name] [Function]	dma1_initial() Sets up the operation of the ADC.
[Arguments]	None
[Return Value]	None
[Startup Method]	Call
[SFRs Used]	ICDMA1, ICDMACT1, DTS1, DSA1, DDA1, DSC1, DDC1, DTC1, DTCT1, DTRS1, DTFR1
[Calling Function]	main()
[Variables]	None
[File Name]	dma_control.c
[Notes]	None

4.3.4 Interrupt Processing (interrupt.c)

[Function Name]	int_dma1()
[Function]	Processes DMA transfer end interrupt.
[Arguments]	None
[Return Value]	None
[Startup Method]	Request INTDMA1 is present in an unmasked state.
[SFRs Used]	DTS1TC, P13
[Calling Function]	None
[Variables]	None
[File Name]	interrupt.c
[Notes]	None

[Function Name]	int_dmact0()
[Function]	Processes DMA transfer count match interrupt.
[Arguments]	None
[Return Value]	None
[Startup Method]	Request INTDMACT0 is present in an unmasked state.
[SFRs Used]	P13
[Calling Function]	None
[Variables]	None
[File Name]	interrupt.c
[Notes]	None



4.3.5 Timer Control Processing (taua0_control.c)

[Function Name] [Function] [Arguments] [Return Value] [Startup Method] [SFRs Used]	taua0_initial() Sets up the inverter function so that INTTAUAOIO becomes the trigger for DMA1. None Call TAUA0TPS, TAUA0BRS, TAUA0CMOR0, TAUA0CMUR0, TAUA0CDR0, TAUA0TOE, TAUA0TOM, TAUA0COC, TAUA0TOL, TAUA0TDE, TAUA0TDM, TAUA0TDL, TAUA0TRE, TAUA0TRO, TAUA0TRC, TAUA0TME, TAUA0RDE, TAUA0RDS, TAUA0RDM, TAUA0RDC
[Calling Function]	main()
[Variables]	None
[File Name]	taua0_control.c
[Notes]	None



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Revision Record

		Description		
Rev.	Date	Page	Summary	
1.00	Jan 30, 2012	_	First edition issued	

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

- 1. Handling of Unused Pins
- Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.
 - The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.
- 2. Processing at Power-on

The state of the product is undefined at the moment when power is supplied.

 The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

- 3. Prohibition of Access to Reserved Addresses
 - Access to reserved addresses is prohibited.

The reserved addresses are provided for the possible future expansion of functions. Do not access
these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

- When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.
- 5. Differences between Products Before changing from one product to another, i.e. to one with a different type number, confirm that the change will not lead to problems.
 - The characteristics of MPU/MCU in the same group but having different type numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different type numbers, implement a system-evaluation test for each of the products.

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