V850ES/JF3-L, RX231 Group

V850ES/JF3-L to RX231 Migration Guide

Introduction

This application note describes key points to consider when migrating from the V850ES/JF3-L to the RX231 Group, as well as points of difference between the two groups. For detailed information on the various functions, refer to the latest User's Manual: Hardware of each product.

The descriptions in this document use the specifications of the μPD70F3736 as representative of the V850ES/JF3-L. Other V850ES/JF3-L products have somewhat different specifications for memory capacity, but their functions are equivalent to those of the μPD70F3736. Therefore this document applies to them as well. In addition, the specifications of the R5F52318A (chip version A) are used as representative of the RX231 Group.

Note that the RX231 Group supports use of a variety of drivers and middleware (Firmware Integration Technology) and the driver generator tool (included with Smart Configurator), which helps to reduce the software development burden.

Contents

1. Overview

1.1 Product Lineup

Table 1.1 lists the product lineup (code sizes and pin counts) of the V850ES/JF3-L and RX231 Group.

Table 1.1 Code Sizes and Pin Counts of V850ES/JF3-L and RX231 Group Products

V850ES/JF3-L		RX231	
Code Flash/RAM	**Pin Count**	**Code Flash/RAM**	**Pin Count**
128 KB/8 KB	80 pins	128 KB/32 KB	48, 64, or 100 pins
256 KB/16 KB	80 pins	256 KB/32 KB	48, 64, or 100 pins
—	—	384 KB/64 KB	48, 64, or 100 pins
—	—	512 KB/64 KB	48, 64, or 100 pins

1.2 Substitutable and Non-substitutable Functions

Table 1.2 lists which functions of the V850ES/JF3-L are substitutable with functions on the RX231 Group and which functions are not substitutable.

Table 1.2 Substitutable and Non-substitutable Functions

Function on V850ES/JF3-L	Substitutable on RX231 Group?
Port functions	Yes
External bus control functions	Yes However, arbitration of bus mastership by the bus hold function is not supported.
Clock generator functions	Yes
Timer functions (TMP and TMQ)	Can be implemented using the multi-function timer pulse unit (MTU2a) or 16-bit timer pulse unit (TPUa). However, some functionality requires utilization of CPU interrupts.
16-bit interval timer M (TMM)	Can be implemented using the compare match timer (CMT).
Watch timer functions	Can be implemented using the realtime clock (RTCe).
Watchdog timer 2 functions	Can be implemented using the watchdog timer (WDTA) or independent watchdog timer (IWDTa).
Real-time output function (RTO)	Can be reproduced using the event link controller (ELC) and timer functions of the user's choice. However, some functionality requires utilization of CPU interrupts.
A/D converter	Can be implemented using the 12-bit A/D converter (S12ADE).
D/A converter	Can be implemented using the 12-bit D/A converter (R12DAA).
Asynchronous serial interface A (UARTA)	Can be implemented using the serial communications interface (SCIg or SCIh).
3-wire variable-length serial I/O (CSIB)	Can be implemented using the serial peripheral interface (RSPIa) or serial communications interface (SCIg or SCIh).
I^2C bus	Can be implemented using the serial communications interface (SCIg or SCIh) or I^2C-bus interface (RIICa).
DMA functions (DMA controller)	Yes
Interrupt/exception processing function	Yes However, specifications dependent on external interrupts or peripheral modules are excluded.
Standby function	Yes
Clock monitor	Can be implemented using oscillation stop detection function.
Low-voltage detector (LVI)	Can be implemented using voltage detection circuit (LVDAb).
CRC function	Yes

2. On-Chip Functions

2.1 CPU Functions

2.1.1 Comparative Specifications

Table 2.1 lists comparative specifications of the CPU functions of the V850ES/JF3-L and RX231 Group.

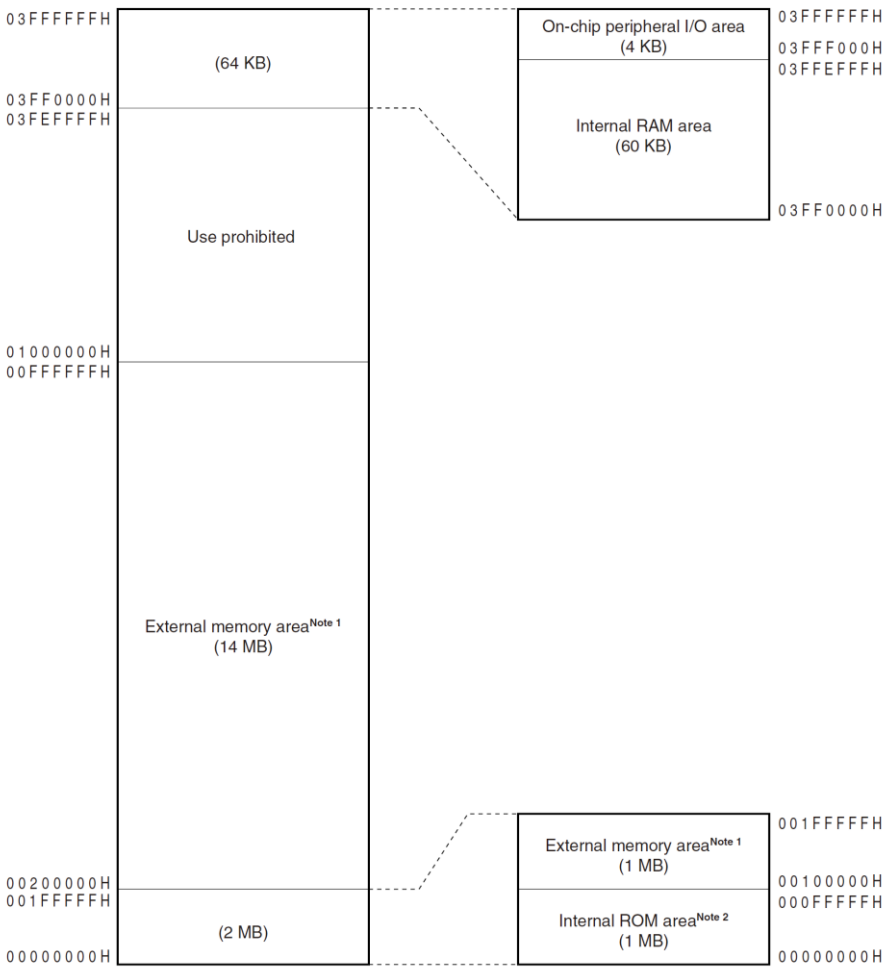
Table 2.1 CPU Functions of V850ES/JF3-L and RX231 Group

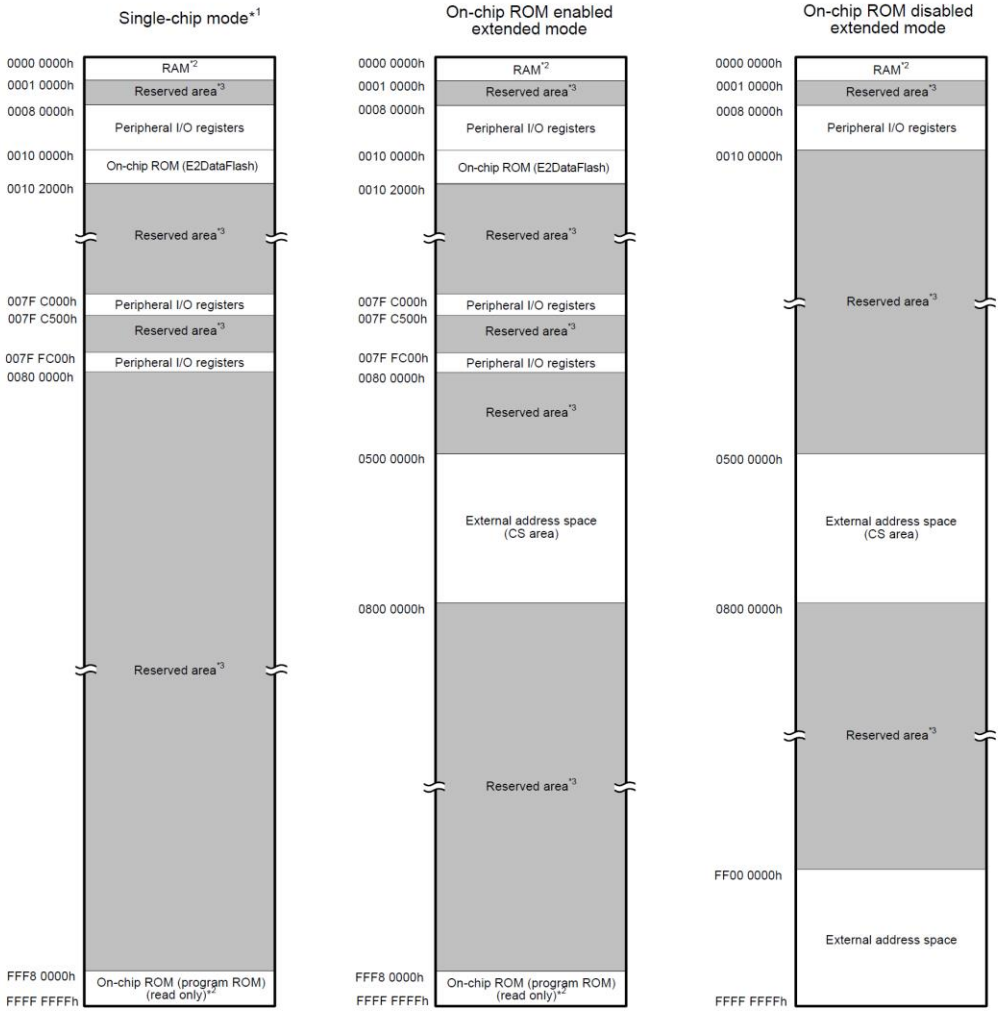
Item	V850ES/JF3-L	RX231
Max. operating frequency	20 MHz	54 MHz

2.1.2 Memory Map

Table 2.2 shows memory maps of the V850ES/JF3-L and RX231 Group.

Table 2.2 Memory Maps of V850ES/JF3-L and RX231 Group

Item	V850ES/JF3-L
Memory map	 **Notes 1.** The V850ES/JF3-L has 18 address pins, so the external memory area appears as a repeated 256 KB image. **2.** Fetch access and read access to addresses 00000000H to 000FFFFFH is made to the internal ROM area. However, data write access to these addresses is made to the external memory area.

Item	RX231
Memory map	

Note 1. The address space in boot mode and USB boot mode is the same as the address space in single-chip mode.
Note 2. The capacity of ROM/RAM differs depending on the products.

ROM (bytes)		RAM (bytes)	
Capacity	**Address**	**Capacity**	**Address**
512 Kbytes	FFF8 0000h to FFFF FFFFh	64 Kbytes	0000 0000h to 0000 FFFFh
384 Kbytes	FFFA 0000h to FFFF FFFFh		
256 Kbytes	FFFC 0000h to FFFF FFFFh	32 Kbytes	0000 0000h to 0000 7FFFh
128 Kbytes	FFFE 0000h to FFFF FFFFh		

Note: See Table 1.3 and Table 1.4 List of Products, for the product type name.

Note 3. Reserved areas should not be accessed.

2.2 Port Functions

2.2.1 Comparative Specifications

Table 2.3 lists correspondences between the specifications of I/O ports on the RX231 Group and port functions on the V850ES/JF3-L.

Table 2.3 Substitutability of Port Functions

Item	V850ES/JF3-L	RX231
CMOS output and N-ch open-drain output	Yes	Yes
Integrated pull-up/pull-down function	Yes (pull-down)	Yes (pull-up)
5 V tolerant input	Yes	Yes

2.2.2 Usage Note

2.2.2.1 Unimplemented Ports

Due to different pin counts among products in the RX231 Group, some ports are not implemented on some products. It is therefore necessary to make appropriate settings for unimplemented ports, as described in 21.4, Initialization of the Port Direction Register (PDR), in RX230 Group, RX231 Group User's Manual: Hardware.

This corresponds to setting the port n mode registers (PMn) on the V850ES/JF3-L. For details of port n mode register (PMn) settings, refer to chapter 4, PORT FUNCTIONS, in V850ES/JF3-L User's Manual: Hardware.

2.3 External Bus Control Functions

2.3.1 Comparative Specifications

Table 2.4 lists correspondences between the specifications of the external bus interface function on the V850ES/JF3-L and the external bus function on the RX231 Group. Table 2.5 is a comparative listing of pins used by these external bus control functions.

Table 2.4 External Bus Interface Function Correspondences

Item	V850ES/JF3-L External Bus Interface Function	RX231 External Bus
Bus width	8-bit/16-bit	8-bit/16-bit
Bus space	4 blocks (block size: 2 MB to 8 MB)	4 blocks (block size: 16 MB)
Wait functions	Data wait	Possible using cycle wait, assert wait, and data output wait settings.*1
	Address setup wait	Possible using CS assert wait setting.
	Address hold wait	Possible using address cycle wait setting.
	External wait using pin	Possible using WAIT# pin.
Bus arbitration in multi-processor configuration	Bus mastership arbitration using bus hold function	Not supported.
Bus modes	Multiplex bus mode	Multiplex bus mode and separate bus mode

Note: 1. Read operation: An equivalent setting is possible using the cycle wait setting (CSRWAIT) and RD assert wait (RDON).
Write operation: An equivalent setting is possible using the cycle wait setting (CSRWAIT) and assert wait (WDON) or data output wait (WDON).

Table 2.5 Comparative Listing of External Bus Interface Function–Related Pins

V850ES/JF3-L			RX231*1		
Pin Name	**I/O**	**Function**	**Pin Name**	**I/O**	**Function**
AD0-AD15	Input/ output	Address/data bus	A15/D15-A0/ D0	Input/ output	Address/data bus (multiplex bus mode)
A16, A17	Input/ output	Address bus	A23-A9	Output	Address bus
$\overline{\text{WAIT}}$	Input	External wait control	WAIT#	Input	External wait control
CLKOUT	Output	Internal system clock output	BCLK	Output	External bus clock
$\overline{\text{WR0}}$ $\overline{\text{WR1}}$	Output	Write strobe	WR1#, WR0#/WR#	Output	Write strobe
$\overline{\text{RD}}$	Output	Read strobe	RD#	Output	Read strobe
ASTB	Output	Address strobe	ALE	Output	Address latch enable (multiplex bus mode)
$\overline{\text{HLDRQ}}$	Input	Bus hold control	—	—	—
$\overline{\text{HLDAK}}$	Output		—	—	—

Note: 1. The external bus function is supported only on 100-pin package versions of the RX231 Group.

2.4 Clock Generator

2.4.1 Comparative Specifications

Table 2.6 lists correspondences between the specifications of the clock generator on the V850ES/JF3-L and the clock generation circuit on the RX231 Group.

Table 2.6 Clock Generator Function Correspondences

Item	V850ES/JF3-L Clock Generator	RX231 Clock Generation Circuit
CPU clock source	Selectable among the following four: • Main clock • PLL clock (×4 fixed) • Subclock • Internal oscillation clock	Selectable among the following five: • Main clock (1 MHz to 20 MHz) (Selectable between resonator and external clock.) • PLL clock (×4 to ×13.5, ×1/1, ×1/2, or ×1/4) • Subclock (32.768 kHz)*1 • High-speed on-chip oscillator (HOCO) (selectable between 54 MHz and 32 MHz) • Low-speed on-chip oscillator (LOCO) (4 MHz)
Operating frequency (max.)	Stipulations by function • CPU clock frequency: f_{CPU}: 20 MHz (max.) • Internal system clock frequency: f_{CLK}: 20 MHz (max.) • Peripheral clock frequency: 20 MHz (max.) • Timer M clock: 20 MHz (max.) • Watch timer clock: 32.768 kHz • Watchdog timer 2 clock: Approx. 39 kHz (max.) • Internal oscillator: 220 kHz	Different clock frequencies are generated according to the function. • ICLK: 54 MHz (max.) • PCLKA: 54 MHz (max.) • PCLKB: 32 MHz (max.) • PCLKD: 54 MHz (max.) • FCLK: 1 MHz to 32 MHz (for programming and erasing the ROM and E2 DataFlash) 32 MHz (max.) (for reading from the E2 DataFlash) • BCLK: 32 MHz (max.) • BCLK pin output: 16 MHz (max.) • UCLK: 48 MHz (max.) • CACCLK: Same frequency as each oscillator • RTCSCLK: 32.768 kHz • IWDTCLK: 15 kHz • CANMCLK: 20 MHz (max.)*2 • SSISCK: 20 MHz (max.) • LPTCLK: Same frequency as selected oscillator

Notes: 1. The subclock pin is not implemented on 48-pin products.
2. CANMCLK is not implemented on chip version C.

2.4.2 Usage Notes

2.4.2.1 Usage Note Regarding Clock Generation Circuit

On the RX231 Group restrictions apply regarding the frequencies of the system clock (ICLK) and of the clocks supplied to the peripheral modules (such as PCLK). For details, refer to 9.8.1, Notes on Clock Generation Circuit, RX231 Group User's Manual: Hardware.

2.4.2.2 Oscillation Stop Detection Function

The RX231 Group has a function that detects when the main clock oscillator stops operating and supplies the low-speed clock output from LOCO as the system clock source instead of the main clock. For details, refer to 9.5, Oscillation Stop Detection Function, in RX230 Group, RX231 Group User's Manual: Hardware.

2.4.2.3 Sub-clock Initialization

On the RX231 Group it is necessary to initialize the sub-clock control circuit after a cold start, regardless of whether or not the sub-clock is in use. For details, refer to 9.8.5, Notes on Sub-Clock, in RX230 Group, RX231 Group User's Manual: Hardware.

2.5 Timer Functions (TMP and TMQ)

2.5.1 Units

Table 2.7 lists the timer function units on the V850ES/JF3-L and RX231 Group.

Table 2.7 Timer Functions on V850ES/JF3-L and RX231 Group

Item	V850ES/JF3-L	RX231
Multi-function timer/counter integrated modules	• 16-bit timer/event counter P (TMP) • 16-bit timer/event counter Q (TMQ)	• Multi-function timer pulse unit 2 (MTU2a) • 16-bit timer pulse unit (TPUa)

2.5.2 Comparative Specifications

Table 2.8 lists correspondences between the specifications of the timer functions (16-bit timer/event counter P and 16-bit timer/event counter Q) on the V850ES/JF3-L and the timer functions (MTU2a and TPUa) on the RX231 Group.

Table 2.8 Timer Function Correspondences

	V850ES/JF3-L	RX231	
Item	**TMP, TMQ**	**MTU2a**	**TPUa**
Timer counters	5 channels TMP01: 4 channels TMQ: 1 channel	8 channels (1 channel each for MTU0 to MTU4, 3 channels for MTU5)	6 channels (1 channel each for TPU0 to TPU5)
Modes	Interval timer Interrupt generation and square wave output at user-defined period Up to 5 channels (TMP: 4 channels, TMQ: 1 channel)	Possible using normal mode on MTU0 to MTU4. • Count timer: 5 channels (MTU0 to MTU4) • Output pins: 4 each for MTU0, MTU3, and MTU4, 2 each for MTU1 and MUT2	Possible using normal mode on TPU0 to TPU5. Output pins: 4 each for TPU0 and TPU3, 2 each for TPU1, TPU2, TPU4, and TPU5
	External event count Counts valid edges of external event count input and generates an interrupt each time the user-defined count is reached. Up to 5 channels (TMP: 4 channels, TMQ: 1 channel)	Possible on up to 5 channels using MTU0 to MTU4, which support external clock input. Input pins: 1 each	Possible on up to 6 channels using TPU0 to TPU5, which support external clock input. Input pins: 1 each
	External trigger pulse output Count operation and PWM waveform output at occurrence of external trigger Up to 5 outputs (TMP: 4 channels, TMQ: 1 channel)	No equivalent functionality is implemented in hardware.*1 However, equivalent operation can be achieved using PWM mode and external input interrupts on MTU0 to MTU4. Waveform outputs: Up to 12 PWM outputs are supported by combining PWM modes 1 and 2.	No equivalent functionality is implemented in hardware.*1 However, equivalent operation can be achieved using PWM mode and external input interrupts on TPU0 to TPU5. Waveform outputs: Up to 15 PWM outputs are supported.
	One-shot pulse output Count operation and one-shot pulse output at occurrence of external trigger Up to 5 outputs (TMP: 4 channels, TMQ: 1 channel)		

Item	V850ES/JF3-L	RX231	
	TMP, TMQ	**MTU2a**	**TPUa**
Modes	PWM output Up to 5 outputs (TMP: 4 channels, TMQ: 1 channel)	Up to 12 PWM outputs are supported by combining PWM modes 1 and 2.	Up to 15 PWM outputs are supported.
	Free running timer Max. 5-channel operation (TMP: 4 channels, TMQ: 1 channel)	Normal mode (free running counter operation) Up to 5 channels 8 count resources (1 each for MTU0 to MTU4, 3 for MTU5)	Normal mode (free running counter operation) Up to 6 channels (1 each for TPU0 to TPU5)
	Pulse width measurement Measurement on up to 5 channels (TMP: 4 channels, TMQ: 1 channel)	Possible using either of the following methods: • Using input capture on each channel (1 each for MTU0 to MTU4, 3 for MTU5) • Using the pulse width measurement function on MTU5 Supports width measurement on up to 3 external pulse inputs (using MTU5).	Using input capture on each channel Input pins: 4 each for TPU0 and TPU3, 2 each for TPU1, TPU2, TPU4, and TPU5

Note: 1. Sample programs are available to demonstrate how to reproduce in software external trigger mode and one-shot pulse mode, which are not supported in hardware on the RX231. For details, refer to section 3, Sample Programs.

2.6 16-Bit Interval Timer M (TMM)

2.6.1 Comparative Specifications

Table 2.9 lists correspondences between the specifications of 16-bit interval timer M (TMM) on the V850ES/JF3-L and the compare match timer (CMT) on the RX231 Group.

Table 2.9 16-Bit Interval Timer Function Correspondences

Item	V850ES/JF3-L TMM	RX231 CMT
Number of channels	1 channel	4 channels
Counter bits	16	16
Selectable clock frequency division ratios	8 ratios A ratio of f_{XX}, $f_{XX}/2$, $f_{XX}/4$, $f_{XX}/64$, $f_{XX}/512$, INTWT, fR/8, or FXT can be selected for each channel.	4 ratios A ratio of PCLK/8, PCLK/32, PCLK/128, PCLK/512 can be selected for each channel.

2.6.2 Usage Note

2.6.2.1 Initializing the Timer Counter

When operation of 16-bit interval timer M is stopped on the V850ES/JF3-L, the counter is reset out of sync with the count clock. It is not possible to read or write to the 16-bit counter. On the RX231 Group, the compare match timer retains its value when counting is stopped. The counter register of the compare match timer can be reset to its initial value freely.

2.7 Watch Timer Functions

2.7.1 Comparative Specifications

Table 2.10 lists correspondences between the specifications of the watch timer functions on the V850ES/JF3-L and the realtime clock (RTCe) on the RX231 Group.

Table 2.10 Watch Timer Function Correspondences

Item	V850ES/JF3-L Watch Timer Function	RX231 Realtime Clock (RTCe)*1
Modes	Watch timer mode Reference time period (interrupt output at intervals of 0.5 or 0.25 seconds)	Periodic interrupts supported. Interrupt period 2 seconds, 1 second, 1/2 second, 1/4 second, 1/8 second, 1/16 second, 1/32 second, 1/64 second, 1/128 second, or 1/256 second
	Interval timer mode	
Difference between watch timer mode and calendar count mode	Operates as interval timer exclusively for reference time period.	Counts time information. Example: hh:mm:ss, etc.
Count clocks	Subclock, main clock	Subclock
Interrupts	Watch timer interrupt, interval timer interrupt	Periodic interrupt, alarm interrupt, carry interrupt

Note: 1. Not supported on 48-pin package products.

2.7.2 Usage Note

2.7.2.1 Initializing the RTC

On the RX231 Group the realtime clock's internal registers are not initialized by a reset, so it is necessary to initialize them regardless of whether or not the realtime clock will be used. For details, refer to 28.3, Operation, and 28.6.7, Initialization Procedure When the Realtime Clock is Not to be Used, in RX230 Group, RX231 Group User's Manual: Hardware.

Initialization may be omitted only in cases where no sub-clock is implemented.

2.8 Watchdog Timer 2 Functions

2.8.1 Units

Table 2.11 lists the watchdog timer functions on the V850ES/JF3-L and the RX231 Group.

Table 2.11 Watchdog Timer Functions on V850ES/JF3-L and RX231 Group

Item	V850ES/JF3-L	RX231
Watchdog timer functions	Watchdog timer 2 functions	• Watchdog timer (WDTA) • Independent watchdog timer (IWDTa)

2.8.2 Comparative Specifications

Table 2.12 lists correspondences between the specifications of the watchdog timer 2 functions on the V850ES/JF3-L and the WDTA and IWDTa functions on the RX231 Group.

Table 2.12 Watchdog Timer Function Correspondences

	V850ES/JF3-L	RX231	
Item	Watchdog Timer 2	WDTA	IWDTa
Counter bit length	16 bits	14 bits	14 bits
Count clock sources	• Subclock • Main clock • Internal oscillation clock	Peripheral clock (PCLKB)	IWDT-dedicated clock (IWDTCLK) Generated by on-chip oscillator.
Overflow time selection	• Subclock $2^9/f_{XT}$ to $2^{16}/f_{XT}$ • Main clock $2^{18}/f_{xx}$ to $2^{25}/f_{xx}$ • Internal oscillation clock $2^{12}/f_R$ to $2^{19}/f_R$	Division ratio of 4 to 8,192	Division ratio of 1 to 256
Operating modes	Selectable between non-maskable interrupt request mode and reset mode.	Selectable between non-maskable interrupt request output and reset output.	Selectable between non-maskable interrupt request output and reset output.
Interrupt/reset generation source	Overflow interrupt	• Underflow interrupt • Refresh error	• Underflow interrupt • Refresh error

2.8.3 Usage Note

2.8.3.1 Count Operation

On the V850ES/JF3-L watchdog timer 2 counts up, and on the RX231 Group the watchdog timer and independent watchdog timer count down.

2.8.3.2 Starting Counting

On the RX231 Group there are two ways to start count operation by the watchdog timer or independent watchdog timer: register start mode and auto-start mode.

2.8.3.3 Settings when Not Using Watchdog Timer

On the V850ES/JF3-L watchdog timer 2 automatically starts in reset mode after a reset is canceled. If the watchdog timer will not be used, it is necessary to first clear watchdog timer 2 and then to stop it within the interval duration. On the RX231 no special settings are necessary when not using the watchdog timer or independent watchdog timer.

2.9 Real-Time Output Function (RTO)

The RX231 Group does not have functionality corresponding to the real-time output function (RTO). However, it is possible to produce waveform output equivalent to that of the real-time output function by using the port group output function of the event link controller (ELC) in combination with any timer function that can be linked to it, provided that the points to consider listed below do not pose a problem.

Points to consider

- Factors such as the difference between the operating clocks of the timer function and event link controller may prevent the output from switching according to the intended timing.
- If output switching does not occur according to the intended timing, try using the timer output function of multi-function timer pulse unit 2 (MTU2a) or the 16-bit timer pulse unit (TPUa).

2.9.1 Comparative Specifications

Table 2.13 lists correspondences between the real-time output function on the V850ES/JF3-L and the port group output function of the event link controller on the RX231 Group.

Table 2.13 Real-Time Output Function Correspondences

	V850ES/JF3-L	**RX231**
Item	**RTO**	**ELC Port Group Output Function + Any Linkable Timer Function***1
Channels	2 channels	2 channels
Output pins	Up to 6 outputs 6 outputs on 1 channel or 4 + 2 outputs on 2 channels are supported.	Up to 16 outputs Up to 8 outputs are supported per channel.
Operation	Outputs preset data in the buffer register by hardware in synchronization with a timer interrupt.	Outputs preset data in the buffer register by hardware via a preset pin, using generation of a specified interrupt request as the trigger.

Note: 1. For timer modules that can be linked to the event link controller, refer to Table 20.2, Correspondence between the ELSRn Register and the Peripheral Modules, in RX230 Group, RX231 Group User's Manual: Hardware.

A sample program is provided that recreates in software the real-time output function, which is not implemented in hardware on the RX231 Group. For details, refer to section 3, Sample Programs.

2.10 A/D Converter

2.10.1 Comparative Specifications

Table 2.14 lists correspondences between the specifications of the A/D converter on the V850ES/JF3-L and the 12-bit A/D converter (S12ADE) on the RX231 Group.

Table 2.14 A/D Converter Function Correspondences

Item	V850ES/JF3-L A/D Converter	RX231 S12ADE
Analog inputs	8 channels	24 channels
Resolution	10 bits	12 bits
A/D conversion method	Successive approximation method	Successive approximation method
A/D conversion operating mode	Continuous select mode	Possible using continuous scan mode.
	Continuous scan mode	
	One-shot select mode	Possible using single scan mode.
	One-shot scan mode	
A/D conversion trigger mode	Software trigger	Software trigger
	Timer trigger	Possible by accepting a synchronous trigger (such as a trigger from an MTU timer function*1).
	External trigger	Possible using an asynchronous trigger (ADTRG0# pin).
External trigger edges	Falling edge, rising edge, both edges	Falling edge
Comparison of conversion results	Power-fail monitor function The A/D conversion result and a register setting value are compared, and an interrupt is generated when the maximum or minimum comparison condition is satisfied.	Can be implemented by using the compare function to compare results. However, no interrupt is generated, and only linkage with the event link function is available.
Conversion time	2.6 µs	0.83 µs
Interrupt sources/ DMA activation sources	A/D conversion end	Possible using scan end interrupt.

Note: 1. Specifically, the timer functions referred to are the following modules:
Multi-function timer pulse unit 2 (MTU2a)
16-bit timer pulse unit (TPUa)
Event link controller (ELC)

2.10.2 Usage Note

2.10.2.1 A/D Converter Operating Status

On the V850ES/JF3-L there are status flags that indicate whether conversion operation is in progress on the A/D converter. On the RX231 Group there are no status flags for the 12-bit A/D converter, but the operating status can be confirmed by checking the A/D conversion start bit in the A/D control register.

2.11 D/A Converter

2.11.1 Comparative Specifications

Table 2.15 lists correspondences between the specifications of the D/A converter on the V850ES/JF3-L and the 12-bit D/A converter (R12DAA) on the RX231 Group.

Table 2.15 D/A Converter Function Correspondences

Item	V850ES/JF3-L D/A Converter	RX231 R12DAA
Number of channels	1 channel	2 channels
Resolution	10 bits	12 bits
Conversion time	Settling time: 3 µs (max.) When AVREF1 = 2.7 V to 3.6 V and external load is 20 pF	Conversion time: 30 µs
Analog output voltage	AVREF1 × m/256 (m = 0 to 255; value set in DA0CS0 register)	Min: 0.35 V, max: AVCC0 − 0.47 The reference voltage is selectable among the following three patterns: • (AVCC0-AVSS0) × m/4096 • (Internal reference voltage − AVSS0) × m / 4096 • (VREFH-VREFL) × m/4096 (m = 0 to 4095; register value)
Operating modes	Normal mode (D/A conversion when register is overwritten)	Normal mode (D/A conversion when register is overwritten)
	D/A conversion when timer interrupt (INTTP2CC0 signal) occurs	Possible using timer interrupt and event link function*1 in combination.

Note: 1. For details of the event link function, refer to 20. Event Link Controller (ELC), in RX230 Group, RX231 Group User's Manual: Hardware.

2.12 Asynchronous Serial Interface A (UARTA)

2.12.1 Comparative Specifications

Table 2.16 lists correspondences between the specifications of asynchronous serial interface A (UARTA) on the V850ES/JF3-L and the asynchronous mode of the serial communications interface (SCIg and SCIh) on the RX231 Group.

Table 2.16 Asynchronous Serial Interface Function Correspondences

Item	V850ES/JF3-L UARTA	RX231 SCIg, SCIh (Asynchronous Mode)
Number of channels	3 channels	7 channels Individual channels can be put into the module stop state.
Transfer speed(max.)	625 kbps (fxx = 20 MHz)	3.75 Mbps (PCLKB = 30 MHz)
Full-duplex communications	Yes	Yes
Character length	Selectable between 7 and 8 bits.	Selectable between 7, 8, and 9 bits.
Stop bit	Selectable between 1 and 2 bits.	Selectable between 1 and 2 bits.
Parity	Selectable among odd parity, even parity, or 0 parity.	Selectable among odd parity, even parity, or no parity.
Data transfer order	Selectable between MSB- or LSB-first.	Selectable between MSB- or LSB-first.
Inverted data output	Yes	Yes
Noise filter	Noise filter circuit suppresses noise.	Possible to use digital filter to suppress noise. Possible to enable or disable filter using software.
Receive error detection	• Parity error • Overrun error • Framing error	• Parity error • Overrun error • Framing error
Interrupt sources	• Reception end/reception error • Transmission enable	• Receive data full • Transmit end • Receive error • Transmit data empty
DMA activation sources	• Reception end • Transmission enable	• Receive data full • Transmit data empty

2.12.2 Usage Note

2.12.2.1 0 Parity

On the V850ES/JF3-L it is possible to set the parity to 0 parity, but no setting corresponding to 0 parity exists on the RX231 Group.

2.13 3-Wire Variable-Length Serial I/O (CSIB)

2.13.1 Units

Table 2.17 lists the units of the 3-wire variable-length serial I/O functions on the V850ES/JF3-L and RX231 Group.

Table 2.17 3-Wire Variable-Length Serial I/O Functions on V850ES/JF3-L and RX231 Group

Item	V850ES/JF3-L	RX231
3-wire variable-length serial	3-wire variable-length serial I/O (CSIB)	• Serial peripheral interface (RSPIa) • Simple SPI mode/clock synchronous mode of serial communications interface (SCIg, SCIh)

2.13.2 Comparative Specifications

Table 2.18 lists correspondences between the specifications of the 3-wire variable-length serial I/O functions on the V850ES/JF3-L and the serial peripheral interface (RSPIa) and clock synchronous mode of the serial communications interface on the RX231 Group.

Table 2.18 3-Wire Variable-Length Serial I/O Function Correspondences

	V850ES/JF3-L	RX231	
Item	CSIB	RSPIa	SCIg and SCIh (Simple SPI Mode/ Clock Synchronous Mode)
Number of channels	3 channels	1 channel	7 channels
Communication clock frequency (max.)	Master/slave shared: 8 MHz	Master operation: 16 MHz Slave operation: 4 MHz (PCLKB = 32 MHz)	Master operation: 7.5 MHz Slave operation: 5 MHz (PCLKB = 30 MHz)
Operating modes	Master/slave	Master/slave	Master/slave
Serial clock and data phase switchable	Ability to switch serial clock and data phase	Ability to change phase and polarity of RSPCK	Ability to specify clock phase and polarity
Data length	8 bits to 16 bits	8 to 16, 20, 24, or 32 bits (specifiable in 1-bit units)	8 bits
Data transfer order	Switchable between MSB- and LSB-first.	Switchable between MSB- and LSB-first.	Switchable between MSB- and LSB-first.
Transmission/ reception mode	Single transfer mode (transmission, reception, or transmission/reception mode)	Single transfer operation possible.	Single transfer operation possible.
	Continuous transfer mode (transmission, reception, or transmission/reception mode)	Transmission and reception buffers are both double buffer configurations, making continuous transfer possible.	Transmission and reception buffers are both double buffer configurations, making continuous transfer possible.
Pins	• Serial data output • Serial data input • Serial clock I/O	• Master transmit data I/O • Slave transmit data I/O • Clock I/O • Slave-select I/O (SPI operation only)	• Clock I/O • Transmit data output • Receive data input • I/O for transmission/ reception/chip select input pin
Interrupt sources	• Consecutive transmission write enable • Reception end/reception error	• Receive buffer full • Transmit buffer empty • RSPI error • RSPI idle	• Transmission end • Transmit data empty • Receive data full • Reception error
DMA activation sources	• Consecutive transmission write enable • Reception end/reception error	• Receive buffer full • Transmit buffer empty	• Transmit data empty • Receive data full

2.14 I²C Bus

2.14.1 Units

Table 2.19 lists the I²C bus function units on the V850ES/JF3-L and RX231 Group.

Table 2.19 I²C Bus Function Units on V850ES/JF3-L and RX231 Group

Item	V850ES/JF3-L	RX231
I²C function	I²C bus	• I²C-bus interface (RIICa) • Simple I²C mode of serial communications interface (SCIg, SCIh)

2.14.2 Comparative Specifications

Table 2.20 lists correspondences between the specifications of the I²C bus functions on the V850ES/JF3-L and the I²C-bus interface and simple I²C mode of the serial communications interface on the RX231 Group.

Table 2.20 I²C Bus Function Correspondences

Item	V850ES/JF3-L	RX231	
	I²C Bus	**RIICa**	**Simple I²C Mode of SCIg and SCIh**
Number of channels	2 channels	1 channel	7 channels
Transfer rate	Standard mode: Up to 100 kbps High-speed mode: Up to 350 kbps	Standard mode: Up to 100 kbps Fast mode: Up to 400 kbps	Standard mode: Up to 100 kbps Fast mode: Up to 350 kbps
Communication format	I²C bus format	• I²C bus format • SMBus format	I²C bus format
Communication operation	• Multimaster support • Slave operation	• Multimaster support • Slave operation	Single master only
Digital filtering	Usable in high-speed mode only	The noise canceling width can be adjusted using software.	The noise canceling width can be adjusted using software.
Reduced power consumption	Operation stop mode	Can be implemented using module stop function.	Can be implemented using module stop function.

Item	V850ES/JF3-L	RX231	
	I²C Bus	**RIICa**	**Simple I²C Mode of SCIg and SCIh**
Interrupts	1 source • Fall of 8th or 9th clock pulse of INTIIC interrupt serial clock • Stop condition detection	4 sources • EEI interrupt Transfer error or transfer event occurrence Arbitration detection NACK detection Timeout detection Start condition (including restart condition) detection Stop condition detection • RXI interrupt Receive data full (including slave address match) • TXI interrupt Transmit data empty (including slave address match) • TEI interrupt Transmit end	3 sources • RXI interrupt ACK detection/reception • TXI interrupt NACK detection/ transmission • STI interrupt Completion of generation of start condition, restart condition, or stop condition
DMA activation sources	IICn transfer end	• Receive data full interrupt • Transmit data empty interrupt	• Receive interrupt • Transmit interrupt

2.15 DMA Functions (DMA Controller)

2.15.1 Comparative Specifications

Table 2.21 lists correspondences between the specifications of the direct memory access (DMA) controller (DMAC) on the V850ES/JF3-L and the DMA controller (DMACA) on the RX231 Group.

Table 2.21 DMA Controller Function Correspondences

Item	V850ES/JF3-L DMAC	RX231 DMACA
Number of channels	4 channels	4 channels
Transfer mode	Single transfer mode	Can be implemented using normal transfer mode. However, two-cycle transfers are not supported.
Transfer unit	8 or 16 bits	8, 16, or 32 bits
Max. transfer count	65,535 times	65,535 times
Transfer requests	On-chip peripheral function interrupts, external interrupt pins, software triggers	Peripheral module interrupts, external interrupt pins, software triggers
Transfer targets	On-chip peripheral I/O ↔ on-chip peripheral I/O On-chip peripheral I/O ↔ on-chip RAM On-chip peripheral I/O ↔ external memory On-chip RAM ↔ external memory External memory ↔ external memory	Transfers can be made to all non-reserved memory areas.
Address counting method	Increment, decrement, fixed	Increment, decrement, fixed, offset calculation*1
Interrupts	DMA transfer end interrupt	Transfer end interrupt, transfer escape end interrupt

Note: 1. The offset calculation setting is supported only on DMAC0.

2.16 Interrupt/Exception Processing Function

2.16.1 Comparative Specifications

Table 2.22 lists correspondences between the specifications of the interrupt and exception processing function on the V850ES/JF3-L and the interrupt controller (ICUb) and exception handling on the RX231 Group.

Table 2.22 Interrupt/Exception Handling Function Correspondences

Item	V850ES/JF3-L Interrupt/Exception Processing Function	RX231 ICUb/Exception Handling
Non-maskable interrupts	• Overflow of watchdog timer 2 • NMI pin interrupt	• NMI pin interrupt • Oscillation stop detection interrupt • WDTA underflow/refresh error • IWDTa underflow/refresh error • Voltage monitoring 1 interrupt • Voltage monitoring 2 interrupt • VBATT Voltage monitoring
Maskable interrupts	• External pin interrupts: 8 sources • On-chip peripheral interrupts	• External pin interrupts: 8 sources • Peripheral function interrupts • Software interrupt: 1 source
Priority control	8 levels	16 levels
External pin noise suppression	• Noise suppression circuit using analog delay: NMI pin, INTP0 to INTP7 pins • Digital noise suppression • Sampling clock Selectable among f_{XX}/64, f_{XX}/128, f_{XX}/256, f_{XX}/512, f_{XX}/1024, and f_{XT}	• Digital filter: NMI pin, IRQ0 to IRQ7 pins • Sampling cycles: 3 times • Sampling frequency: Selectable among PCLK, PCLK/8, PCLK/32, and PCLK/64. • Selectable between digital filter enabled and disabled.
External pin interrupt detection	• Edge detection Rising edge Falling edge Both edges • No edge detection	• Edge detection Rising edge (NMI, IRQ0 to IRQ7) Falling edge (NMI, IRQ0 to IRQ7) Both edges (IRQ0 to IRQ7) • Low-level detection (IRQ0 to IRQ7)
Software exceptions	TRAP1n instruction, TRAP0n instruction (dedicated vectors: 32 sources)	INT instruction, BRK instruction (unconditional trap: 16 sources)
Illegal opcode exceptions	Yes	Yes (undefined instruction exception)

2.16.2 Usage Note

2.16.2.1 Differences among Chip Versions

On the RX231 Group the specifications differ as follows according to the chip version:

- SDHI interrupts (vector numbers 40 to 43) are not implemented on chip versions A and C.
- RSCAN0 interrupts (vector numbers 52 to 56) are not implemented on chip version C.
- Security interrupts (vector numbers 111 to 113) are not implemented on chip versions A and C.

2.17 Standby Function

2.17.1 Comparative Specifications

Table 2.23 lists correspondences on the RX231 Group with the standby function on the V850ES/JF3-L, and Table 2.24 shows the operating status after transition to each mode.

Table 2.23 Standby Function Correspondences

Item	V850ES/JF3-L	RX231
HALT mode	Mode in which only the operating clock of the CPU is stopped < Cancellation sources > • Non-maskable interrupt request signal • Unmasked maskable interrupt request signal • Reset signal (reset triggered by RESET pin input, WDT2RES signal, low-voltage detector (LVI), or clock monitor (CLM))	Can be implemented using sleep mode. However, the watchdog timer (WDT) cannot be used. < Cancellation sources > • All interrupts • Reset (RST# pin reset, power-on reset, voltage monitoring reset, IWDT reset)
IDLE1 mode	Clock oscillator, PLL operation, and flash memory operation continue. < Cancellation sources > • Non-maskable interrupt request signal • Unmasked maskable interrupt request signal • Reset signal (reset triggered by RESET pin input, WDT2RES signal, low-voltage detector (LVI), or clock monitor (CLM))	Can be implemented using sleep mode and module stop function. < Cancellation sources > • All interrupts • Reset (RST# pin reset, power-on reset, voltage monitoring reset, IWDT reset)
IDLE2 mode	Clock oscillator, PLL operation, and flash memory operation continue. The PLL is restored to its state before the transition to IDLE2 mode. < Cancellation sources > • Non-maskable interrupt request signal • Unmasked maskable interrupt request signal • Reset signal (reset triggered by RESET pin input, WDT2RES signal, low-voltage detector (LVI), or clock monitor (CLM))	Can be implemented using sleep mode and module stop function. However, the PLL must be started or stopped using the normal procedure. < Cancellation sources > • All interrupts • Reset (RST# pin reset, power-on reset, voltage monitoring reset, IWDT reset)

Item	V850ES/JF3-L	RX231
STOP mode/ low-voltage STOP mode	Mode in which operation of all internal circuits is stopped < Cancellation sources > • Non-maskable interrupt request signal • Unmasked maskable interrupt request signal • Reset signal (reset triggered by RESET pin input, WDT2RES signal, low-voltage detector (LVI), or clock monitor (CLM))	Can be implemented using software standby mode. However, with some exceptions peripheral module operation is not possible. < Cancellation sources > • Interrupts from peripheral modules that can operate in software standby mode • Reset (RST# pin reset, power-on reset, voltage monitoring reset, IWDT reset)
Subclock operation mode/ low-voltage subclock operation mode	Mode in which the entire system operates on the subclock	Can be implemented by setting the sub-clock as the system clock and using low-speed operating mode.

Table 2.24 Operating Status after Transition to Each Mode

Function	V850ES/JF3-L							RX231		
	HALT	IDLE1	IDLE2	STOP	Low-voltage STOP	Subclock Operation	Low-Voltage Subclock Operation	Sleep	Deep Sleep	Software Standby
Main clock	○	○	○	×	×	○	○	○	○	×
Subclock	○	○	○	○	○	○	○	○	○	○
Internal oscillator/ HOCO LOCO	○	○	○	○	○	○	○	○	○	×
PLL	○	×	×	×	×	○	○	○	○	×
CPU	×	×	×	×	×	○	○	× (Retained)	× (Retained)	× (Retained)
DMA	○	×	×	×	×	○	○	○ *1	× (Retained)	× (Retained)
Watch timer/RTC	○	○	○	○ *2	○ *2	○	○	○	○	○
Watchdog timer 2/ independent watchdog timer	○	○	○	○	○	○	○	○ *3	○ *3	○ *3
Port functions	Retained	Retained	Retained	Retained	Retained	○	○	○	○	× (Retained)
Interrupt controller	○	× *4	× *4	× *4	× *4	○	○	○	○	○
Low-voltage detector/voltage detection circuit	○	○	○	○	○	○	○	○	○	○
RAM	Retained	Retained	Retained	Retained	Retained	Retained	Retained	× (Retained)	× (Retained)	× (Retained)
Registers	Retained	Retained	Retained	Retained	Retained	Retained	Retained	Retained	Retained	Retained
Other peripheral modules	*5	*5	*5	*5	*5	*5	*5	○	○	× (Retained)

○: operating, ×: stopped

“Retained” means that the setting values of internal registers are retained and the internal status is operation suspended.

Notes: 1. Writing to system control–related registers is prohibited in sleep mode. For details, refer to Table 5.1, List of I/O Registers (Address Order), in RX230 Group, RX231 Group User’s Manual: Hardware.
2. Operation is possible if a subclock is available.
3. Watchdog timer operation stops.
4. Only cancelling of standby mode is possible.
5. The conditions and modules on which operation is possible differ in each mode. For details, refer to chapter 21, STANDBY FUNCTION, in V850ES/JF3-L User’s Manual: Hardware.

2.18 Clock Monitor

2.18.1 Comparative Specifications

Table 2.25 lists correspondences between the specifications of the clock monitor functions on the V850ES/JF3-L and the oscillation stop detection function of the clock generation circuit on the RX231 Group.

Table 2.25 Clock Monitor Function Correspondences

Item	V850ES/JF3-L Clock Monitor	RX231 Oscillation Stop Detection Function
Target of monitoring	Main clock	Main clock
Operation when oscillation stop detected	Reset	• When main clock is selected as system clock: The system clock is switched to the low-speed on-chip oscillator and an oscillation stop detection interrupt*1 is generated. • When PLL is selected as system clock: The PLL switches to free-running oscillation and an oscillation stop detection interrupt is generated. • When USB-dedicated PLL is selected: The USB-dedicated PLL switches to free-running oscillation and an oscillation stop detection interrupt is generated.
Auto-shutdown of function	• From start of STOP mode until expiration of stabilization time • When sampling clock (internal oscillation clock) is halted • When CPU is operating on internal oscillation clock • When main clock is halted*2	No

Notes: 1. The oscillation stop detection interrupt is a non-maskable interrupt.
2. State in which the main clock has been halted intentionally by user software using the main clock oscillator control bit (PCC.MCK).

2.18.2 Usage Note

2.18.2.1 Disabling the Oscillation Stop Detection Function

The oscillation stop detection function on the RX231 Group is provided to deal with situations where the main clock is stopped by an external factor. Therefore, it is necessary to disable the oscillation stop detection function in advance before stopping the main clock by using software, transitioning to software standby mode, or the like. For details, refer to 9.5.1, Oscillation Stop Detection and Operation after Detection, in RX230 Group, RX231 Group User's Manual: Hardware.

2.19 Low-Voltage Detector (LVI)

2.19.1 Comparative Specifications

Table 2.26 lists correspondences between the specifications of the low-voltage detector (LVI) on the V850ES/JF3-L and the voltage detection circuit (LVDAb) on the RX231 Group.

Table 2.26 Low-Voltage Detector Function Correspondences

	V850ES/JF3-L	RX231		
Item	**Low-Voltage Detector (LVI)**	**LVDAb Voltage Monitoring 0**	**LVDAb Voltage Monitoring 1**	**LVDAb Voltage Monitoring 2**
Operation when voltage detected	• When V_{DD} < V_{LVI} or V_{DD} < V_{LVI} detection occurs, a maskable interrupt or reset request is generated. • Selectable between interrupt and reset.	• When Vdet0 > VCC, a reset occurs.	• When Vdet1 > VCC, a reset occurs. • When Vdet1 > VCC and/or VCC > Vdet1, an interrupt request is generated. • Selectable between maskable interrupt and non-maskable interrupt.	• When Vdet2 > VCC or CMPA2 pin, a reset occurs. • When Vdet2 > (VCC or CMPA2 pin) and/or (VCC or CMPA2 pin) > Vdet2, an interrupt request is generated. • Selectable between maskable interrupt and non-maskable interrupt.
Detection voltage	2 levels 2.30 V 2.80 V	4 levels 1.90 V 2.51 V 2.82 V 3.84 V	14 levels 1.86 V 1.96 V 2.20 V 2.48 V 2.58 V 2.68 V 2.79 V 2.90 V 3.00 V 3.10 V 3.84 V 4.02 V 4.14 V 4.29 V	4 levels 3.84 V 4.02 V 4.14 V 4.29 V

Notes: 1. When operation is enabled and the operating mode is set to “when power supply voltage < detection voltage, an internal reset signal is generated,” it is not possible to stop operation of the low-voltage detector (LVI) until a reset request other than a reset by the low-voltage detector is generated.

2. Do not use the non-maskable interrupt to initiate writing or erasing of the flash memory.

2.19.2 Usage Note

2.19.2.1 Usage Note Regarding Reenabling Voltage Detection

After voltage detection occurs once on the RX231 Group, the setting must be reset by, for example, clearing the detect flag. For details, refer to 8, Voltage Detection Circuit (LVDAb), in RX230 Group, RX231 Group User’s Manual: Hardware.

2.20 CRC Function

2.20.1 Comparative Specifications

Table 2.27 lists correspondences between the specifications of the CRC function on the V850ES/JF3-L and the CRC calculator (CRC) on the RX231 Group.

Table 2.27 CRC Function Correspondences

Item	V850ES/JF3-L CRC Function	RX231 CRC
Data unit	8 bits	8 bits
Formula	CRC-16-CCITT (16-bit CRC) $X^{16} + X^{12} + X^5 + 1$	CRC-16-CCITT (16-bit CRC) $X^{16} + X^{12} + X^5 + 1$ CRC-16-IBM (16-bit CRC) $X^{16} + X^{15} + X^2 + 1$ CRC-8-ATM (8-bit CRC) $X^8 + X^2 + X + 1$
Data transfer	Fixed at LSB.	Selectable between MSB and LSB.

3. Sample Programs

The distribution package containing this application note includes sample programs that reproduce in software functions of the V850ES/JF3-L that are not implemented in hardware on the RX231 Group.

The latest versions of the sample programs are available on the Renesas Electronics website.

3.1 Operation Confirmation Conditions

Table 3.1 shows the environment on which the operation of the sample programs has been confirmed.

Table 3.1 Operation Confirmation Conditions

Item	Description
MCU used	R5F52318ADFP
Operating frequencies	• Main clock: 8Hz • PLL: 54 MHz (main clock divided by 2 and multiplied by 13.5) • HOCO: Stopped • LOCO: 4 MHz • System clock (ICLK): 54 MHz (PLL divided by 1) • Peripheral module clock A (PCLKA): 54 MHz (PLL divided by 1) • Peripheral module clock B (PCLKB): 27 MHz (PLL divided by 2) • Peripheral module clock D (PCLKD): 54 MHz (PLL divided by 1) • FlashIF clock (FCLK): 27 MHz (PLL divided by 2) • External bus clock (BCLK): 27 MHz (PLL divided by 2)
Operating voltage	3.3 V
Integrated development environment	Renesas Electronics e² studio Version 2021-10
Compiler	Renesas Electronics C/C++ Compiler Package for RX Family V.3.03.00
	Default settings of integrated development environment
iodefine.h version	1.0I
Endian order	Little endian
Operating mode	Single-chip mode
Processor mode	Supervisor mode
Sample program version	Version 1.00
Board used	Renesas Starter Kit for RX231 (product No.: RTK5005231SxxxxxBE)

3.2 Project Structure

Table 3.2 lists the sample projects accompanying this application note, and Table 3.3 lists files in which changes were made to source code generated by the code generation function.

Table 3.2 Projects

Function	Project Name	Description
External trigger PWM output function	external_input_rx231	This project reproduces the functionality on the V850ES/JF3-L for using external trigger input to initiate count start and PWM output on the RX231 Group using the IRQ external input interrupt*1 and the multi-function timer pulse unit in PWM mode 1.
One-shot pulse output function	one_shot_pulse_rx231	This project reproduces the functionality on the V850ES/JF3-L for using external trigger input to initiate count start and one-shot pulse output on the RX231 Group using the IRQ external input interrupt*1 and the multi-function timer pulse unit in PWM mode 1.
Real-time output function	rto_output_rx231	This project reproduces the real-time output function on the V850ES/JF3-L on the RX231 Group using the port group output function of the event link controller and the TMR.

Note: 1. Connected to SW1 (tactile switch) on the RSK board.

Table 3.3 Changes to Files Generated by Code Generation Function

Project	Folder	File Name	Description
external_input_rx231	Config_ICU	Config_ICU_user.c	User-implemented interrupt handling
one_shot_pulse_rx231	Config_ICU	Config_ICU_user.c	User-implemented interrupt handling
	Config_MTU	Config_MTU0_user.c	User-implemented interrupt handling
rto_output_rx231	Config_ICU	Config_ICU_user.c	User-implemented interrupt handling
	Config_TMR	Config_TMR0_user.c	User-implemented interrupt handling

Note: For details of the added processing, refer to 3.5, Flowcharts. Source code generated by the code generation function of Smart Configurator that has not been modified is omitted.

3.3 Functions

Table 3.4 lists the functions used by the sample programs.

Table 3.4 Functions Used by Sample Programs

Function Name	Description
main	Main processing routine
r_Config_ICU_irq1_interrupt	External interrupt handler
r_Config_MTU0_tgib0_interrupt	MTU0 compare match interrupt processing (only used by one-shot pulse output function sample program)
r_Config_TMR0_cmia0_interrupt	TMR0 compare match interrupt processing (only used by real-time output function sample program)

Note: Source code generated by the code generation function of Smart Configurator that has not been modified is omitted.

3.4 Function Specifications

The sample code function specifications are listed below.

main	
Outline	Main processing routine
Header	None
Declaration	void main (void)
Description	Makes initial settings.
Arguments	None
Return Value	None

r_Config_ICU_irq1_interrupt	
Outline	IRQ1 interrupt handler
Header	Config_ICU.h
Declaration	static void r_Config_ICU_irq1_interrupt (void)
Description	Handles the IRQ1 interrupt. The IRQ1 interrupt handler starts count operation on MTU0.
Arguments	None
Return Value	None
Remarks	This function is generated by the code generation function of Smart Configurator. It is only used by external_input_rx231 and one_shot_pulse_rx231.

r_Config_MTU0_tgib0_interrupt	
Outline	MTU0 compare match B interrupt processing
Header	Config_MTU0.h
Declaration	static void r_Config_MTU0_tgib0_interrupt (void)
Description	Handles the MTU0 compare match interrupt. The MTU0 compare match interrupt handler stops count operation on MTU0.
Arguments	None
Return Value	None
Remarks	This function is generated by the code generation function of Smart Configurator. This function is only used by one_shot_pulse_RX231.

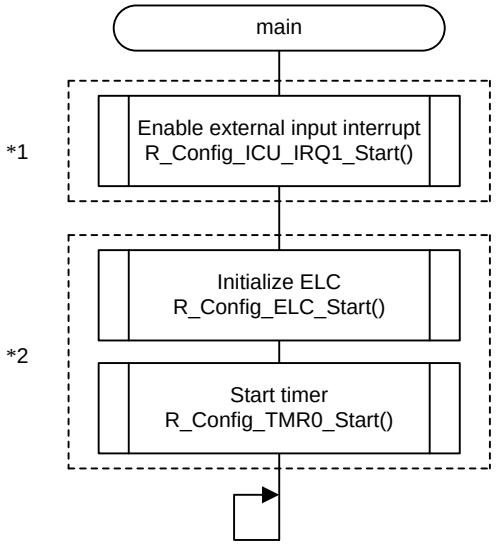
r_Config_TMR0_cmia0_interrupt	
Outline	TMR0 compare match A interrupt processing
Header	Config_TMR0.h
Declaration	static void r_Config_TMR0_cmia0_interrupt (void)
Description	Handles the TMR0 compare match interrupt. The TMR0 compare match interrupt handler configures PDBF1 register settings.
Arguments	None
Return Value	None
Remarks	This function is generated by the code generation function of Smart Configurator. This function is only used by rto_output_rx231.

3.5 Flowcharts

The sample programs make use of the code generation function. This section contains flowcharts of functions containing changes to the program code generated by e^2 studio and that are used to reproduce the hardware functionality of the V850ES/JF3-L. For details of other peripheral functions, etc., refer to the setting screens in Smart Configurator and the generated code.

3.5.1 Main

Figure 3.1 is a flowchart of the main processing routine.

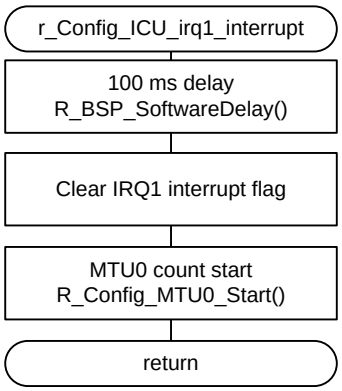


Notes: 1. Only exists in one_shot_pulse_rx231 and external_input_rx231.
2. Only exists in rto_output_rx231.

Figure 3.1 Main Processing Routine

3.5.2 External Interrupt Handler

Figure 3.2 is a flowchart of the external interrupt handler.



Note: The 100 ms delay is to accommodate chattering by SW1 (tactile switch).

Figure 3.2 External Interrupt Handler

3.5.3 MTU0 Interrupt Handler of One-Shot Pulse Output Function

Figure 3.3 is a flowchart of the timer interrupt handler of the one-shot pulse output function.

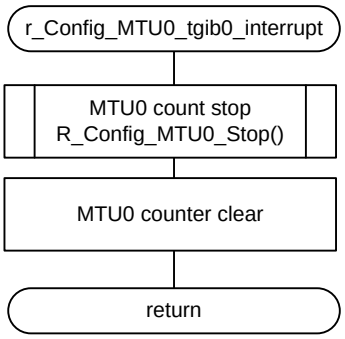


Figure 3.3 Timer Interrupt Handler of One-Shot Pulse Output Function

3.5.4 TMR0 Interrupt Handler of Real-Time Output Function

Figure 3.4 is a flowchart of the timer interrupt handler of the real-time output function.

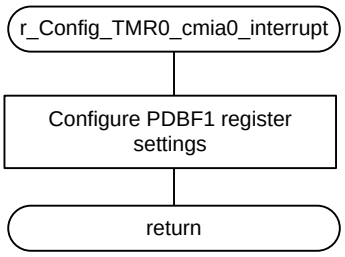


Figure 3.4 Timer Interrupt Handler of Real-Time Output Function

4. Importing a Project

The sample programs are distributed in e² studio project format. This section shows how to import a project into e² studio. After importing a project, check the build and debug settings.

4.1 Procedure in e² studio

To use sample programs in e² studio, follow the steps below to import them into e² studio. (Note that depending on the version of e² studio you are using, the interface may appear somewhat different from the screenshots below.)

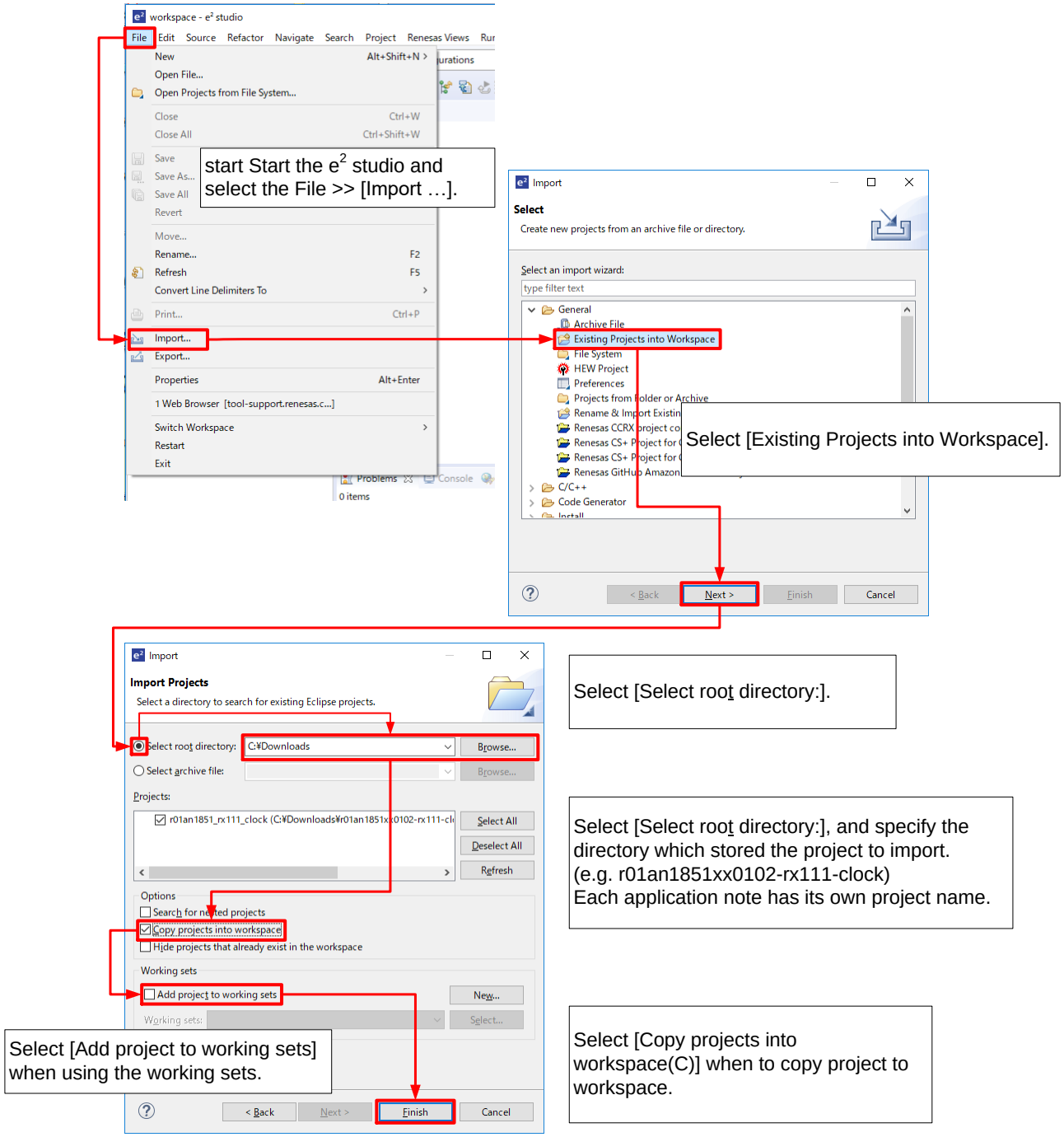


Figure 4.1 Importing a Project into e² studio

Notes: In projects managed by e² studio, do not use space codes, multibyte characters, and symbols such as "$", "#", "%" in folder names or paths to them.

4.2 Procedure in CS+

To use sample programs in CS+, follow the steps below to import them into CS+. (Note that depending on the version of CS+ you are using, the interface may appear somewhat different from the screenshots below.)

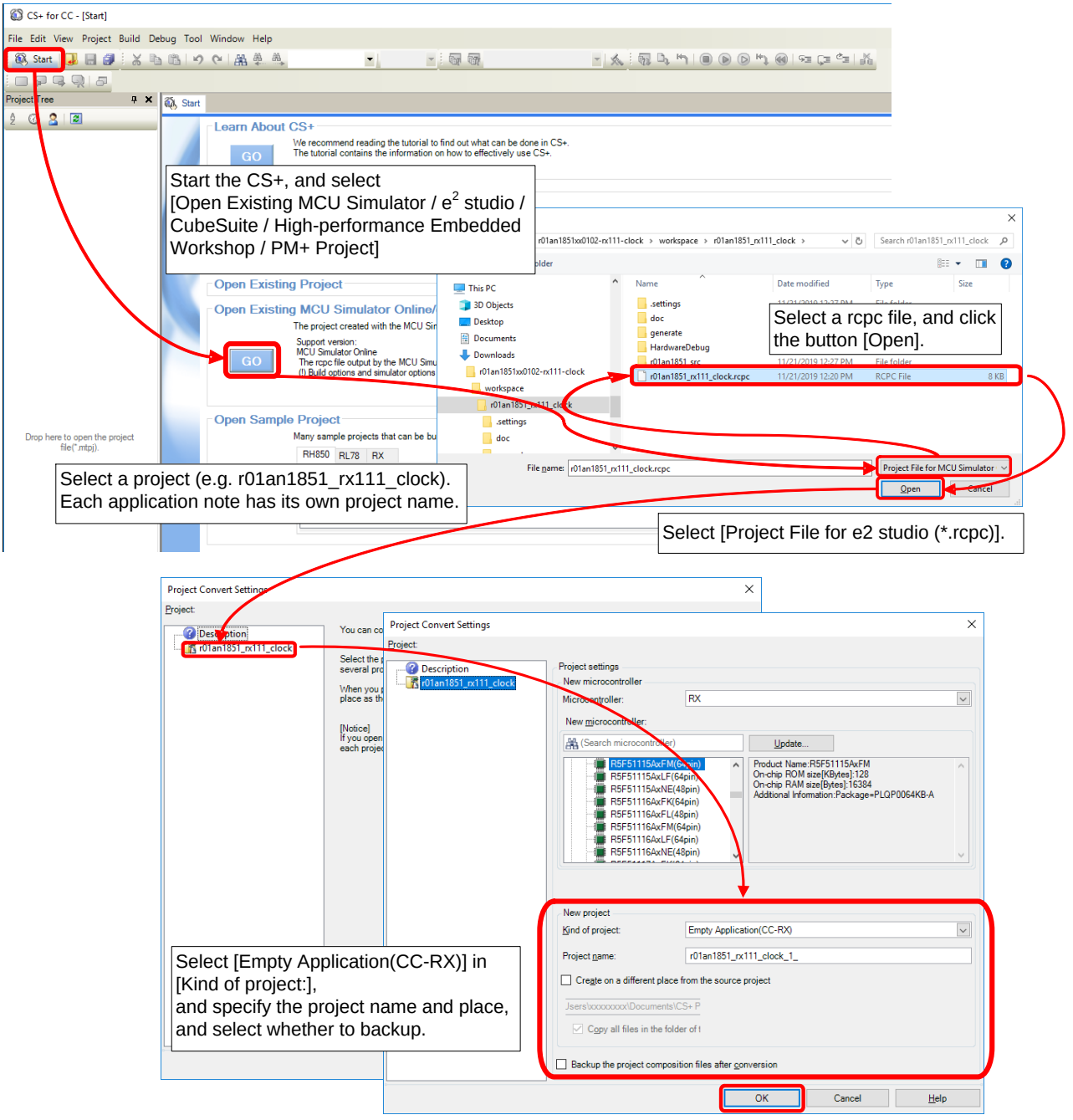


Figure 4.2 Importing a Project into CS+

Notes: In projects managed by CS +, do not use space codes, multibyte characters, and symbols such as "$", "#", "%" in folder names or paths to them.

5. Reference Documents

User's Manual: Hardware

RX230 Group, RX231 Group User's Manual: Hardware (R01UH0496)
V850ES/JF3-L User's Manual: Hardware (R01UH0017)
(The latest version can be downloaded from the Renesas Electronics website.)

Technical Updates/Technical News

(The latest information can be downloaded from the Renesas Electronics website.)

User's Manual: Development Tools

CC-RX Compiler User's Manual (R20UT3248)
(The latest version can be downloaded from the Renesas Electronics website.)

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Dec. 29.21	—	First edition issued

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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