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H8SX Family

Using TPU to Clear External WDT during Flash Memory Programming/Erasing

Introduction

This example shows how to use a 16-bit timer pulse unit (TPU) to clear an external watchdog timer (external WDT) during the programming or erasure of flash memory.

Normally, user processing cannot be executed during programming/erasing of the on-chip flash memory of the MCU. In systems where an external watchdog timer (WDT) is connected to the microcomputer, on-going programming /erasing processing is aborted due to resetting of the MCU, since the WDT-clearing signal from the MCU is stopped. This application describes an example where resetting of the MCU is avoided by internally running the TPU during programming/erasing so that the WDT-clearing signal is output in the same way as in normal operation.

The WDT should be cleared by user processing while the user program is running.

Target Device

H8SX/1638F

Preface

Other than the target device indicated above, the program covered in this application note can be run on H8SX devices that have the same I/O registers as those employed by the program. However, since some functional modules may be changed for the addition of functionality etc., be sure to perform a thorough evaluation by confirming the details with the hardware manual for the actual target device

Contents

1. Specifications

This application note describes an example of clearing the external WDT during programming/erasing of flash memory by using the output-compare function of the TPU. The specifications are described below. An example of the connection for this sample application is shown in figure 1.

(1) The 3V supply system reset IC with watchdog timer (M62050) from Renesas Technology is used as the WDT. In this sample, only its watchdog timer function is used. The watchdog timer period is set to 120 ms. For details, see the M62050 datasheet.

(2) The external WDT outputs a reset signal if an external WDT clear signal is not input within 120 ms. While any external WDT clear signal is continued to be input to the external WDT input (WD pin), the M62050 retains the $\overline{\text{RST1}}$ pin high. It outputs low (reset signal) from the $\overline{\text{RST1}}$ pin to reset the H8SX MCU when the WDT clear signal is missed.

(3) The H8SX MCU employs the TPU_3 output-compare function to toggle the TIOCA3 pin output during flash memory programming/erasing. The TIOCA3 pin produces an input signal for the WD pin of the external WDT every time a compare-match interrupt occurs (about every 10 ms), and this acts as a clearing signal for the external WDT. This operation ensures that the MCU is able to continue processing to erase or program the flash memory without being reset.

(4) This sample application is also capable of stopping the clearing signal for the external WDT when abnormal processing is intentionally initiated. An IRQ interrupt for the H8SX MCU stops output of the WDT-clearing signal from the TIOCA3 pin, in turn causing the WDT to output a reset signal. Input of the reset signal to the $\overline{\text{RES}}$ pin of the H8SX MCU resets the MCU.

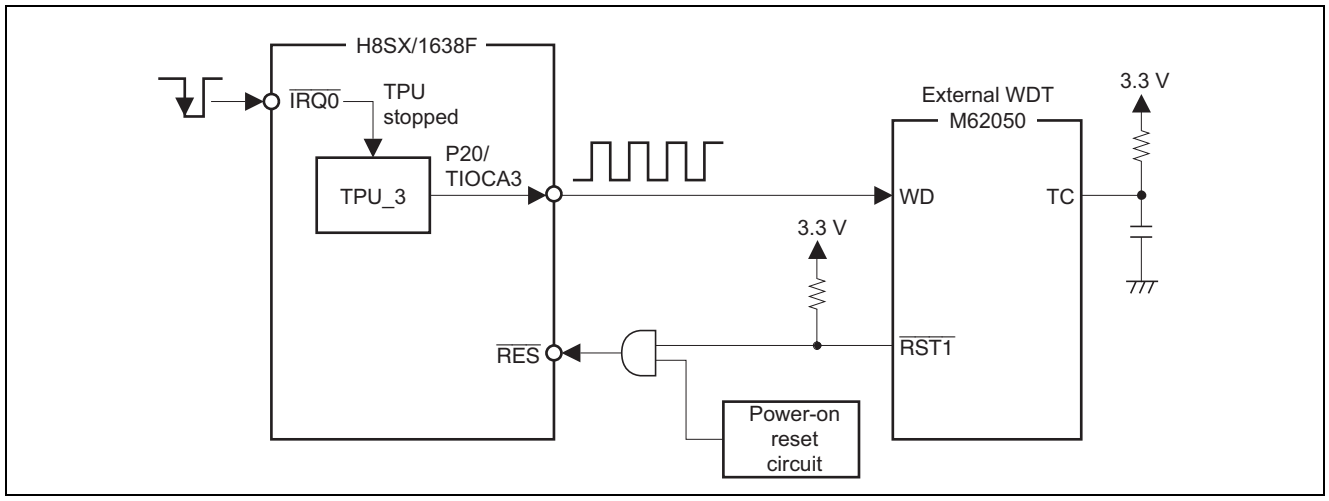


Figure 1 External WDT Connection Using TPU

2. Applicable Conditions

Table 1 Applicable Conditions

Item	Setting	
Operating frequency	Input clock	: 12 MHz
	System clock (Iϕ)	: 24 MHz (input clock frequency × 2)
	Peripheral module clock (Pϕ)	: 24 MHz (input clock frequency × 2)
	External bus clock (Bϕ)	: 24 MHz (input clock frequency × 2)
Operating mode	Mode 7 (single chip mode)	
	Mode pin settings: MD2 = 1, MD1 = 1, MD0 = 1	

3. Description of Operation

3.1 Operation Timing

Figure 2 shows the timing for clearing the WDT by using the TPU. To explain (1) to (4) in figure 2, detailed descriptions are given in tables 2 and 3.

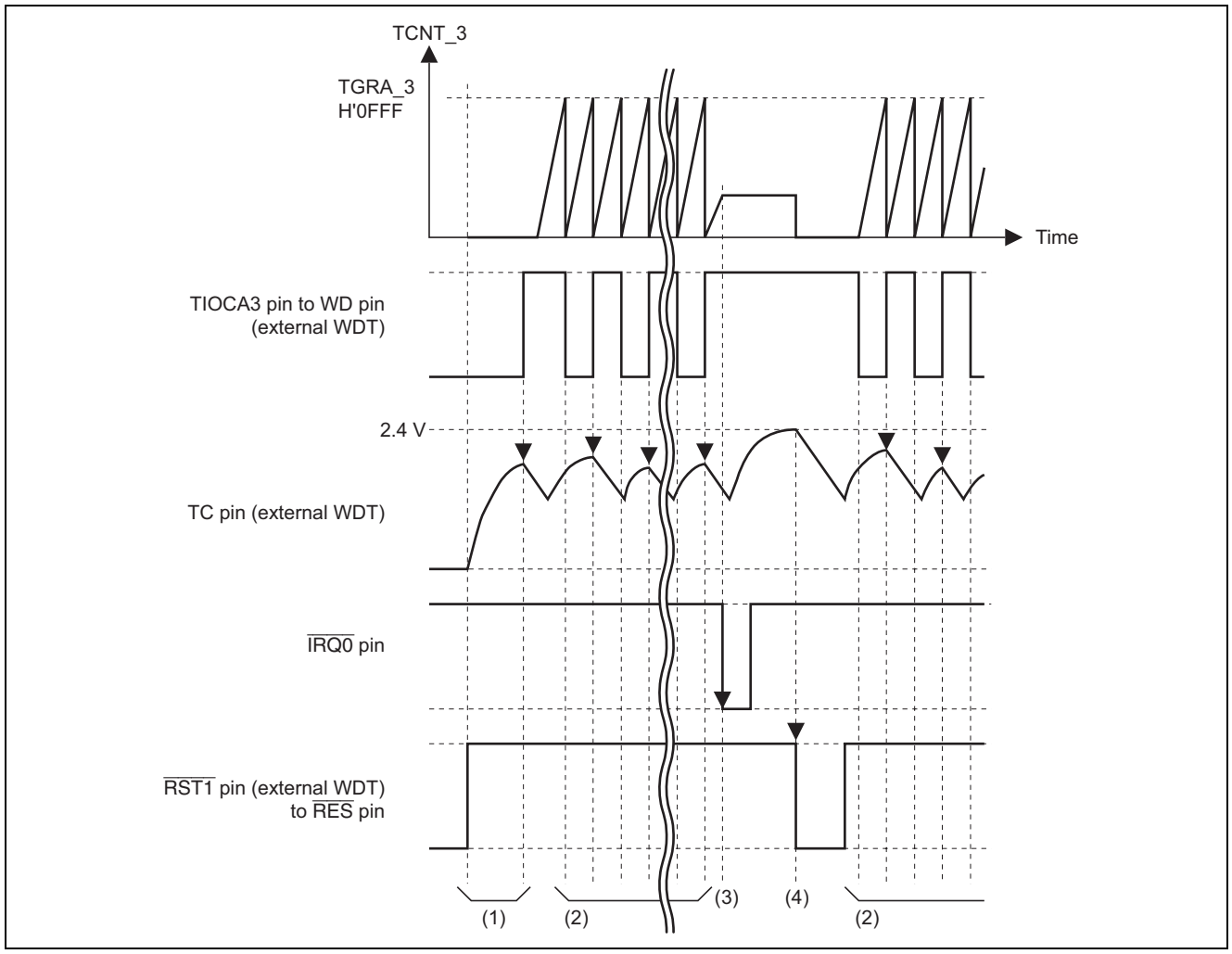


Figure 2 Operation Timing

Table 2 Description of Normal Operation Processing

	Hardware processing	Software processing
(1)	Power-on reset	Initial setting (a) Set the TIOCA3 pin to output 1 initially. (b) For other settings, see section 4, Description of Software.
(2)	On a TGRA_3 compare match (a) The TIOCA3 pin output is toggled to 0 or 1 for (input of 0 or 1 to the WD pin of the external WDT). The M62050 retains the $\overline{\text{RST1}}$ pin output at 1 as long as a 1 is input to the external WDT (external WDT clearing signal input) before the potential on the TC pin reaches 2.4 V. (b) Clear TCNT_3. This processing is repeated while in normal operation.	No processing

Table 3 Description of Abnormal Operation Processing

	Hardware processing	Software processing
(3)	IRQ0 Interrupt (a) Set IRQ0F of ISR to 1 at the rising edge. (b) Clear IRQ0F of ISR to 0 by executing IRQ0 interrupt exception handling.	IRQ0 Interrupt Exception Handling (a) Stop TCNT_3 counting operation. (b) Dummy wait for at least 200 ms.
(4)	Internal reset (a) Input 0 to the H8SX/1638F $\overline{\text{RES}}$ pin (0 is output from the $\overline{\text{RST1}}$ pin of the external WDT). (b) Reset the H8SX/1638F.	Initial setting (a) Set the TIOCA3 pin to output 1 initially. (b) For other settings, see section 4, Description of Software.

Legend:
TGRA_3: Timer general register A_3
TCNT_3: Timer counter_3
ISR: IRQ status register

3.2 Calculating the Clearing Period for the External WDT

TPU_3 inverts the TIOCA3 pin on every TGRA_3 compare match. When TGRA_3 = H'0FFF, Pϕ=24 MHz, and the TCNT_3 counter clock frequency =Pϕ/64, the TPU_3 compare match interval is calculated as follows.

$$\text{TPU\_3 compare match time} = \frac{\text{TGRA\_3} + 1}{(\text{P}/64)} = \frac{\text{H'0FFF} + 1}{24\ \text{MHz}/64} \approx 10.92\ \text{ms}$$

Therefore, the period for clearing of the external WDT by a low-level output is as follows because the compare-match period is for inversion of the TIOCA3 pin output.

$$\text{External WDT clearing period} = \text{compare match time} \times 2 = 10.92 \times 2 \approx 21.84\ \text{ms}$$

Since the external WDT clearing signal is output with a period shorter than the external WDT setting time (120 ms), the H8SX MCU can continue processing for flash memory programming/erasing without being reset by the external WDT.

4. Description of Software

4.1 Operating Environment

Table 4 Operating Environment

Item	Details
Development tool	High-performance Embedded Workshop Ver.4.03.00
C/C++ compiler	H8S,H8/300 SERIES C/C++ Compiler Ver6.02.00 (manufactured by Renesas Technology)
	Option settings: -cpu=h8sxa:24:md, -code = machinecode, -optimize=1, -regparam=3 -speed=(register,shift,struct,expression)
Optimizing linkage editor	Optimizing Linkage Editor Ver.9.03.00 (manufactured by Renesas Technology)
	Option settings: None

Table 5 Section Settings

Address	Section Name	Description
H'001000	P	Program area

Table 6 Vector Table for Interrupt Exception Handling

Exception Handling Source	Vector No.	Address in Vector Table	Destination Interrupt Processing Function
Reset	0	H'000000	init
IRQ0	64	H'000100	irq0_int

4.2 List of Functions

Table 7 list the functions used in this sample. Figure 3 shows the hierarchical structure of calls.

Table 7 List of Functions

Function Name	Function
init	Initialization routine Releases the modules from module stop mode, configures the clocks, and calls the main function.
main	Main routine Configures TPU_3 for the output-compare function and sets the TIOCA3 pin to output the external WDT clear signal to the external WDT. It also enables the IRQ0 interrupt.
irq0_int	IRQ0 interrupt exception handling Stops the signal from the TIOCA3 pin to cause the external WDT to output a reset signal.

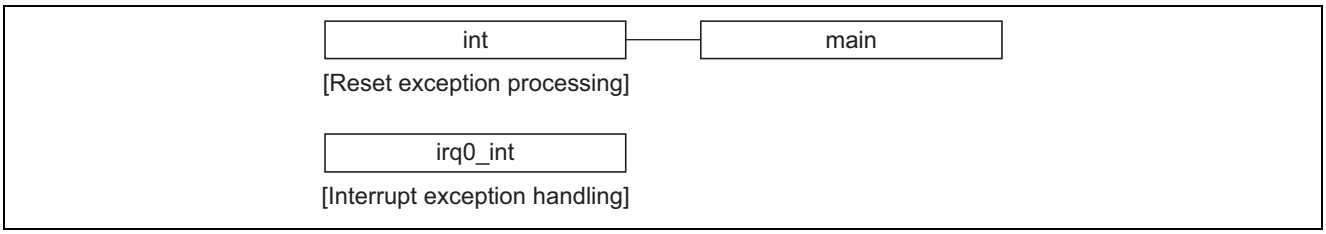


Figure 3 Hierarchical Structure

4.3 Description of Functions

4.3.1 init Function

1. Functional overview
   Initialization routine. It releases the modules from module stop mode, configures the clocks, and calls the main function.
2. Arguments
   None
3. Return value
   None
4. Description of internal registers used
   The internal registers used in this sample task are listed below. Note that settings presented below are used in this sample task and are not the initial values.

- Mode control register (MDCR) Number of bits: 16 Address: H'FFFDC0

Bit	Bit Name	Setting	R/W	Description
15	MDS7	—*	R	This bit indicates the value set by the mode pin (MD3). When MDCR is read, the signal level input on pin MD3 is latched into this bit. This latch is released by a reset.
11	MDS3	—*	R	Mode Select 3 to 0
10	MDS2	—*	R	These bits indicate the operating mode selected by the mode pins (MD2 to MD0) (see table 8).
9	MDS1	—*	R	When MDCR is read, the signal levels input on pins MD2 to MD0 are latched into these bits. These latches are released by a reset.
8	MDS0	—*	R	

Note: * Determined by the settings on pins MD3 to MD0.

Table 8 Settings of Bits MDS3 to MDS0

MCU Operating Mode	Mode Pins			MDCR			
	MD2	MD1	MD0	MDS3	MDS2	MDS1	MDS0
1	0	0	1	1	1	0	1
2	0	1	0	1	1	0	0
3	0	1	1	0	1	0	0
4	1	0	0	0	0	1	0
5	1	0	1	0	0	0	1
6	1	1	0	0	1	0	1
7	1	1	1	0	1	0	0

- System clock control register (SCKCR) Number of bits: 16 Address: H'FFFDC4

Bit	Bit Name	Setting	R/W	Description
10	ICK2	0	R/W	System Clock (Iϕ) Select
9	ICK1	0	R/W	These bits select the frequency of the system clock provided to
8	ICK0	1	R/W	the CPU, DMAC, and DTC. 001: Input clock × 2
6	PCK2	0	R/W	Peripheral Module Clock (Pϕ) Select
5	PCK1	0	R/W	These bits select the frequency of the peripheral module clock.
4	PCK0	1	R/W	001: Input clock × 2
2	BCK2	0	R/W	External Bus Clock (Bϕ) Select
1	BCK1	0	R/W	These bits select the frequency of the external bus clock.
0	BCK0	1	R/W	001: Input clock × 2

- MSTPCRA, MSTPCRB, and MSTPCRC control module stop mode. Setting a bit to 1 makes the corresponding module enter the module stop mode, while clearing the bit to 0 releases the module from module stop mode.

- Module stop control register A (MSTPCRA) Number of bits: 16 Address: H'FFFDC8

Bit	Bit Name	Setting	R/W	Target Module
15	ACSE	0	R/W	All-Module-Clock-Stop Mode Enable Enables/disables all-module-clock-stop mode for reducing current consumption by stopping the bus controller and I/O ports operations when the CPU executes the SLEEP instruction after the module stop state has been set for all of the on-chip peripheral modules controlled by MSTPCR. 0: All-module-clock-stop mode disabled 1: All-module-clock-stop mode enabled
13	MSTPA13	1	R/W	DMA controller (DMAC)
12	MSTPA12	1	R/W	Data transfer controller (DTC)
9	MSTPA9	1	R/W	8-bit timers (TMR_3 and TMR_2)
8	MSTPA8	1	R/W	8-bit timers (TMR_1 and TMR_0)
5	MSTPA5	1	R/W	D/A converter (channels 1 and 0)
3	MSTPA3	1	R/W	A/D converter (unit 0)
1	MSTPA1	1	R/W	16-bit timer pulse unit (TPU channels 11 to 6)
0	MSTPA0	0	R/W	16-bit timer pulse unit (TPU channels 5 to 0)

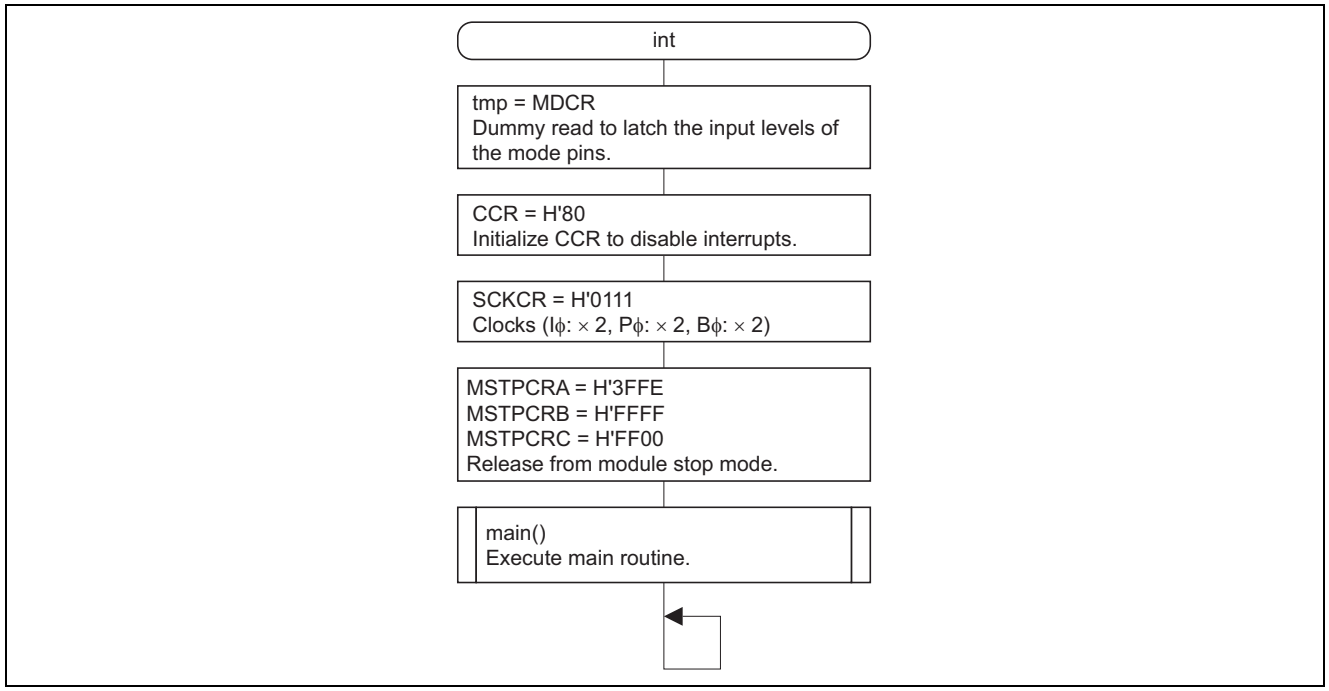
- Module stop control register B (MSTPCRB) Number of bits: 16 Address: H'FFFDCA

Bit	Bit Name	Setting	R/W	Target Module
15	MSTPB15	1	R/W	Programmable pulse generator (PPG_0: PO15 to PO0)
12	MSTPB12	1	R/W	Serial communications interface_4 (SCI_4)
11	MSTPB11	1	R/W	Serial communications interface_3 (SCI_3)
10	MSTPB10	1	R/W	Serial communications interface_2 (SCI_2)
9	MSTPB9	1	R/W	Serial communications interface_1 (SCI_1)
8	MSTPB8	1	R/W	Serial communications interface_0 (SCI_0)
7	MSTPB7	1	R/W	I^2C bus interface 2_1 (IIC2_1)
6	MSTPB6	1	R/W	I^2C bus interface 2_0 (IIC1_0)
5	MSTPB5	1	R/W	User break controller (USC)

- Module stop control register C (MSTPCRC) Number of bits: 16 Address: H'FFFDCC

Bit	Bit Name	Setting	R/W	Target Module
15	MSTPC15	1	R/W	Serial communications interface_5 (SCI_5), (IrDA)
14	MSTPC14	1	R/W	Serial communications interface_6 (SCI_6)
13	MSTPC13	1	R/W	8-bit timers (TMR_4 and TMR_5)
12	MSTPC12	1	R/W	8-bit timers (TMR_6 and TMR_7)
10	MSTPC10	1	R/W	Cyclic redundancy checker
9	MSTPC9	1	R/W	A/D converter (unit 1)
8	MSTPC8	1	R/W	Programmable pulse generator (PPG_1: PO31 to PO16)
7	MSTPC7	0	R/W	On-chip RAM_6 (H'FEE000 to H'FEFFFF)
6	MSTPC6	0	R/W	Always set the MSTPC7 and MSTPC6 bits to the same value.
5	MSTPC5	0	R/W	On-chip RAM_5, 4 (H'FF0000 to H'FF3FFF)
4	MSTPC4	0	R/W	Always set the MSTPC5 and MSTPC4 bits to the same value.
3	MSTPC3	0	R/W	On-chip RAM_3, 2 (H'FF4000 to H'FF7FFF)
2	MSTPC2	0	R/W	Always set the MSTPC3 and MSTPC2 bits to the same value.
1	MSTPC1	0	R/W	On-chip RAM_1, 0 (H'FF8000 to H'FFBFFF)
0	MSTPC0	0	R/W	Always set the MSTPC1 and MSTPC0 bits to the same value.

5. Flowcharts



4.3.2 main Function

1. Functional overview
   Main routine: configures TPU_3 for the output-compare function and sets the TIOCA3 pin to output the external WDT clearing signal to the external WDT. This function also enables the IRQ0 interrupt.
2. Arguments
   None
3. Return value
   None
4. Description of internal registers used
   The internal registers used in this sample task are listed below. Note that settings presented below are used in this sample task and are not the initial values.

- Port 3 data direction register (P3DDR) Number of bits: 8 Address: H'FFFB82

Bit	Bit Name	Setting	R/W	Description
0	P30DDR	1	R/W	0: Selects pin P30 as input 1: Selects pin P30 as output

- Port 5 input buffer control register (P5ICR) Number of bits: 8 Address: H'FFFB94

Bit	Bit Name	Setting	R/W	Description
0	P50ICR	1	R/W	0: Disables input buffer for pin P50 ($\overline{\text{IRQ0}}$-B). 1: Enables input buffer for pin P50 ($\overline{\text{IRQ0}}$-B).

- Port function control register C (PFCRC) Address: H'FFFBCC

Bit	Bit Name	Setting	R/W	Description
0	ITS0	1	R/W	$\overline{\text{IRQ0}}$ Pin Select 0: Selects pin P10 as $\overline{\text{IRQ0}}$-A input. 1: Selects pin P50 as $\overline{\text{IRQ0}}$-B input.

- IRQ sense control register L (ISCRL) Number of bits: 16 Address: H'FFFD6A

Bit	Bit Name	Setting	R/W	Description
1	IRQ0SR	0	R/W	IRQ0 Sense Control Rise
0	IRQ0SF	1	R/W	IRQ0 Sense Control Fall 01: Interrupt request generated by at falling edge of $\overline{\text{IRQ0}}$

- IRQ enable register (IER) Number of bits: 16 Address: H'FFFF34

Bit	Bit Name	Setting	R/W	Description
0	IRQ0E	1	R/W	IRQ0 Enable 0: Disables IRQ0 interrupt requests. 1: Enables IRQ0 interrupt requests.

- IRQ status register (ISR) Number of bits: 16 Address: H'FFFF36

Bit	Bit Name	Setting	R/W	Description
0	IRQ0F	0	R/(W)*	[Setting condition] • Occurrence of the interrupt selected by ISCR [Clearing condition] • Writing 0 after having read it as 1 • Execution of interrupt exception handling while low-level sensing is selected and $\overline{\text{IRQn}}$ inputs is high (n = 11 to 0) • Execution of IRQn interrupt exception handling while falling-, rising- or both-edge sensing is selected • Activation of the DTC by an IRQn interrupt, and clearing of the DISEL bit in MRB of the DTC to 0

Note: * Only 0 can be written, to clear the flag.

- Port 3 data register (P3DR) Number of bits: 8 Address: H'FFFF52

Bit	Bit Name	Setting	R/W	Description
0	P30DR	0/1	R/W	0: The P30 pin is low. 1: The P30 pin is high.

- Timer start register (TSTR) Number of bits: 8 Address: H'FFFFBC

Bit	Bit Name	Setting	R/W	Description
5	CST5	0	R/W	Counter Start 5 to 0
4	CST4	0	R/W	These bits select operation or stoppage for TCNT.
3	CST3	1	R/W	0: TCNT_5 to TCNT_0 is stopped.
2	CST2	0	R/W	1: TCNT_5 to TCNT_0 performs count operation.
1	CST1	0	R/W	
0	CST0	0	R/W	

- Timer control register _3(TCR_3) Number of bits: 8 Address: H'FFFFF0

Bit	Bit Name	Setting	R/W	Description
7	CCLR2	0	R/W	Counter Clear 2 to 0
6	CCLR1	0	R/W	Select the trigger for clearing of counter TCNT_3.
5	CCLR0	1	R/W	001: TCNT_3 cleared on a compare match of/input capture in TGRA_3.
4	CKEG1	0	R/W	Clock Edge 1 and 0
3	CKEG0	0	R/W	Selects the input clock edge. 00: Counts on falling edges.
2	TPSC2	0	R/W	Timer Prescaler 2 to 0
1	TPSC1	1	R/W	Select the counter clock for TCNT_3.
0	TPSC0	1	R/W	011: Counts on the internal clock Pϕ/64.

- Timer mode register_3(TMDR_3) Number of bits: 8 Address: H'FFFFF1

Bit	Bit Name	Setting	R/W	Description
3	MD3	0	R/W	Mode 3 to 0
2	MD2	0	R/W	Set the timer-operating mode.
1	MD1	0	R/W	0000: Normal operation
0	MD0	0	R/W	

- Timer I/O control register H_3(TIORH_3) Number of bits: 8 Address: H'FFFFF2

Bit	Bit Name	Setting	R/W	Description
3	IOA3	0	R/W	I/O Control A3 to A0
2	IOA2	1	R/W	Specify the function of TGRA_3.
1	IOA1	1	R/W	0111: TGRA_3 functions as an output-compare register.
0	IOA0	1	R/W	The output on TIOCA3 is initially 1, and is toggled on each compare match.

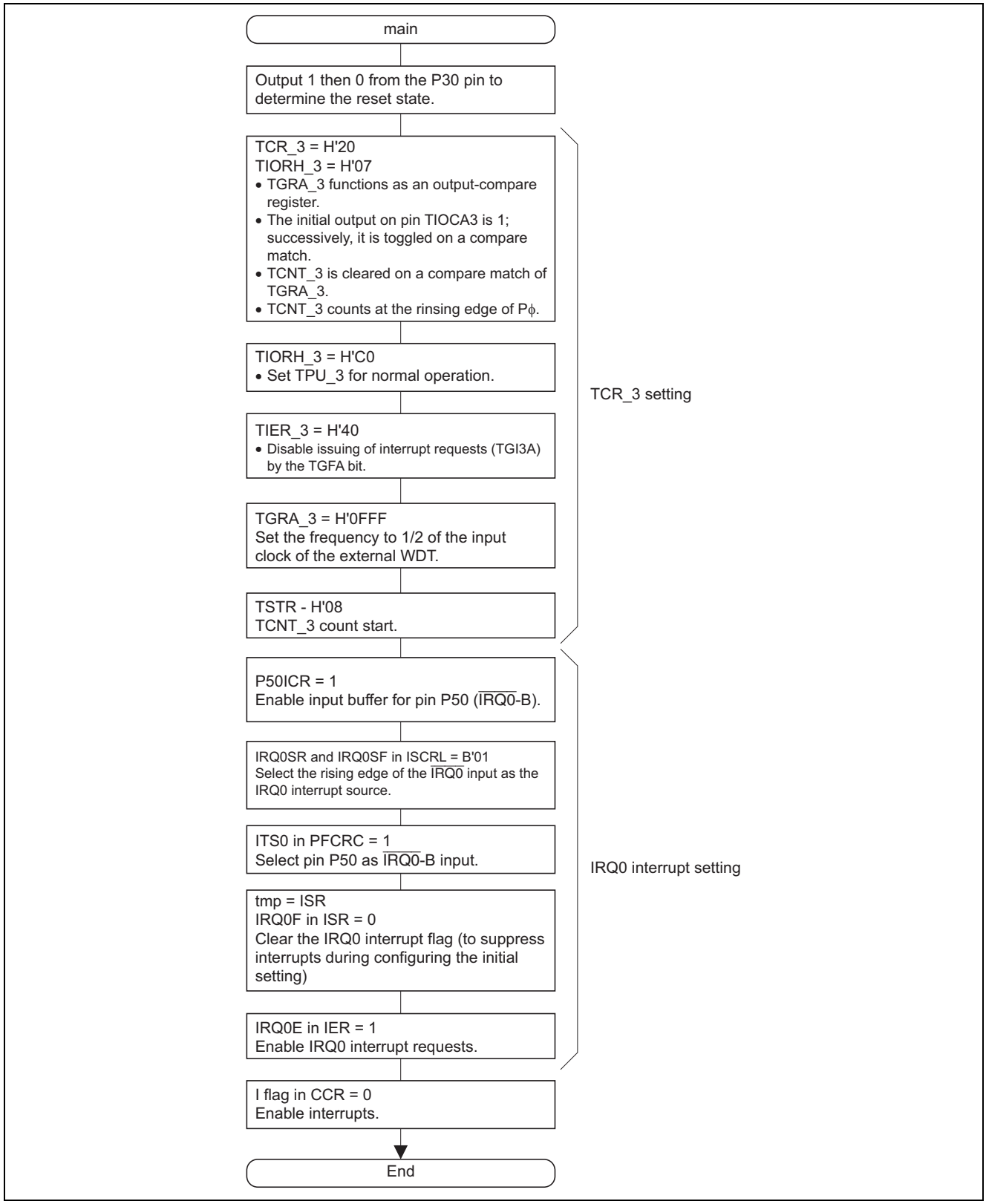
- Timer interrupt enable register_3(TIER_3) Number of bits: 8 Address: H'FFFFF4

Bit	Bit Name	Setting	R/W	Description
0	TGIEA	0	R/W	TGR Interrupt Enable A Enables or disables the operation of interrupt requests (TGIA) when the TGFA bit of TSR is set to 1. 0: Disables issuing of interrupt requests (TGIA) by the TGFA bit. 1: Enables issuing of interrupt requests (TGIA) by the TGFA bit.

- Timer general register A_3 (TGRA_3) Number of bits: 16 Address: H'FFFFF8

  Function: TGRA_3 is used as an output-compare register in this sample.
  Setting: H'0FFF

5. Flowchart


main
Output 1 then 0 from the P30 pin to determine the reset state.
TCR_3 = H'20
TIORH_3 = H'07
• TGRA_3 functions as an output-compare register.
• The initial output on pin TIOCA3 is 1; successively, it is toggled on a compare match.
• TCNT_3 is cleared on a compare match of TGRA_3.
• TCNT_3 counts at the rinsing edge of Pϕ.
TIORH_3 = H'C0
• Set TPU_3 for normal operation.
TIER_3 = H'40
• Disable issuing of interrupt requests (TGI3A) by the TGFA bit.
TGRA_3 = H'0FFF
Set the frequency to 1/2 of the input clock of the external WDT.
TSTR - H'08
TCNT_3 count start.
TCR_3 setting
P50ICR = 1
Enable input buffer for pin P50 (IRQ0-B).
IRQ0SR and IRQ0SF in ISCRL = B'01
Select the rising edge of the IRQ0 input as the IRQ0 interrupt source.
ITS0 in PFCRC = 1
Select pin P50 as IRQ0-B input.
tmp = ISR
IRQ0F in ISR = 0
Clear the IRQ0 interrupt flag (to suppress interrupts during configuring the initial setting)
IRQ0E in IER = 1
Enable IRQ0 interrupt requests.
IRQ0 interrupt setting
I flag in CCR = 0
Enable interrupts.
End

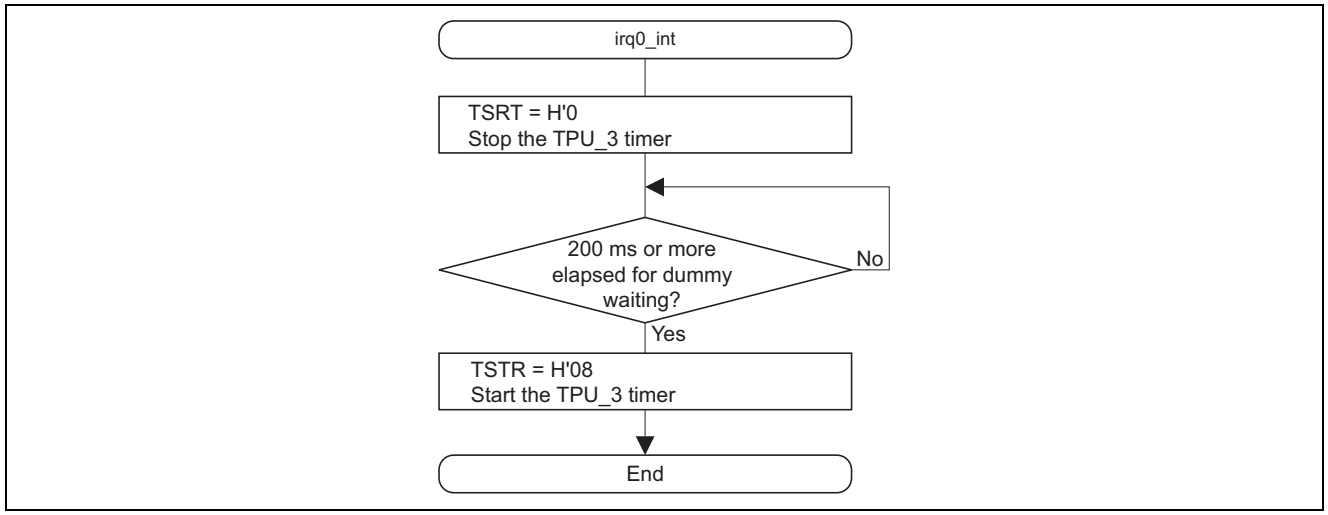
4.3.3 irq0_int Function

1. Functional overview
   IRQ0 interrupt exception handling. This function stops the signal from the TIOCA3 pin, causing the external WDT to output a reset signal.
2. Arguments
   None
3. Return value
   None
4. Description of internal registers used
   The internal registers used in this sample task are listed below. Note that settings presented below are used in this sample task and are not the initial values.

- Timer start register (TSTR) Number of bits: 8 Address: H'FFFFBC

Bit	Bit Name	Setting	R/W	Description
5	CST5	0	R/W	Counter Start 5 to 0
4	CST4	0	R/W	These bits select operation or stoppage for TCNT.
3	CST3	0/1	R/W	0: TCNT_5 to TCNT_0 count operation is stopped
2	CST2	0	R/W	1: TCNT_5 to TCNT_0 performs count operation.
1	CST1	0	R/W	
0	CST0	0	R/W	

5. Flowchart



5. Documents for Reference

- Hardware Manual
  H8SX/1638 Group Hardware Manual
  The most up-to-date version of this document is available on the Renesas Technology Website.
- Technical News/Technical Update
  The most up-to-date information is available on the Renesas Technology Website.
- Datasheet
  M62050P/FP Datasheet
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