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H8/38099 Group

Using the TPU for Audio Output by PWM

Introduction

This application note describes an example of voice output by the 16-bit timer pulse unit (TPU) of an H8/38099F product in PWM operation.

Non-compressed 8-bit audio data, sampled at 8 kHz, are stored in the on-chip flash memory of the H8/38099F product.

Target Device

H8/38099F

Contents

1. Specification

(1) The 16-bit timer pulse unit (TPU) of the H8/38099F is used for output of a voice sound in PWM mode.
(2) Non-compressed 8-bit-length audio data (PCM data), sampled at 8 kHz, are stored in on-chip flash memory of the H8/38099F product.
(3) A low-pass filter and amplifier are externally connected to a PWM output pin (TIOCA1) to drive output of the voice sound from a speaker.
(4) Pressing the $\overline{\text{IRQ0}}$ pin interrupt switch starts output of the voice sound. The LED connected to the I/O port (P90 pin) lights up during audio output.
(5) A block diagram of the hardware for this sample task is shown in figure 1. In this sample task, audio output is realized by externally connecting an audio-output circuit (low-pass filter, amplifier, speaker, etc.) to the starter kit (RSKH838099-1) manufactured by Renesas Technology.

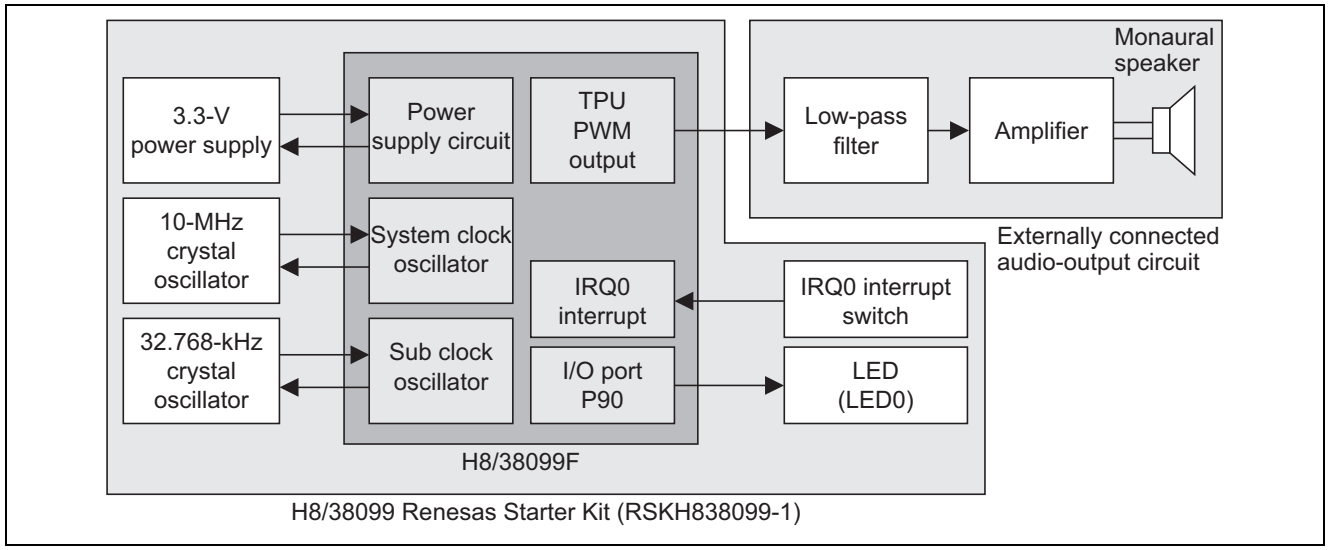

Figure 1 Block Diagram of Hardware

(6) When the switch connected to the $\overline{\text{IRQ0}}$ interrupt pin is pressed, the sound of a voice saying "Irasshaimase" is output. The specification of the audio data (PCM data) is shown in table 1.

Table 1 Specification of Audio Data (PCM)

Item	Description
Sample size	8 bits
Sampling frequency	8 kHz
Number of channels	1 (monaural)
Total playback time	0.97 sec
Total number of samples	7,769
Data size	7,769 bytes

(7) In this sample application, all modules are initialized after release from the reset state; the chip is then placed in watch mode. Pressing the switch connected to the $\overline{\text{IRQ0}}$ pin initiates a transition from watch mode to active mode (high-speed mode) in which audio output is performed. Once the audio output is completed, the chip reenters watch mode and again waits until the switch connected to the $\overline{\text{IRQ0}}$ pin is pressed. A state transition diagram for this sample task is given as figure 2.

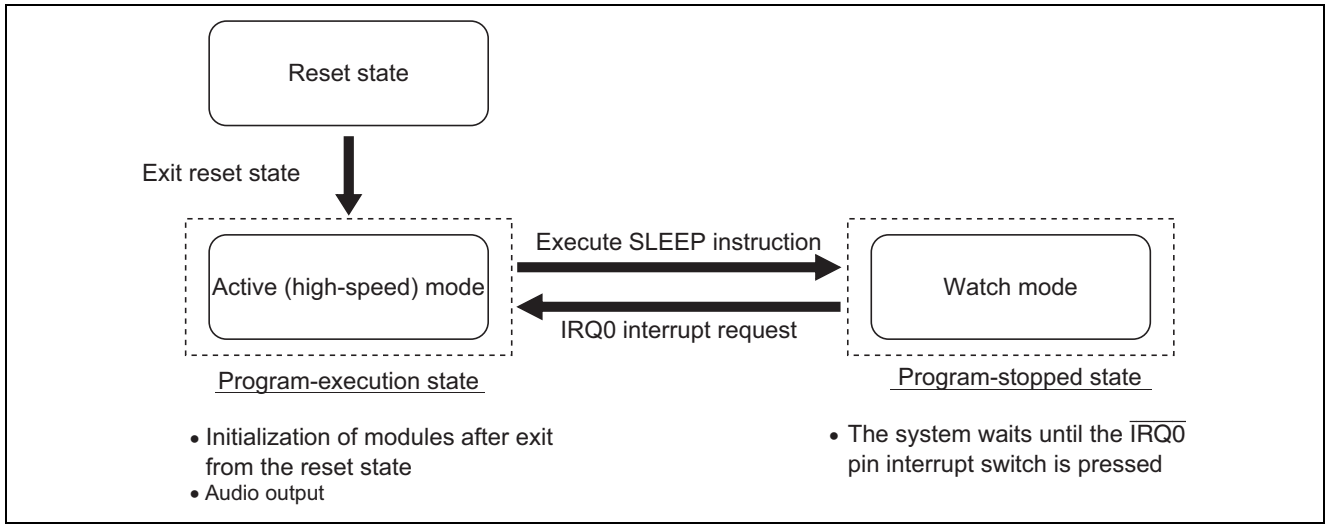

Figure 2 State Transition Diagram

2. Applicable Conditions

The applicable conditions for the H8/38099F product in this sample task are listed in table 2.

Table 2 Applicable Conditions

Item	Setting
System clock frequency	Crystal oscillator frequency: 10 MHz System clock (ϕ): 10 MHz
Sub clock frequency	Crystal oscillator frequency: 32.768 kHz Watch clock (ϕ_W): 32.768 kHz
Power supply voltage	Vcc = AVcc = 3.3 V

3. Description of Hardware

3.1 Audio Output Block

PWM waveforms generated by the 16-bit timer pulse unit (TPU) of the H8/38099F product are input to the operational amplifier via the low-pass filter. A speaker is connected to the output of the operational amplifier to handle audio output. Figure 3 is a diagram of the audio output circuit.

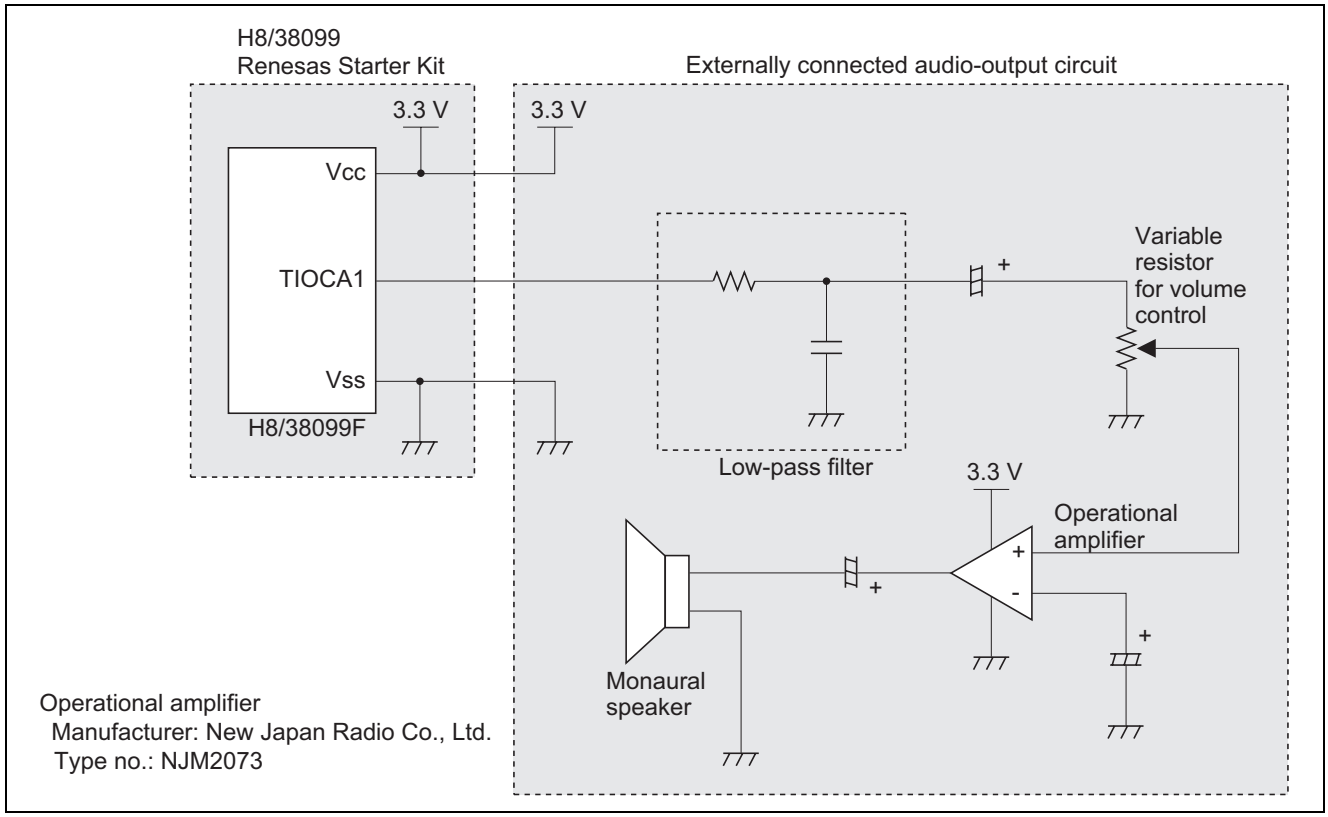

Figure 3 Circuit Diagram of Audio Output

3.2 $\overline{\text{IRQ0}}$ Pin Interrupt Switch

Figure 4 is a circuit diagram for the $\overline{\text{IRQ0}}$ interrupt switch connected to the $\overline{\text{IRQ0}}$ pin of the H8/38099F product. Pressing the switch releases the chip from watch mode, and initiates a transition to active mode (high-speed mode). Audio output is then performed in active mode.

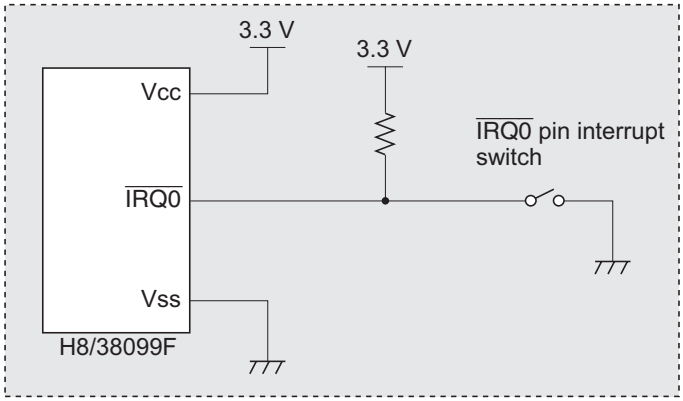

Figure 4 Circuit Diagram for the $\overline{\text{IRQ0}}$ Pin Interrupt Switch

3.3 LED Block

Figure 5 is a circuit diagram for the LED connected to the P90 pin of the H38099F product. When the output signal from the P90 pin switches to the high level, the LED light goes out. When the signal switches to the low level, the LED lights up.

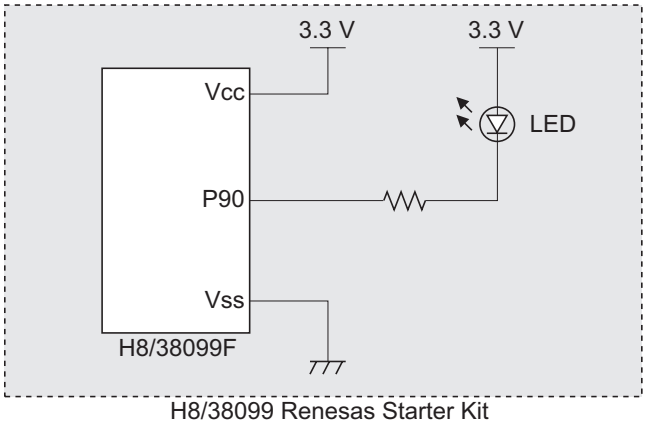

Figure 5 Circuit Diagram for the LED

4. Principles of Operation

4.1 Description of Audio-Output Operation

Figure 6 illustrates audio-output operation. On-chip peripheral modules are initialized in active mode (high-speed mode) after release from the reset state; the H8/38099F chip then enters watch mode. Pressing the $\overline{\text{IRQ0}}$-pin interrupt switch releases the chip from watch mode to perform audio output. The LED connected to the P90 pin lights up during audio output. Once the audio output is completed, the chip returns to watch mode and again waits until the $\overline{\text{IRQ0}}$-pin interrupt switch is pressed.

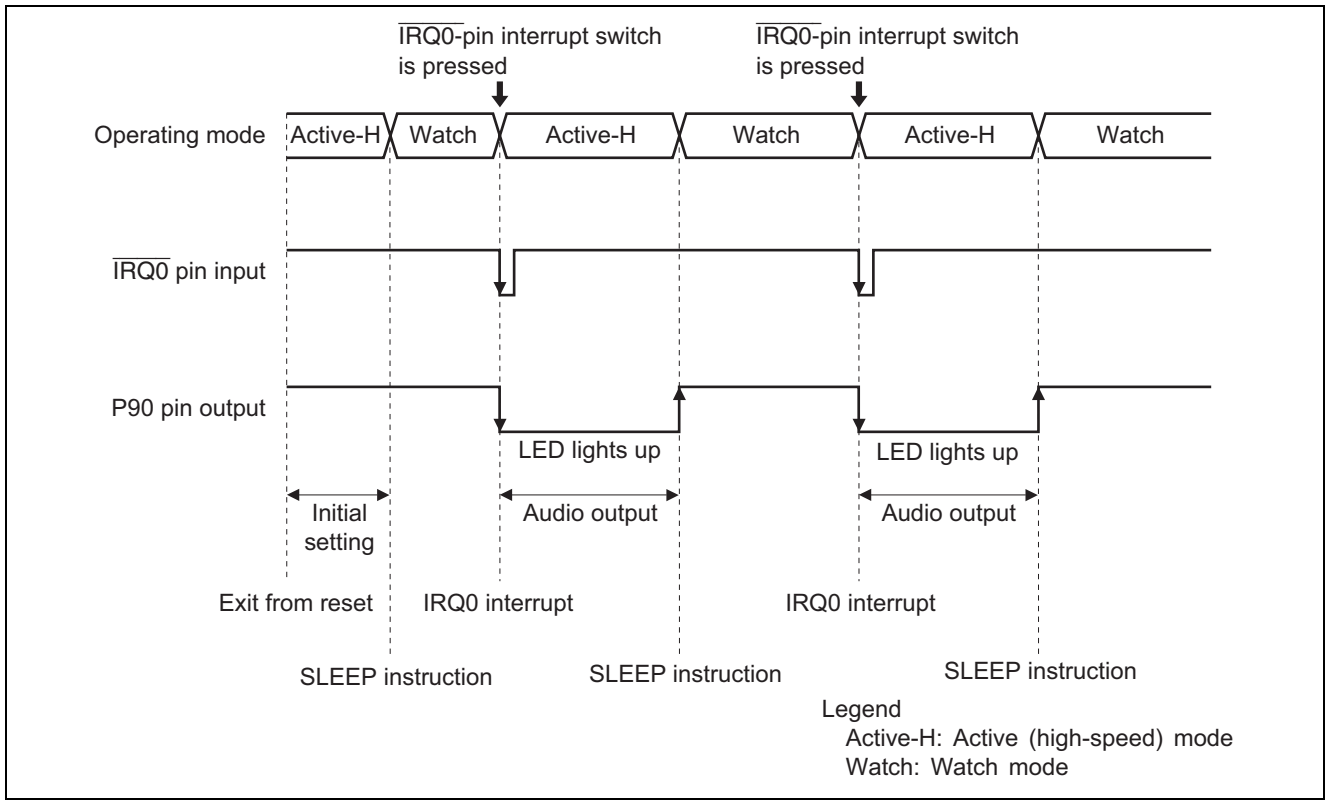

Figure 6 Audio-Output Operation

4.2 Description of PWM Output Operation by Using TPU

Figure 7 illustrates PWM output operation by the timer pulse unit (TPU) of the H8/38099F. In this sample application, channels 1 and 2 of the TPU are used to output PWM waveforms from the TIOCA1 pin. Channel 1 outputs a 40-kHz (39.0625-kHz) PWM waveform and channel 2 is used as an 8-kHz (7.8125-kHz) PWM timer.

Although the audio data in use were sampled at 8 kHz, setting the frequency of the PWM output waveform within the range of audible frequencies (20 Hz to 20 kHz) at 8 kHz will result in superposed noise (a tone) at 8 kHz. Therefore, channel 1 of the TPU is used to output a PWM waveform at 40-kHz (8 kHz x 5), i.e. out of the range of audible frequencies and at a multiple of the 8-kHz sampling frequency, from the TIOCA1 pin.

In the normal mode, the period of the signal on channel 2 is five times that of the signal on channel 1. Channel 2 is used to overwrite the audio data (duty cycle) of the PWM waveform for output from the TIOCA1 pin.

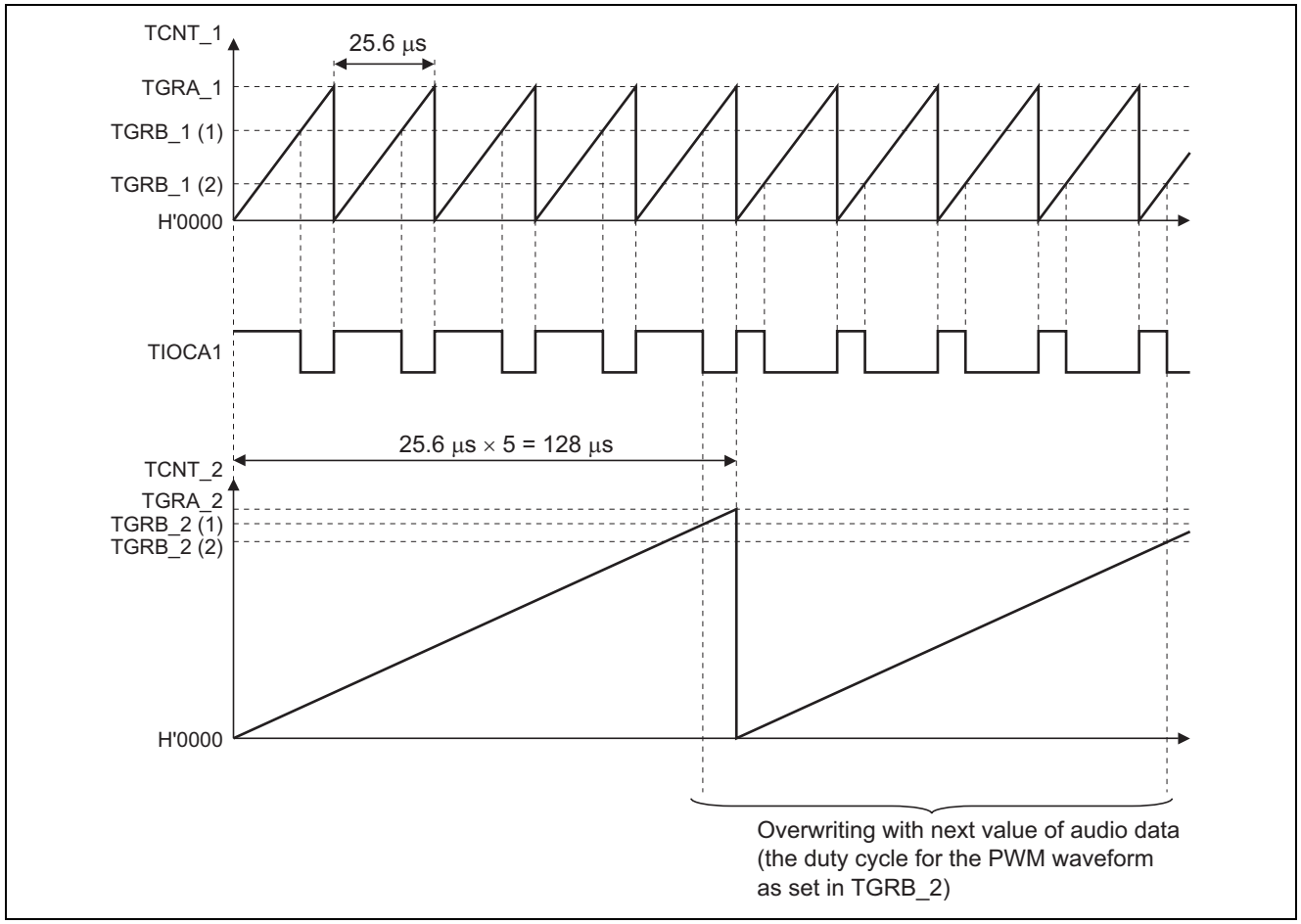

Figure 7 Operation of PWM Output by the TPU

(1) **Setting of TGRA_1 (Timer General Register A1)**

Timer general register A1 (TGRA_1) is used as the cycle register for the PWM waveform output from the TIOCA1 pin. The input clock for the timer counter 1 (TCNT_1) is set to ϕ. Since the sample size for the audio data is 8 bits, the TGRA_1 setting H'FF:

TGRA_1 = H'FF (8-bit size (256) - 1)

produces the following period for the PWM waveform output from the TIOCA1 pin.

$(1/(\phi)) \times 256 = 25.6\ \mu s$

(2) **Setting of TGRB_1 (Timer General Register B1)**

Timer general register B1 (TGRB_1) is used as the duty-cycle register for the PWM waveform output from the TIOCA1 pin. Settings for output of a PWM waveform from the TIOCA1 pin are initial output = 1, output on compare match with TGRA_1 = 1, and output on compare match with TGRB_1 = 0.

The duty-cycle setting in TGRB_1 is overwritten on a compare match with the TGRB_2 register of TPU_2.

TGRB_1 = (audio data - 1)

(3) **Setting of TGRA_2 (Timer General Register A2)**

Timer general register A2 (TGRA_2) is used as the cycle register for the PWM timer to drive overwriting of the audio data (duty-cycle) setting in TGRB_1. The setting is for a period five times that for a compare match with TGRA_1. Although the audio data in use were sampled at 8 kHz, setting the frequency of the PWM output waveform within the range of audible frequencies at 8 kHz will result in an audible sound at 8 kHz. Therefore, the period of the PWM waveform output from the TIOCA1 pin is set to 40 kHz (39.0625 kHz), i.e. five times the sampling frequency of 8 kHz, with updating of the audio data at 8 kHz.

TGRA_2 = ((8 bits (256)) × 5) – 1 = H'4FF

(4) **Setting of TGRB_2 (Timer General Register B2)**

Timer general register B2 (TGRB_2) is used as the duty-cycle register for the PWM timer to drive overwriting of the audio data (duty-cycle) setting in TGRB_1. The duty-cycle setting is for four cycles plus the duty cycle (4 cycles + duty cycle) of the 40-kHz (3.90625-kHz) PWM waveform output from the TIOCA1 pin.

TGRB_2 = ((8 bits (256) × 4) + (audio data)) - 1

(5) **Timing for Overwriting of Audio Data**

Figure 8 shows the timing for overwriting of the audio data (duty cycle).

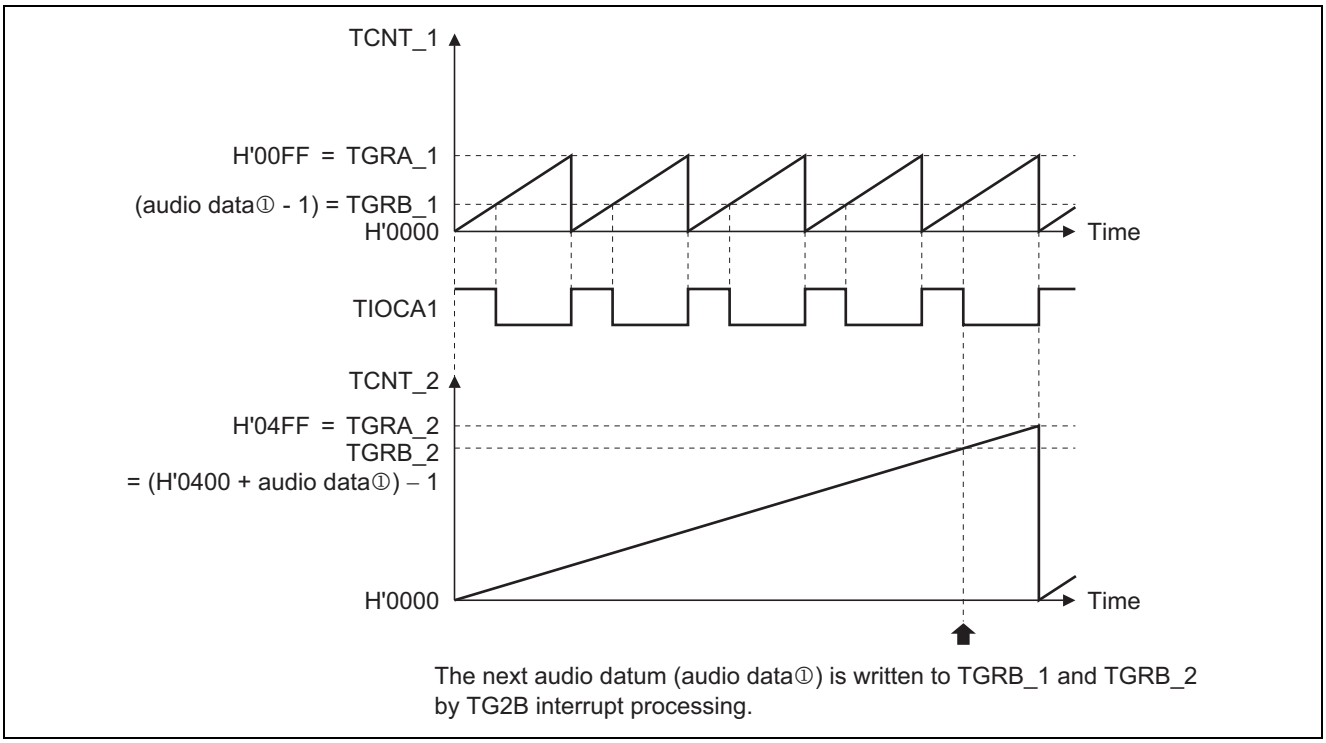

Figure 8 Timing for Overwriting of Audio Data

5. Description of Software

5.1 Operating Environment

Table 3 Operating Environment

Item	Description
Development tool	High-performance Embedded Workshop Ver.4.02.00.022
C/C++ complier	H8S, H8/300 SERIES C/C++ Compiler Ver.6.01.02
Complier options	-cpu = 300HA:24 -object = "$(CONFIGDIR)¥$(FILELEAF).obj" -debug -nolist -chgincpath -nologo

Table 4 Section Settings

Address	Section Name	Description
H'000000	CVECT	Vector table area
H'000100	P, C	Program area, constant area
H'FFF380	B	On-chip RAM area (non-initialized data area)

Table 5 Vector Table for Interrupt Exception Handling

Exception Handling Source	Vector No.	Address in Vector Table			Destination Interrupt Processing Function
$\overline{\text{RES}}$	0	H'000000	to	H'000003	main
Watchdog timer					
System reserved	1	H'000004	to	H'000007	main
System reserved	2	H'000008	to	H'00000B	main
NMI	3	H'00000C	to	H'00000F	main
System reserved	4	H'000010	to	H'000013	main
Address break	5	H'000014	to	H'000017	main
IRQ0	6	H'000018	to	H'00001B	int_irq0
IRQ1	7	H'00001C	to	H'00001F	main
IRQAEC	8	H'000020	to	H'000023	main
IRQ3	9	H'000024	to	H'000027	main
IRQ4	10	H'000028	to	H'00002B	main
WKP0	11	H'00002C	to	H'00002F	main
WKP1	12	H'000030	to	H'000033	main
WKP2	13	H'000034	to	H'000037	main
WKP3	14	H'000038	to	H'00003B	main
WKP4	15	H'00003C	to	H'00003F	main
WKP5	16	H'000040	to	H'000043	main
WKP6	17	H'000044	to	H'000047	main
WKP7	18	H'000048	to	H'00004B	main
RTC 0.25-second overflow	19	H'00004C	to	H'00004F	main
RTC 0.5-second overflow	20	H'000050	to	H'000053	main
RTC second periodic overflow	21	H'000054	to	H'000057	main
RTC minute periodic overflow	22	H'000058	to	H'00005B	main

Exception Handling Source	Vector No.	Address in Vector Table			Destination Interrupt Processing Function
RTC hour periodic overflow	23	H'00005C	to	H'00005F	main
RTC day periodic overflow	24	H'000060	to	H'000063	main
RTC week periodic overflow	25	H'000064	to	H'000067	main
RTC free-running overflow	26	H'000068	to	H'00006B	main
WDT overflow	27	H'00006C	to	H'00006F	main
AEC	28	H'000070	to	H'000073	main
TPU TG1A	29	H'000074	to	H'000077	main
TPU TG1B	30	H'000078	to	H'00007B	main
TPU TCI1V	31	H'00007C	to	H'00007F	main
TPU TG2A	32	H'000080	to	H'000083	main
TPU TG2B	33	H'000084	to	H'000087	int_tg2b
TPU TCI2V	34	H'000088	to	H'00008B	main
Timer FL	35	H'00008C	to	H'00008F	main
Timer FH	36	H'000090	to	H'000093	main
SCI4	37	H'000094	to	H'000097	main
SCI3_1	38	H'000098	to	H'00009B	main
SCI3_2	39	H'00009C	to	H'00009F	main
IIC2	40	H'0000A0	to	H'0000A3	main
10-bit A/D	41	H'0000A4	to	H'0000A7	main
Direct transition	42	H'0000A8	to	H'0000AB	main
System reserved	43	H'0000AC	to	H'0000AF	main
System reserved	44	H'0000B0	to	H'0000B3	main
System reserved	45	H'0000B4	to	H'0000B7	main
System reserved	46	H'0000B8	to	H'0000BB	main
System reserved	47	H'0000BC	to	H'0000BF	main
System reserved	48	H'0000C0	to	H'0000C3	main
System reserved	49	H'0000C4	to	H'0000C7	main
System reserved	50	H'0000C8	to	H'0000CB	main
System reserved	51	H'0000CC	to	H'0000CF	main
System reserved	52	H'0000D0	to	H'0000D3	main
Timer C	53	H'0000D4	to	H'0000D7	main
Timer G	54	H'0000D8	to	H'0000DB	main
SCI_3	55	H'0000DC	to	H'0000DF	main

5.2 List of Functions

Table 6 List of Functions

Function Name	Description
main	Main routine Specifies stack pointers, initializes on-chip peripheral modules, controls interrupts, the transition to watch mode, and the LED.
int_irq0	IRQ0 interrupt handling routine Clears interrupt request flags.
int_tg2b	TG2B interrupt handling routine Clears interrupt request flags and makes the duty-cycle settings in TGRB_1 and TGRB_2.
initialize	Initialization subroutine Initializes the watchdog timer, module standby mode, and I/O pins.
init_tpu	TPU initialization subroutine Initializes the TPU.

5.3 List of On-Chip RAM Areas in Use (Non-Initialized Data Area)

Table 7 List of On-Chip RAM Areas in Use

Data Type	Variable Name	Description	Address	Used in
unsigned short	voice_cnt	Counter for audio data	H'FFF380	main int_tg2b init_tpu

5.4 List of Constant Areas

Table 8 List of Constant Areas

Data Type	Constant Name	Description	Address	Data
Const unsigned short	DATA_SIZE	Audio data size	H'000276	H'1E59
Const unsigned char	VOICE_DATA [0]	Audio data (0)	H'000278	H'80
Const unsigned char	VOICE_DATA [1]	Audio data (1)	H'000279	H'80
		. . .		
Const unsigned char	VOICE_DATA [7767]	Audio data (7767)	H'0020CF	H'80
Const unsigned char	VOICE_DATA [7768]	Audio data (7768)	H'0020D0	H'80

5.5 Description of Functions

5.5.1 main Function (main routine)

1. Functional Overview
   This function specifies stack pointers, initializes on-chip peripheral modules, and controls interrupts, the transition to watch mode, starting of the TPU counters, and the LED.
2. Arguments
   None
3. Return value
   None

4. Flowchart

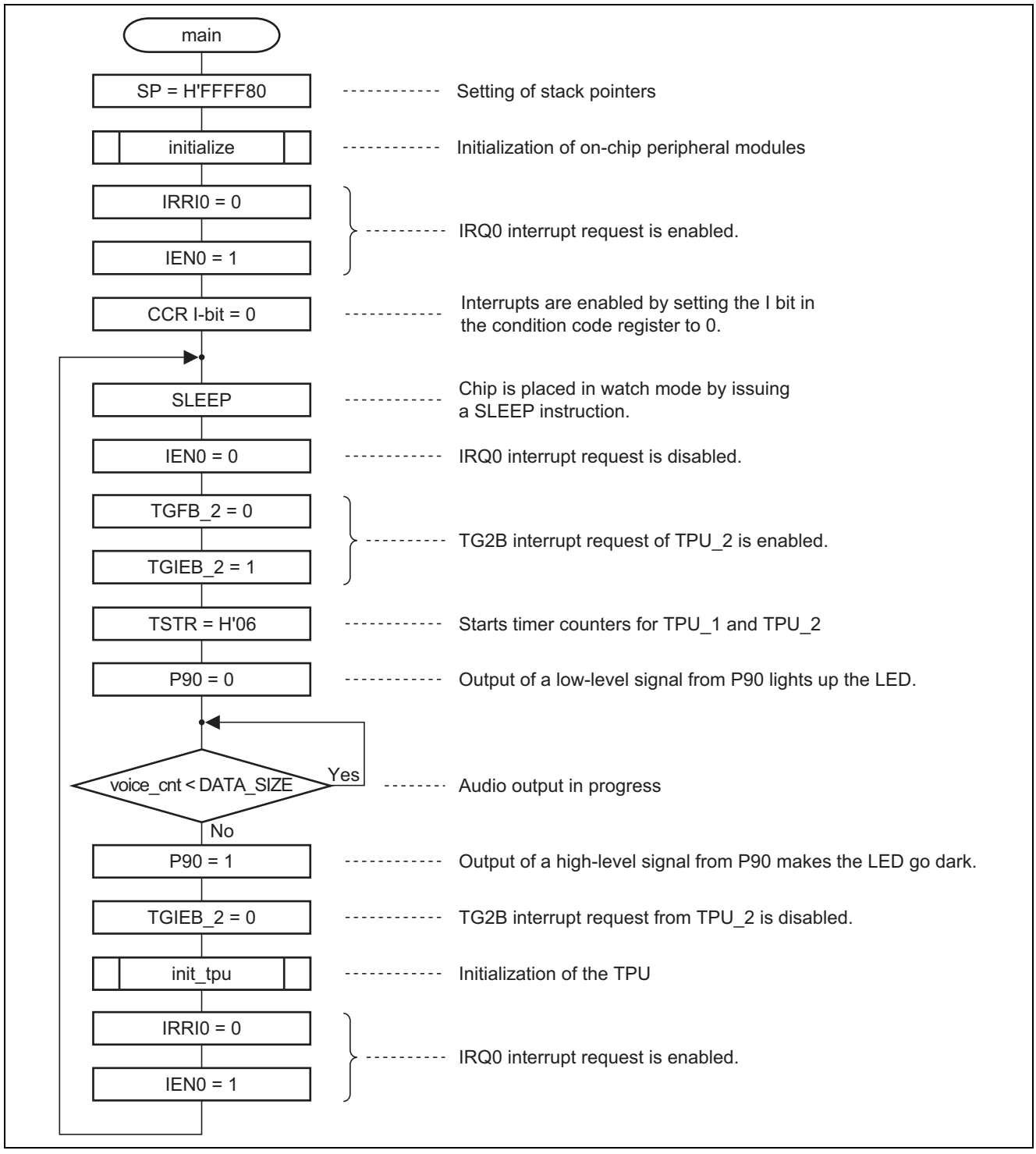

Figure 9 Flowchart of main Function

5.5.2 int_irq0 Function

1. Functional Overview
   IRQ0 interrupt handling routine; performs wait processing to eliminate chattering signal from the $\overline{\text{IRQ0}}$-pin interrupt switch, and clears the IRQ0 interrupt request flag.
2. Arguments
   None
3. Return value
   None
4. Flowchart

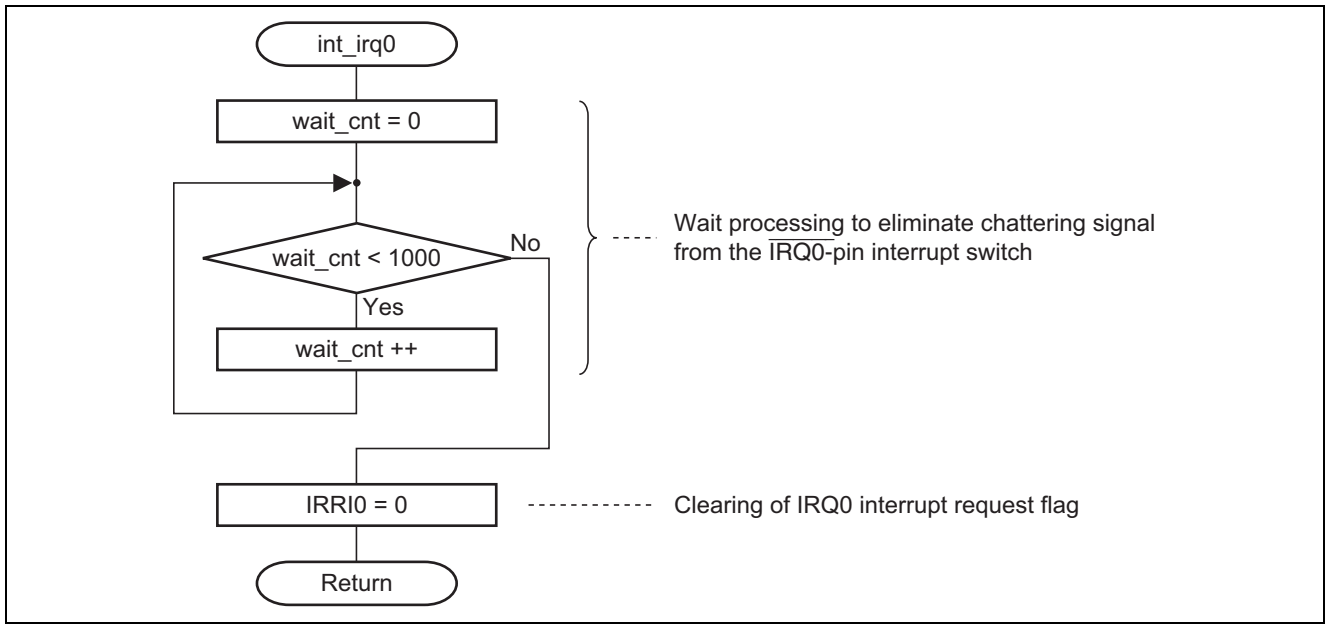

Figure 10 Flowchart of int_irq0 Function

5.5.3 int_tg2b Function

1. Functional Overview
   TG2B interrupt handling routine of TPU_2; clears the TG2B interrupt flag and makes audio-data (duty-cycle) settings in TGRB_1 and TGRB_2.
2. Arguments
   None
3. Return value
   None
4. Flowchart

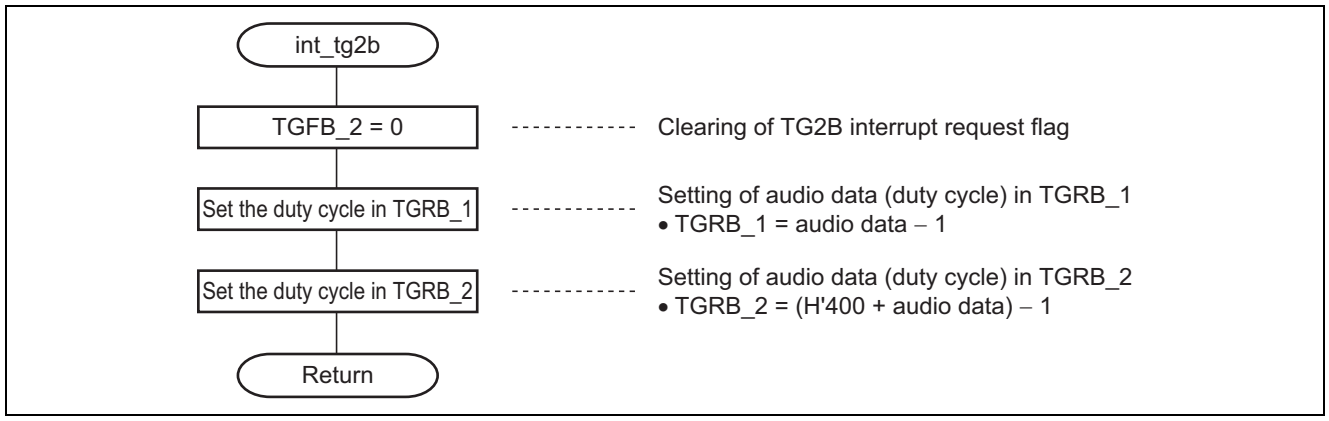

Figure 11 Flowchart of int_tg2b Function

5.5.4 initialize Function

1. Functional Overview
   This function halts the watchdog timer, makes settings for module standby mode and for initialization of the I/O pin (pin P90 connected to the LED), TPU, $\overline{\text{IRQ0}}$ pin, and the system control register for the transition to watch mode.
2. Arguments
   None
3. Return value
   None
4. Flowchart

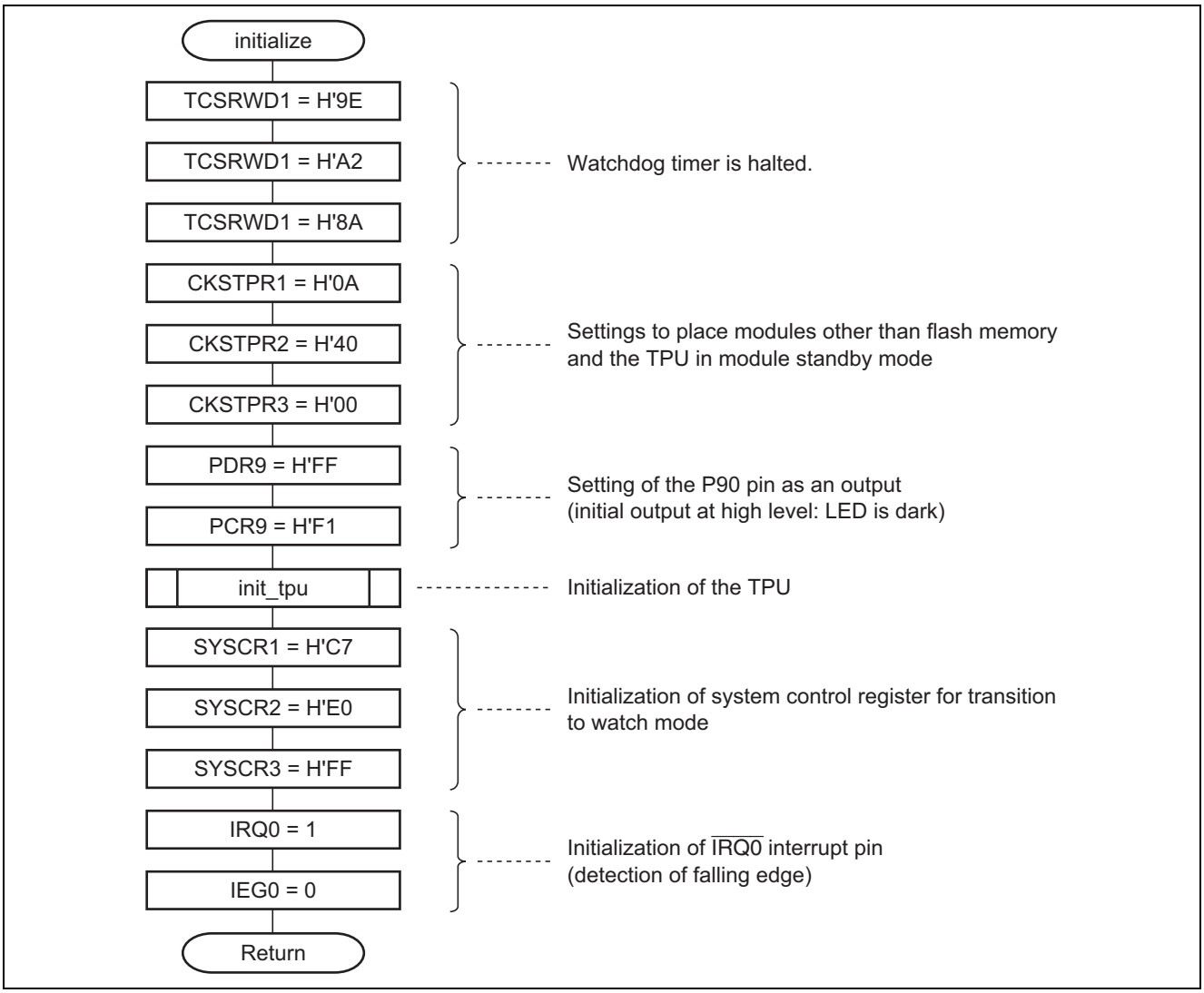

Figure 12 Flowchart of initialize Function

5.5.5 init_tpu Function

1. Functional Overview
   This function initializes the TPU.
2. Arguments
   None
3. Return value
   None
4. Flowchart

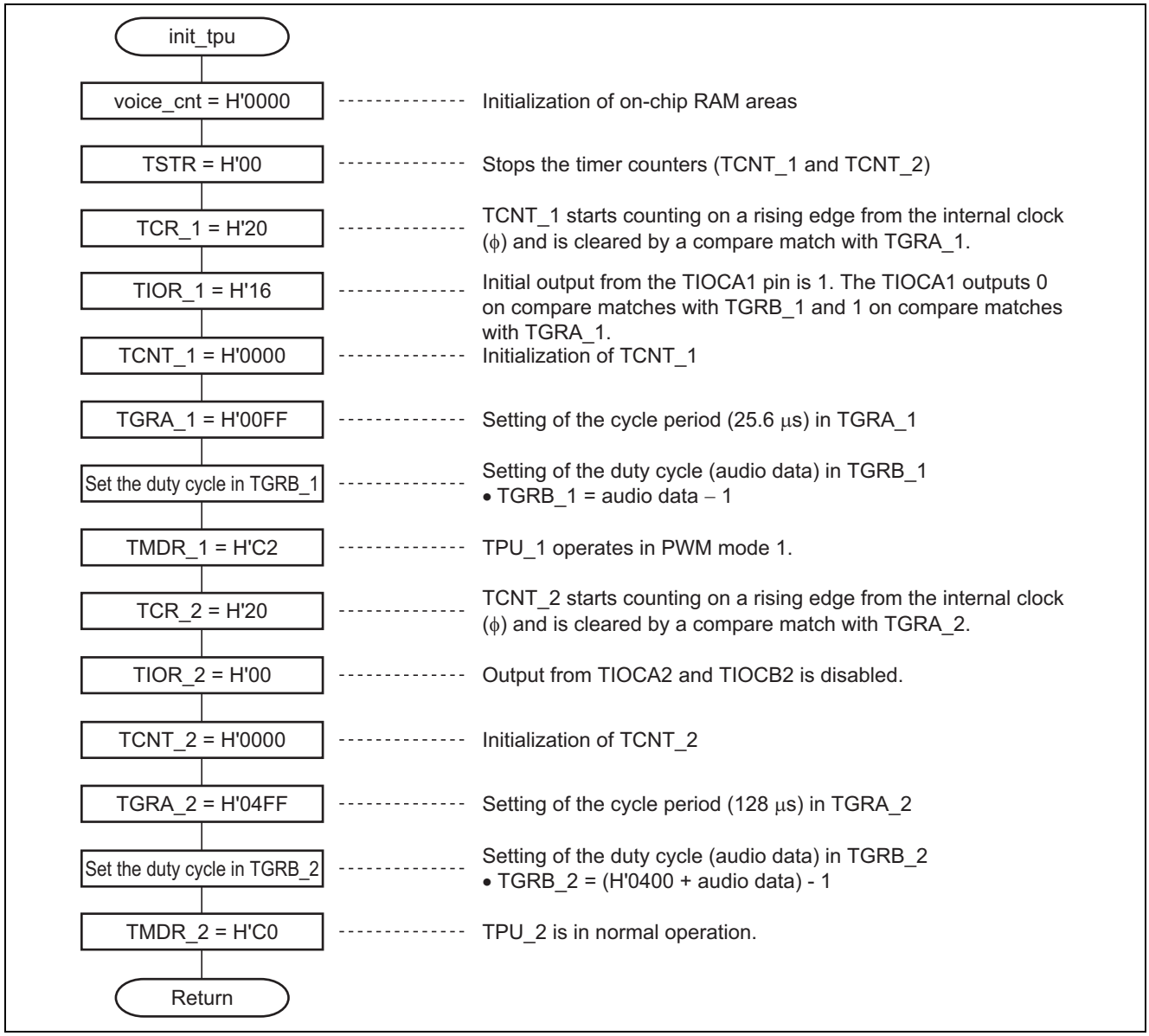

Figure 13 Flowchart of init_tpu Function

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