To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

Send any inquiries to http://www.renesas.com/inquiry.

H8SX Family

Using the DMAC to Drive Continuous SCI Transmission in Clock Synchronous Mode

Introduction

Clock synchronous transfer is used to transmit 128 bytes of data. Using the DMAC to handle the transfer (transmission) of data enables continuous transmission with no CPU intervention.

Target Device

H8SX/1653

Contents

1. Specification

Clock synchronous transfer is used to transmit 128 bytes of data. Using the DMAC to handle the transfer (transmission) of data enables continuous transmission with no CPU intervention.

- An example of connection for this sample task is shown in figure 1.
- Table 1 shows the communications format.
- After a power-on reset of the transmitting side, the SCI and DMAC modules are set up and the state of pin P13 is polled. When the P13 pin is a high level, the transmitting side judges the transfer is enabled at the receiving side, after which operations for the clock synchronous transmission of 128 bytes of data proceed.
- After a power-on reset of the receiving side, the SCI and DMAC functions are set up. The same side outputs a high-level signal on pin P13, after which operations for the clock synchronous reception of 128 bytes of data proceed in synchronization with the transmitting-side clock input on pin SCK.

In this sample task, the DMAC modules on each side are interrupt-activated to handle consecutive transmission of the 128 bytes of data.

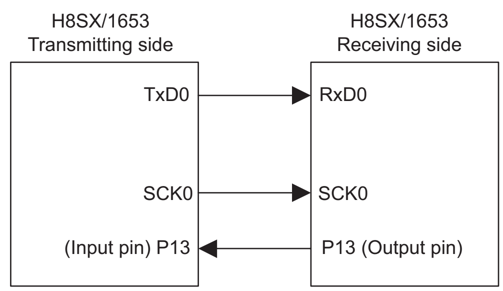


Figure 1 Clock Synchronous Serial Transmission

Table 1 Format for Clock Synchronous Serial Transmission

Format	Setting
Pϕ	32 MHz
Serial communications mode	Clock synchronous
Clock source	Internal clock
Transfer rate	250 kbps
Data length	8 bits
Serial/parallel conversion format	LSB first

2. Applicable Conditions

Table 2 Applicable Conditions

Item	Description	
Operating frequency	Input clock	:16 MHz
	System clock (Iϕ)	:32 MHz (input clock frequency × 2)
	Peripheral mode clock (Pϕ)	:32 MHz (input clock frequency × 2)
	External bus clock (Bϕ)	:32 MHz (input clock frequency × 2)
Mode of operation	Mode 6 (MD2 = 1, MD1 = 1, MD0 = 0, MD_CLK = 0)	

3. Description of Modules Used

3.1 Description in Outline

Peripheral modules of the H8SX/1653 which are used in this sample task are shown in Figure 2.

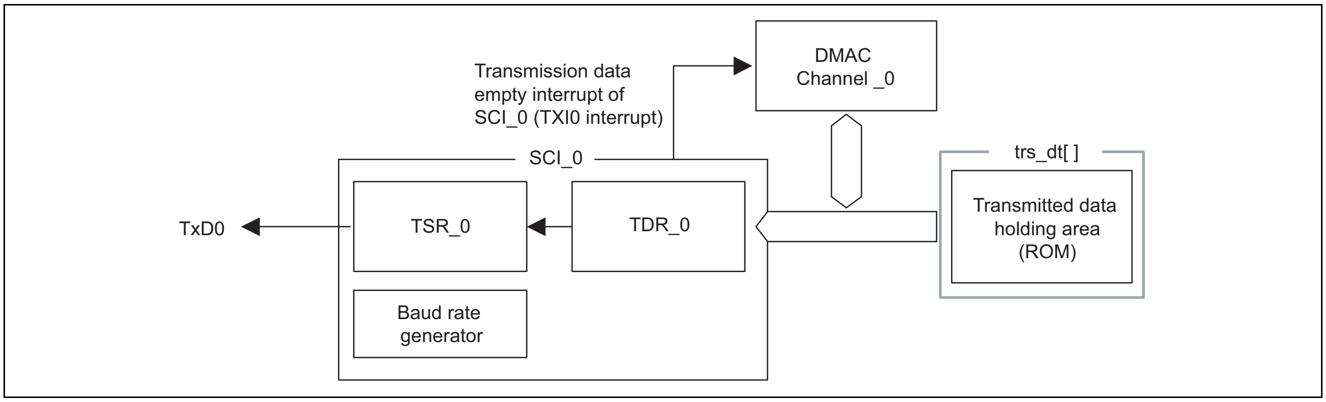


Figure 2 Functions of the H8SX/1653

The description which concerns the blocks shown in figure 2 is stated below.

1. SCI_0
   Transmits data with timing provided by the clock synchronous communications.
   - When TSR_0 is not full, data for transmission are written to TDR_0, transferred to TSR_0, and then output on the TxD0 pin.
   - When the data are transferred from TDR_0 to TSR_0, a transmission data empty interrupt (TXI0 interrupt) from SCI_0 is generated.

2. DMAC channel 0
   - Channel 0 is activated by the transmission data empty interrupt (TXI0 interrupt) from SCI_0 and transfers data from the area where data for transmission are stored to the TDR_0 register.

3.2 Description of SCI_0

In this sample task, SCI_0 is used for clock synchronous serial data transmission. Figure 3 is a block diagram of SCI_0.

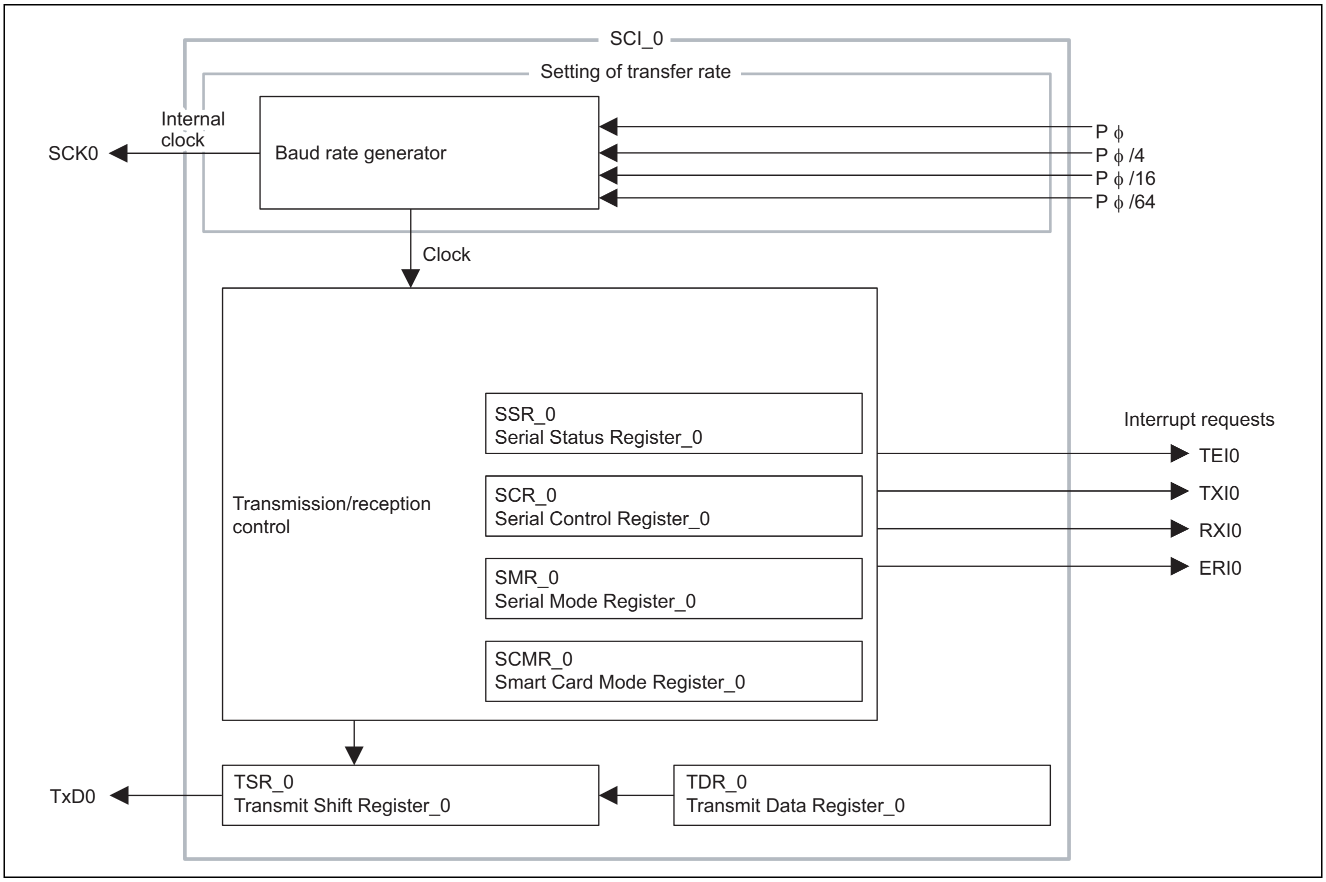


Figure 3 Block Diagram of SCI_0

The description which concerns the blocks shown in figure 3 is stated below.

- On-chip peripheral clock Pϕ
  This is the base clock for the operation of on-chip peripheral functions and is generated by a clock oscillator.

- Transmit shift register_0 (TSR_0)
  TSR_0 is used to transmit serial data. In transmission, data are transferred from the transmit data register (TDR_0) to TSR_0, and then output on the TxD0 pin. TSR_0 is not directly accessible from the CPU.

- Transmit data register_0 (TDR_0)
  TDR_0 is an 8-bit register and used to store data for transmission. When SCI_0 detects that TSR_0 is empty, data that have been written to TDR_0 are automatically transferred to TSR_0. Since TDR_0 and TSR_0 function as a double buffer, if the next data for transmission has already been written to TDR_0 when one frame of data is transmitted, the written data are transferred to TSR_0. This allows continual transmission. Although TDR_0 can be read from or written to by the CPU at all times, only write data for transmission data after having confirmed setting of the TDRE bit in the serial status register (SSR_0) to 1.

- Serial mode register_0 (SMR_0)
  SMR_0 is an 8-bit register and used to select the format of serial data communications and the clock source for the on-chip baud-rate generator.

- Serial control register_0 (SCR_0)
  SCR_0 is used to control transmission, reception, and interrupts, and to select the clock source for transmission and reception.

- Serial status register_0 (SSR_0)
  SSR_0 consists of status flags for SCI_0 and multiprocessor bits for transmission and reception. TDRE, RDRF, ORER, PER, and FER can only be cleared.

- Smart card mode register_0 (SCMR_0)
  SCMR_0 is used to select the smart-card or normal interface mode for SCMR_0, and to set up the format for the smart-card mode. For this task, the setting in SCMR_0 selects the normal asynchronous or clock synchronous mode.

- Bit rate register_0 (BRR_0)
  BRR_0 is an 8-bit register that is used to adjust the bit rate.

3.3 Channel 0 of the DMAC

In this sample task, DMAC channel 0 is activated by the TXI0 interrupt of SCI_0. A block diagram of the DMAC is given in figure 4.

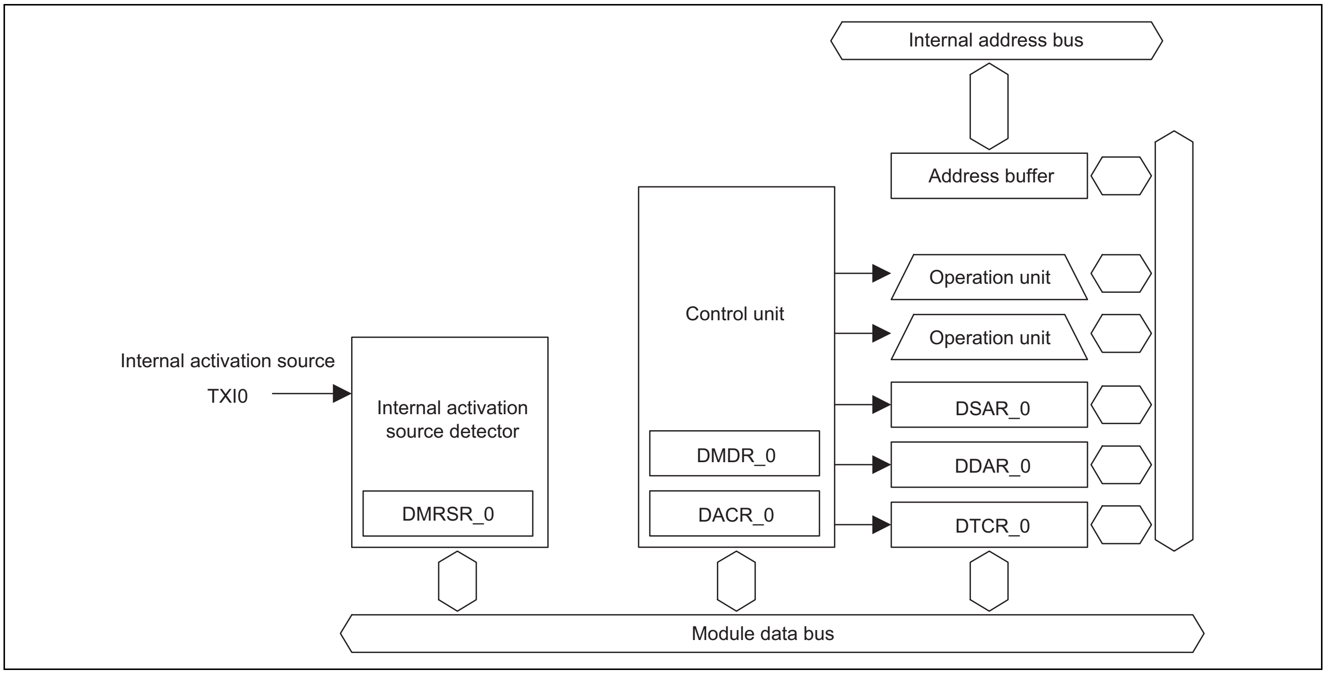


Figure 4 Block Diagram of the DMAC

The description with reference to figure 4 is stated below.

- DMA source address register _0 (DSAR_0)
  DSAR_0 is a 32-bit readable/writable register and specifies the source address for the transfer. The register is equipped with an address-updating function, so the source address is updated to that for the next transfer each time a transfer operation takes place.

- DMA destination address register _0 (DDAR_0)
  DDAR_0 is a 32-bit readable/writable register and specifies the destination address for the transfer. This register is equipped with an address-updating function, so the destination address is updated to that for the next transfer each time a transfer operation takes place.

- DMA transfer count register _0 (DTCR_0)
  DTCR_0 is a 32-bit readable/writable register and specifies the amount of data to be transferred (total size for transfer). After data transfer operation, the value is reduced by the amount that corresponds to the transferred amount of data. In this sample task, the register is set for 128 bytes of data, and the byte is selected as the unit of data access. One is subtracted from the value on DMAC operation, to indicate the amount still to be transferred.

- DMA mode control register _0 (DMDR_0)
  DMDR_0 controls DMAC operation.

- DMA address control register_0 (DACR_0)
  DACR_0 sets the operating mode and transfer method.

- DMA module request select register_0 (DMRSR_0)
  DMRSR_0 sets the activation source.

4. Principles of Operation

4.1 Outline

An outline of operation for this sample task is given in figure 5. 128-byte blocks of data are simultaneously transferred in both directions between the transmitting and receiving sides.

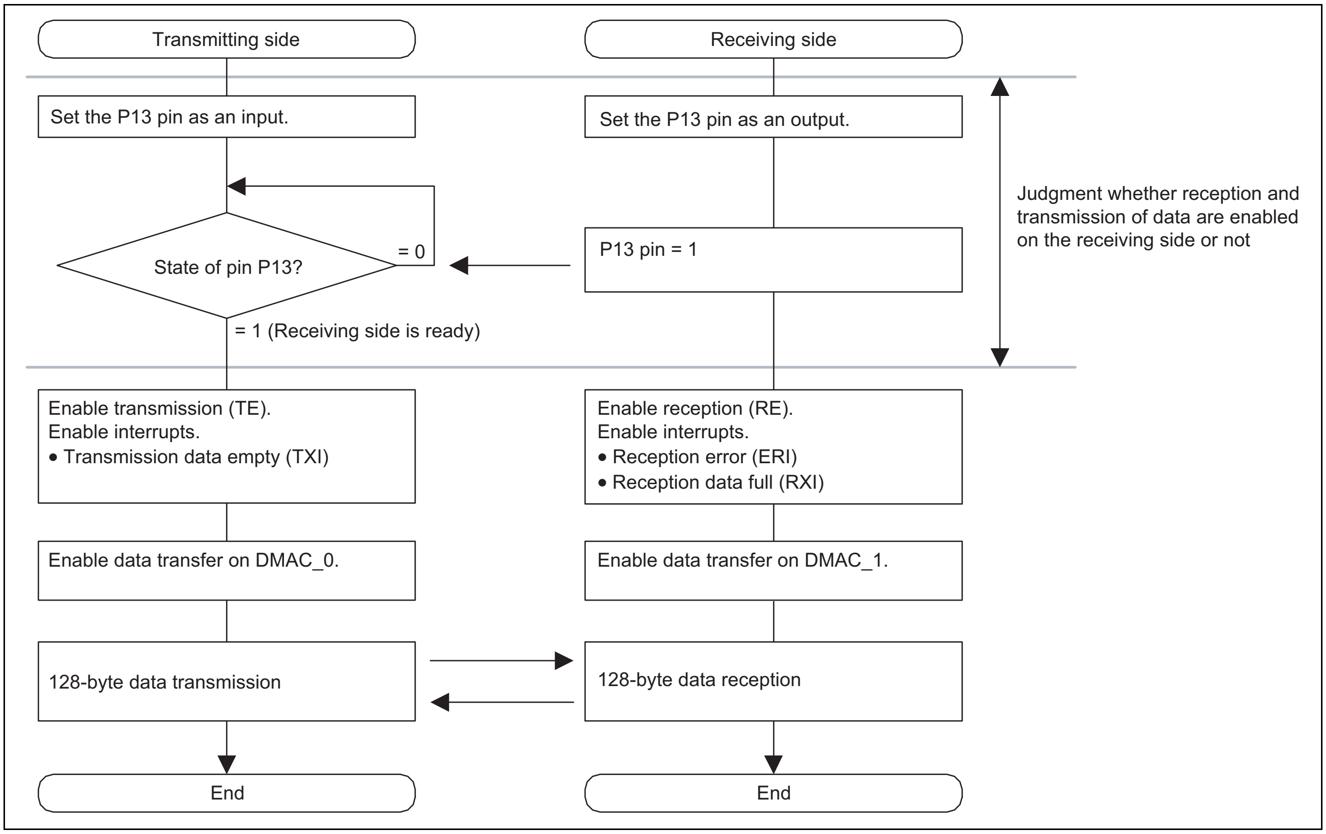


Figure 5 Outline of Operation

4.2 Transmission

4.2.1 Transmission Start

The timing of transmission start operations is illustrated in figure 6. Table 3 is a list of the hardware and software processing at the numbered points in figure 6.

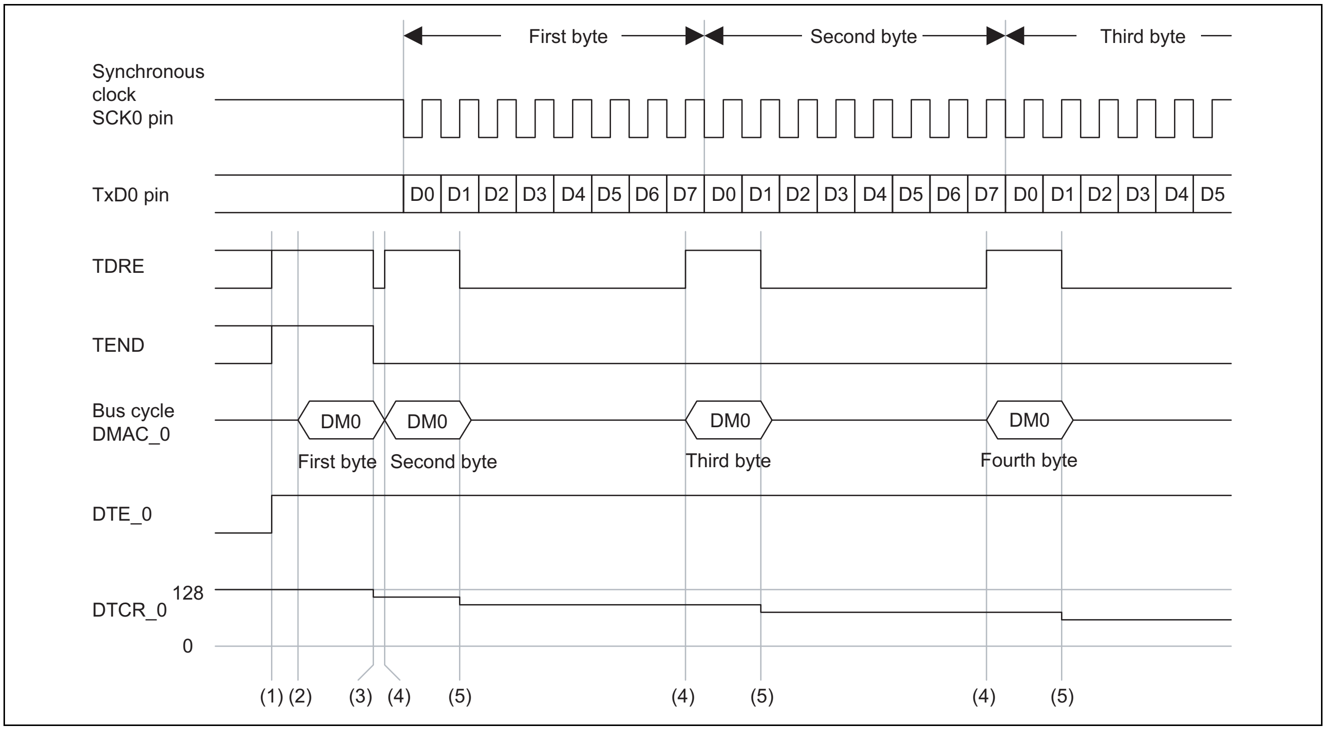


Figure 6 Timing of Transmission Start

Table 3 Processing

	Hardware Processing	Software Processing
(1)	Power-on reset	Initial settings*
(2)	a. Activate DMAC_0, and transfers data for transmission from the transmitted data holding area to TDR_0.	No processing
(3)	a. Clear TDRE to 0. b. DTCR_0 counts down. c. Transfer the contents of TDR_0 to TSR_0.	No processing
(4)	a. Set TDRE to 1. b. Activate DMAC_0 by TXI interrupt, and transfers data for transmission from the transmitted data holding area to TDR_0. c. Output the contents of data of TSR_0 on pin TxD0.	No processing
(5)	a. Clear TDRE to 0. b. DTCR_0 counts down. c. Transfer the contents of TDR_0 to TSR_0.	No processing

Notes: *Initial settings

DMAC_0 settings

a. Source for activation: TXI0 interrupt. The flag (TDRE) fro the TXI0 interrupt source is cleared on completion of the DMA transfer.
b. Source address: First address of the area where the data for transmission are stored. Incrementation is selected as the address incrementation or decrementation setting.
c. Destination address: Address of TDR_0. Fixed address is selected as the address incrementation or decrementation setting.
d. Total amount of transfer: 128 bytes
e. DMA data transfer is enabled (DTE_0 = 1).

SCR_0 settings

a. Clock synchronous mode. When Pϕ = 32 MHz, set the transfer rate to 250 kbps.
b. TXI0 interrupt requests are enabled.
c. Set SCI_0 to enable transmit operations.

4.2.2 Transmission End

The timing of end of transmission operations is illustrated in figure 7. Table 4 is a list of the hardware and software processing at the numbered points in figure 7.

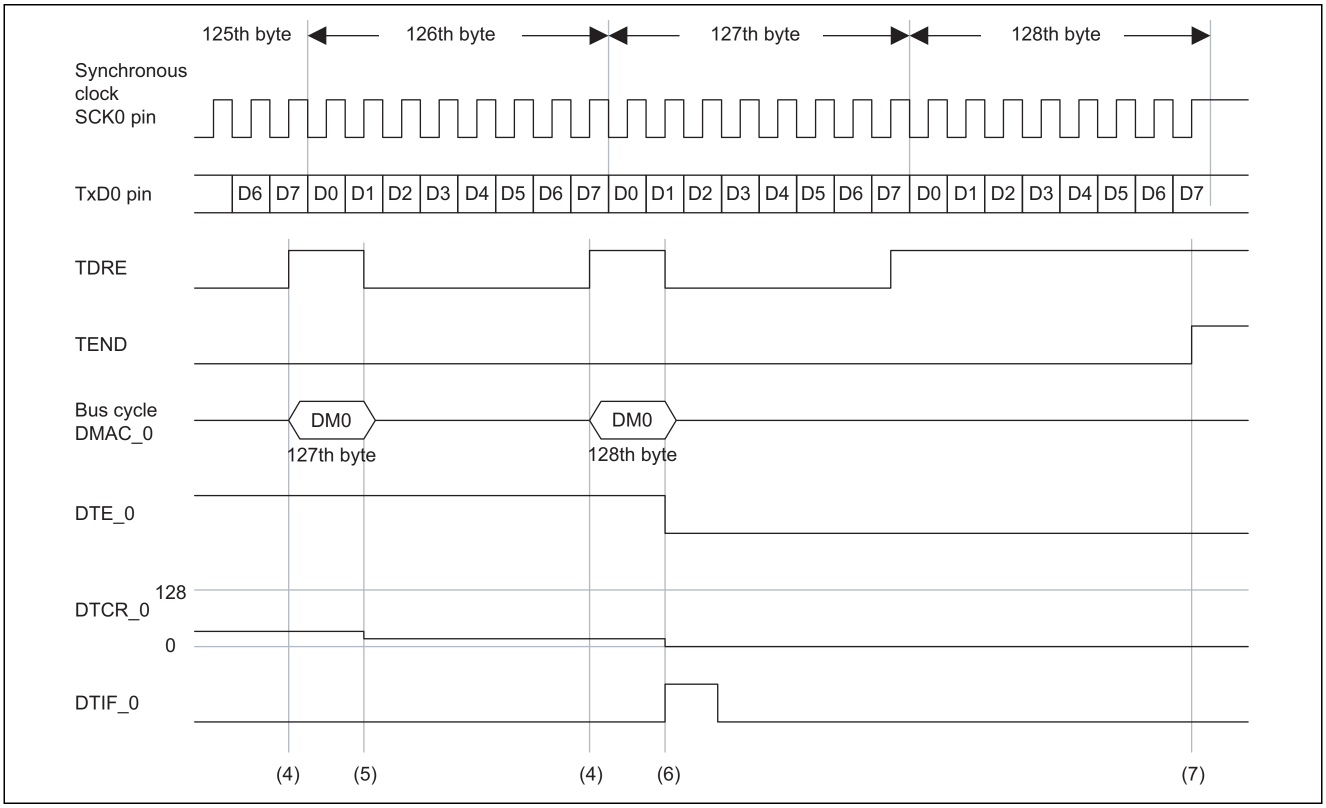


Figure 7 Timing of Transmission End

Table 4 Processing

	Hardware Processing	Software Processing
(4)	a. Set TDRE to 1. b. Activate DMAC_0 by TXI0 interrupt, and transfers data for transmission from the transmitted data holding area to TDR_0. c. Output the contents of TSR_0 on pin TxD0.	No processing
(5)	a. Clear TDRE to 0. b. DTCR_0 counts down. c. Transfer the contents of TDR_0 to TSR_0.	No processing
(6)	a. Clear TDRE to 0. b. DTCR_0 (DTCR_0 = 0) counts down. c. Transfer the contents of TDR_0 to TSR_0.	DMAC_0 transfer end interrupt a. Disable interrupt request. b. Disable DMAC_0 transfer end interrupt requests.
(7)	a. Set TEND to 1.	TEI0 Interrupt a. Stop SCI_0 transmission operations (TE = 0). b. Disable TEI0 interrupt requests.

5. Description of Software

5.1 Operating Environment

Table 5 Operating Environment

Item	Details
Development tool	High-performance Embedded Workshop Ver.4.01.01
C/C++ compiler	H8S, H8/300 Series C/C++ Compiler Ver.6.01.02 (manufactured by Renesas Technology)
Compiler options	-cpu = h8sxa:24:md, -code = machinecode, -optimize = 1, -regparam = 3, -speed = (register, shift, struct, expression)

Table 6 Section Setting

Address	Section Name	Description
H'001000	P	Program area
	C	Constant area
H'FF2000	B	Non-initialized data area (RAM area)

Table 7 Vector Table for Interrupt Exception Handling

Exception Handling Source		Vector No.	Vector Address	Function to Interrupt Destination
Reset		0	H'000000	init
DMAC_0	DMTEND0	128	H'000200	dmtend0_int
SCI_0	TEI0	147	H'00024C	tei0_int

5.2 List of Functions

Table 8 lists the functions used in this sample task. Figure 8 shows the structure of hierarchy.

Table 8 List of Functions

Function Name	Description
init	Initialization routine: Takes the chip out of module stop mode, performs clock settings, and calls the main function.
main	Main routine Selects clock synchronous SCI. Calls the DMAC0_trs_init function. Judges input of high-level signal on pin P13. Makes settings for transmission of 128 bytes of data.
DMAC0_trs_init	DMAC_0 initialization Selects TXI0-interrupt-triggered processing of transfer from the area where data for transmission are stored to TDR_0.
dmtend0_int	DMAC_0 transfer end interrupt Sets TEI0 interrupt request enabled, TXI0 interrupt and DMAC_0 transfer end interrupt requests disabled.
tei0_int	Transmission end interrupt Sets SCI_0 transmission and TEI0 interrupt requests disabled.

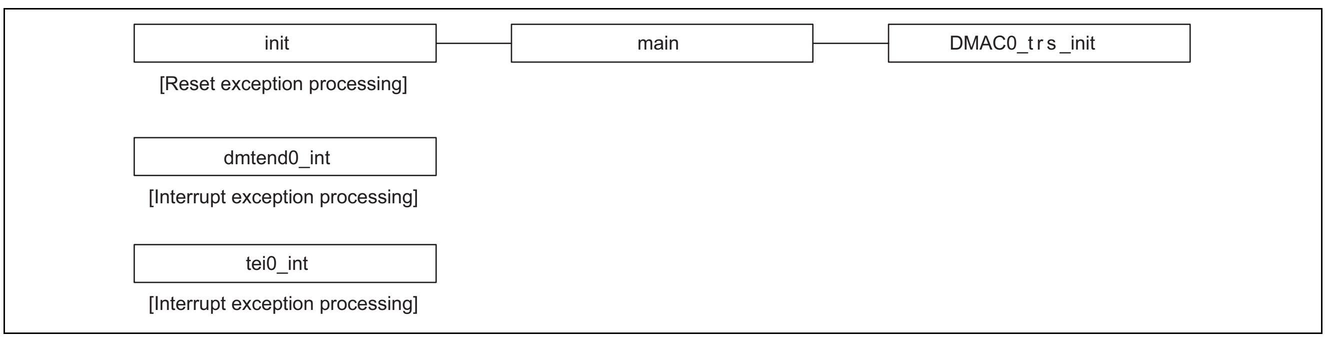


Figure 8 Hierarchy of Calls in the User Program

5.3 RAM Usage

Table 9 RAM Usage

Type	Variable Name	Description	Used in
unsigned char	endflg	Transmission end flag 0: Transmission in progress 1: Transmission ended	main, tei0_int
unsigned char	tcnt	Transmission counter	main, dmtend0_int

5.4 Constant

Table 10 Constants

Type	Variable Name	Setting	Description	Used in
unsigned char	trs_dt[128]	H’00, H’01, H’02, … ………H’7E, H’7F	Transmitted data holding area (ROM)	main, DMAC0_trs_init

5.5 Symbolic Constants

Table 11 Symbolic Constants

Constant Name	Setting	Description
NUM	128	Sets the number of data for transmission.

5.6 Description of Functions

5.6.1 init Function

1. Functional overview
   Initialization routine which releases the required modules from module stop mode, makes clock settings, and calls the main function.
2. Argument
   None
3. Return value
   None
4. Description of internal registers used
   The internal registers used in this sample task are described below. The settings shown in these tables are the values used in this sample task and differ from the initial values.

- Mode control register (MDCR) Number of bits: 16 Address: H'FFFDC0

Bit	Bit Name	Setting	R/W	Description
15	MDS7	Undefined*	R	Indicates the value set by a mode pin (MD3). When MDCR is read, the input level on the MD3 pin is latched. This latching is released by a reset.
11 10 9 8	MDS3 MDS2 MDS1 MDS0	Undefined* Undefined* Undefined* Undefined*	R R R R	Mode Select 3 to 0 These bits indicate the operating mode selected by the mode pins (MD2 to MD0) (see table 12). When MDCR is read, the signal levels input on pins MD2 to MD0 are latched into these bits. The latches are released by a reset.

Note: * Determined by the settings on pins MD3 to MD0.

Table 12 Settings of Bits MDS3 to MDS0

MCU Operating Mode	Mode Pins			MDCR			
	MD2	MD1	MD0	MDS3	MDS2	MDS1	MDS0
2	0	1	0	1	1	0	0
4	1	0	0	0	0	1	0
5	1	0	1	0	0	0	1
6	1	1	0	0	1	0	1
7	1	1	1	0	1	0	0

- System clock control register (SCKCR) Number of bits: 16 Address: H'FFFDC4

Bit	Bit Name	Setting	R/W	Description
10 9 8	ICK2 ICK1 ICK0	0 0 1	R/W R/W R/W	System Clock (Iϕ) Select These bits select the frequency of the system clock signal, which is provided to the CPU, DMAC, and DTC. 001: Input clock × 2
6 5 4	PCK2 PCK1 PCK0	0 0 1	R/W R/W R/W	Peripheral Module Clock (Pϕ) Select These bits select the frequency of the peripheral module clock. 001: Input clock × 2
2 1 0	BCK2 BCK1 BCK0	0 0 1	R/W R/W R/W	External Bus Clock (Bϕ) Select These bits select the frequency of the external bus clock. 001: Input clock × 2

- MSTPCRA, MSTPCRB, and MSTPCRC control module stop mode. Setting a bit to 1 places the corresponding module in module stop mode, while clearing the bit to 0 releases the module from module stop mode.

- Module stop control register A (MSTPCRA) Number of bits: 16 Address: H'FFFDC8

Bit	Bit Name	Setting	R/W	Description
15	ACSE	0	R/W	All-Module-Clock-Stop Mode Enable This bit enables/disables all-module-clock-stop mode for reducing current consumption by stopping the bus controller and I/O port operation when the CPU executes the SLEEP instruction after module stop mode has been set for all of the on-chip peripheral modules controlled by MSTPCR. 0: All-module-clock-stop mode disabled 1: All-module-clock-stop mode enabled
13	MSTPA13	0	R/W	DMA controller (DMAC)
12	MSTPA12	1	R/W	Data transfer controller (DTC)
9	MSTPA9	1	R/W	8-bit timer unit (TMR_3, TMR_2)
8	MSTPA8	1	R/W	8-bit timer unit (TMR_1, TMR_0)
5	MSTPA5	1	R/W	D/A converter (channels 1 and 0)
3	MSTPA3	1	R/W	A/D converter (unit 0)
0	MSTPA0	1	R/W	16-bit timer pulse unit (TPU channels 5 to 0)

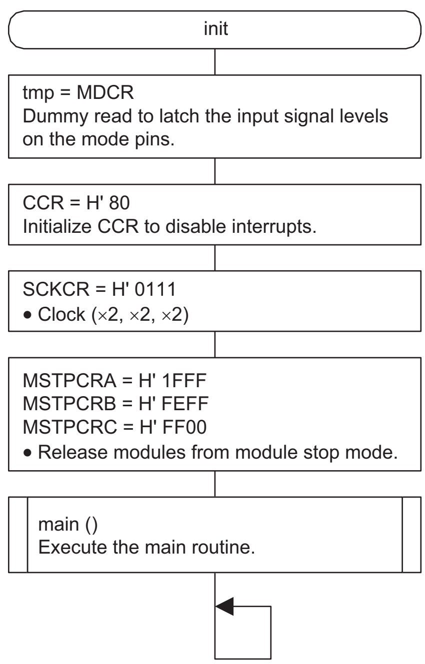
- Module stop control register B (MSTPCRB) Number of bits: 16 Address: H'FFFDCA

Bit	Bit Name	Setting	R/W	Description
15	MSTPB15	1	R/W	Programmable pulse generator (PPG)
12	MSTPB12	1	R/W	Serial communications interface_4 (SCI_4)
10	MSTPB10	1	R/W	Serial communications interface_2 (SCI_2)
9	MSTPB9	1	R/W	Serial communications interface_1 (SCI_1)
8	MSTPB8	0	R/W	Serial communications interface_0 (SCI_0)
7	MSTPB7	1	R/W	I^2C bus interface_1 (IIC_1)
6	MSTPB6	1	R/W	I^2C bus interface_0 (IIC_0)

- Module stop control register C (MSTPCRC) Number of bits: 16 Address: H'FFFDCC

Bit	Bit Name	Setting	R/W	Description
15	MSTPC15	1	R/W	Serial communications interface_5 (SCI_5), (IrDA)
14	MSTPC14	1	R/W	Serial communications interface_6 (SCI_6)
13	MSTPC13	1	R/W	8-bit timer unit (TMR_4, TMR_5)
12	MSTPC12	1	R/W	8-bit timer unit (TMR_6, TMR_7)
11	MSTPC11	1	R/W	Universal serial bus interface (USB)
10	MSTPC10	1	R/W	Cyclic redundancy check module
4	MSTPC4	0	R/W	On-chip RAM_4 (H'FF2000 to H'FF3FFF)
3	MSTPC3	0	R/W	On-chip RAM_3 (H'FF4000 to H'FF5FFF)
2	MSTPC2	0	R/W	On-chip RAM_2 (H'FF6000 to H'FF7FFF)
1	MSTPC1	0	R/W	On-chip RAM_1 (H'FF8000 to H'FF9FFF)
0	MSTPC0	0	R/W	On-chip RAM_0 (H'FFA000 to H'FFBFFF)

5. Flowchart



5.6.2 main Function

1. Functional overview
   Main routine: Sets the clock synchronous SCI, calls the DMAC0_trs_init function, judges input of high-level signal on pin P13, and sets transmission of 128 byte-data.
2. Argument
   None
3. Return value
   None
4. Description of internal registers used
   The internal registers used in this sample task are described below. The settings shown in these tables are the values used in this sample task and differ from the initial values.

- Port 1 data direction register (P1DDR) Number of bits: 8 Address: Address H’FFFB80

Bit	Bit Name	Setting	R/W	Description
3	P13DDR	0	W	0: Sets pin P13 as an input. 1: Sets pin P13 as an output.

- DMA mode control register_0 (DMDR_0) Number of bits: 32 Address: H’FFFC14

Bit	Bit Name	Setting	R/W	Description
31	DTE	1	R/W	Data Transfer Enable 0: Disables data transfer. 1: Enables data transfer.

- Port 1 register (PORT1) Number of bits: 8 Address: H’FFFF40

Bit	Bit Name	Setting	R/W	Description
3	P13PORT	Undefined	R	0: Pin P13 is set to a high level. 1: Pin P13 is set to a low level.

- Serial mode control register_0 (SMR_0) Number of bits: 8 Address: H’FFFF80

Bit	Bit Name	Setting	R/W	Description
7	C/$\overline{A}$	1	R/W	Communication Mode 0: Asynchronous 1: Clock synchronous
1 0	CKS1 CKS0	0 0	R/W R/W	Clock Select 1, 0 These bits select the clock source for the baud rate generator. 00: Pϕ clock (n = 0) For the relation between the settings of these bits and the baud rate, see section 14.3.9, Bit Rate Register (BRR) in the hardware manual. n is the decimal display of the value of n in BRR (see section 14.3.9, Bit Rate Register in the hardware manual).

- Bit rate register_0 (BRR_0) Number of bits: 8 Address: H'FFFF81
  Function: BRR_0 is used to adjust the bit rate. When Pϕ = 32 MHz, CKS1 and CKS2 in SMR_0 = B’00, and BRR_0 = 31 will set the bit rate to 250 kbps.
  Setting: 31

- Serial control register_0 (SCR_0) Number of bits: 8 Address: H'FFFF82

Bit	Bit Name	Setting	R/W	Description
7	TIE	0/1	R/W	Transmit Interrupt Enable 0: Disables TXI interrupt requests. 1: Enables TXI interrupt requests.
6	RIE	0	R/W	Receive Interrupt Enable 0: Disables RXI and ERI interrupt requests. 1: Enables RXI and ERI interrupt requests.
5	TE	0/1	R/W	Transmit Enable 0: Disables transmission. 1: Enables transmission.
4	RE	0	R/W	Receive Enable 0: Disables reception. 1: Enables reception.
2	TEIE	0/1	R/W	Transmit End Interrupt Enable 0: Disables TEI interrupt requests. 1: Enables TEI interrupt requests.
1 0	CKE1 CKE0	0 0	R/W	Clock Enable 1 and 0 Selects the clock source. When in clock synchronous mode; 0X: Internal clock. SCK pin is set as a clock output pin. 1X: External clock. SCK pin is set as a clock input pin.

Note X: Don't care.

- Serial status register_0 (SSR_0) Number of bits: 8 Address: H'FFFF84

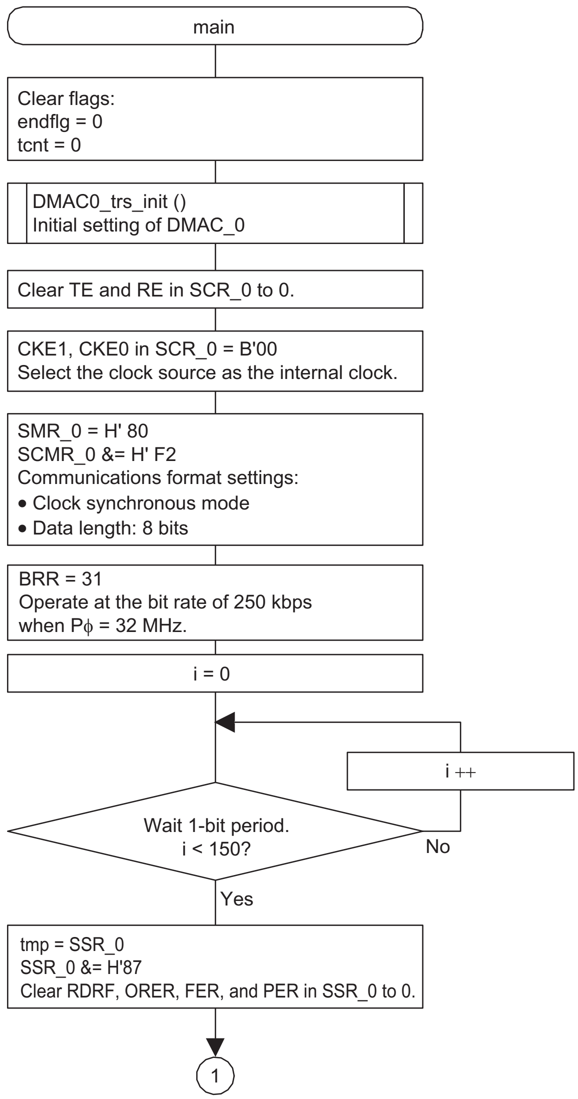
Bit	Bit Name	Setting	R/W	Description
7	TDRE	Undefined	R/(W)*	Transmit Data Register Empty Indicates whether TDR contains data for transmission. [Setting conditions] • Clearing of the TE bit in SCR to 0 • Transfer of data from TDR to TSR [Clearing conditions] • Writing of 0 to TDRE after having read TDRE = 1 (when using an interrupt and having the CPU clear it, be sure to read the flag after having written 0 to it). • Generation of a TXI interrupt request allowing DMAC to write transmit data to TDR
2	TEND	Undefined	R	Transmit End [Setting conditions] • Clearing of the TE bit in SCR to 0 • TDRE = 1 on transmission of the last bit of a character [Clearing conditions] • Writing of 0 to TDRE after having read TDRE = 1 • Generation of a TXI interrupt request allowing its value DMAC to write data to TDR

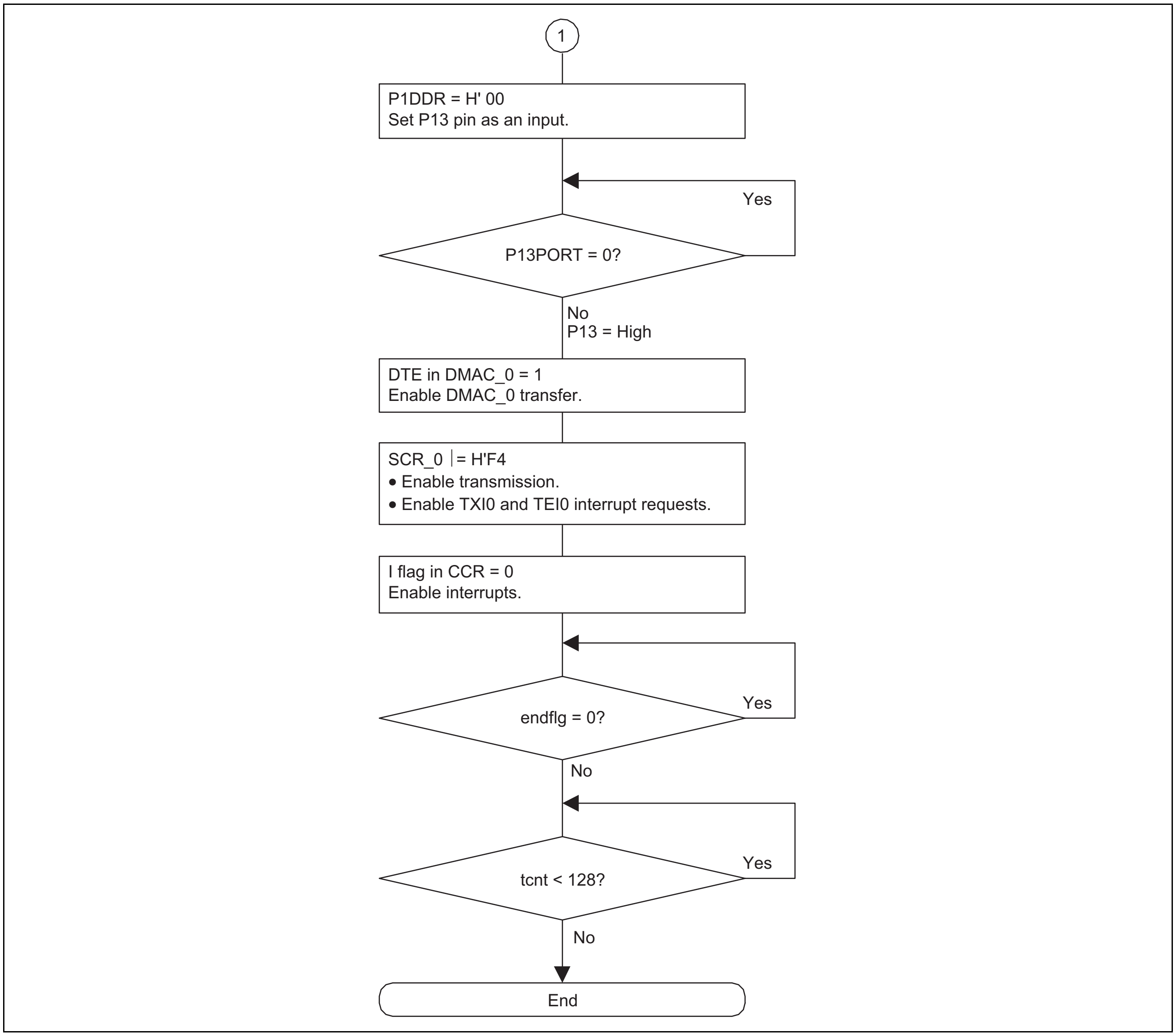
Note: * Only 0 can be written here, to clear the flag.

• Smart card mode register_0 (SCMR_0) Number of bits: 8 Address: H'FFFF86

Bit	Bit Name	Setting	R/W	Description
0	SMIF	0	R/W	Smart Card Interface Mode Select 0: Operation is in the normal asynchronous or clock synchronous mode. 1: Operation is in smart card interface mode.

5. Flowchart




1
P1DDR = H' 00
Set P13 pin as an input.
Yes
P13PORT = 0?
No
P13 = High
DTE in DMAC_0 = 1
Enable DMAC_0 transfer.
SCR_0 |= H'F4
• Enable transmission.
• Enable TXI0 and TEI0 interrupt requests.
I flag in CCR = 0
Enable interrupts.
Yes
endflg = 0?
No
Yes
tcnt < 128?
No
End

5.6.3 DMAC0_trs_init Function

1. Functional overview
   DMAC_0 initialization. Sets the transfer processing by TXI0 interrupts to TDR_0 from transmitted data holding area.
2. Argument
   None
3. Return value
   None
4. Description of internal registers used
   The internal registers used in this sample task are described below. The settings shown in these tables are the values used in this sample task and differ from the initial values.

- DMA source address register_0 (DSAR_0) Number of bits: 32 Address: H'FFFC00
  Function: DSAR_0 specifies the source address for the transfer.
  Setting: &trs_dt

- DMA destination address register_0 (DDAR_0) Number of bits: 32 Address: H'FFFC04
  Function: DDAR_0 specifies the destination address for the transfer.
  Setting: &TDR_0

- DMA transfer count register_0 (DTCR_0) Number of bits: 32 Address: H'FFFC0C
  Function: DTCR_0 sets the amount of data to be transferred (total amount for transfer).
  Setting: 128

- DMA mode control register_0 (DMDR_0) Number of bits: 32 Address: H'FFFC14

Bit	Bit Name	Setting	R/W	Description
31	DTE	0	R/W	Data Transfer Enable 0: Disables data transfer. 1: Enables data transfer.
26	NRD	0	R/W	Next Request Delay 0: Starts accepting the next transfer request after completion of the current transfer. 1: Starts accepting the next transfer request one cycle after completion of the current round of transfer.
17	ESIF	0	R/(W)*	Transfer Escape Interrupt Flag 0: A transfer escape end interrupt request has not been issued. 1: A transfer escape end interrupt request has been issued.
16	DTIF	0	R/(W)*	Data Transfer Interrupt Flag 0: A transfer end interrupt request by the transfer counter has not been issued. 1: A transfer end interrupt request by the transfer counter has been issued.
15 14	DTSZ1 DTSZ0	0	R/W R/W	Data Access Size 1 and 0 00: Data access size for transfer is in bytes (8 bits).
13 12	MDS1 MDS0	0	R/W R/W	Transfer Mode Select 1 and 0 00: Sets the normal transfer mode.

Bit	Bit Name	Setting	R/W	Description
9	ESIE	0	R/W	Transfer Escape interrupt Enable 0: Disables transfer escape interrupt requests. 1: Enables transfer escape interrupt requests.
8	DTIE	1	R/W	Data Transfer End Interrupt Enable 0: Disables transfer end interrupt requests. 1: Enables transfer end interrupt requests.
7 6	DTF1 DTF0	1 0	R/W R/W	Data Transfer Factor 1 and 0 10: DMAC activation source is an on-chip module interrupt.
5	DTA	1	R/W	Data Transfer Acknowledge When DTF 1 and DTF 0 = H'10, which selects execution of DMA transfer in response to an internal module interrupt, this bit enables or disables clearing of the source flag selected by DMRSR. 0: Source flag for the internal module interrupt is not cleared. 1: Source flag for the internal module interrupt is cleared.

Note: * Only 0 can be written here, to clear the flag.

- DMA address control register_0 (DACR_0) Number of bits: 32 Address: H’FFFC18

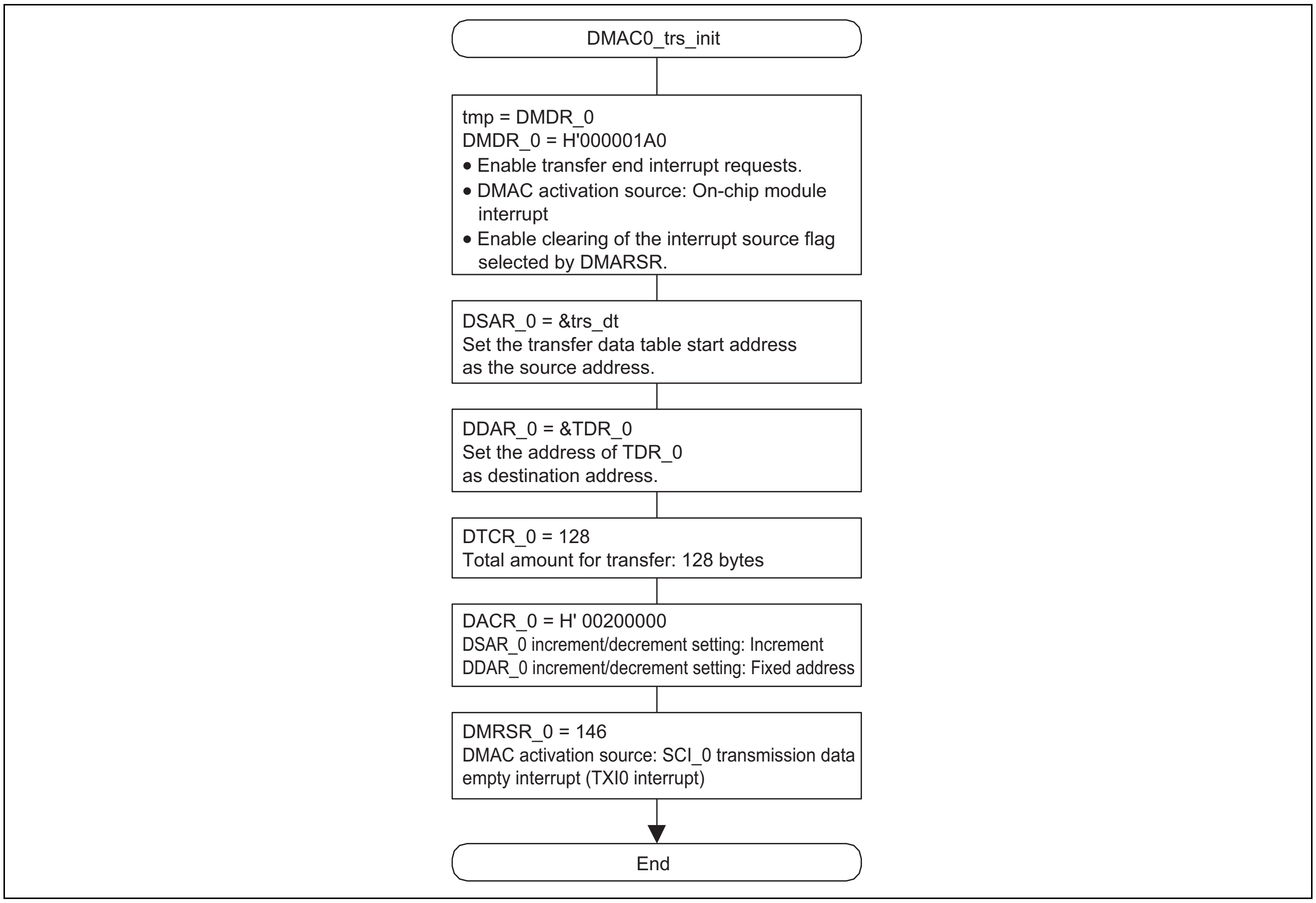
Bit	Bit Name	Setting	R/W	Description
31	AMS	0	R/W	Address Mode Select 0: Dual address mode 1: Single address mode
21 20	SAT1 SAT0	1 0	R/W R/W	Source Address Update Mode 1 and 0 10: Increment the source address.
17 16	DAT1 DAT0	0 0	R/W R/W	Destination Address Update Mode 1 and 0 00: Destination address is fixed.

- DMA module request select register_0 (DMRSR_0) Number of bits: 8 Address: H'FFFD20

  Function: DMRSR_0 specifies the source of on-chip module interrupts. The setting 146 corresponds to DMAC activation by SCI_0 transmission data empty interrupts (TXI0 interrupts).

  Setting: 146

5. Flowchart


DMAC0_trs_init
tmp = DMDR_0
DMDR_0 = H'000001A0
• Enable transfer end interrupt requests.
• DMAC activation source: On-chip module interrupt
• Enable clearing of the interrupt source flag selected by DMARSR.
DSAR_0 = &trs_dt
Set the transfer data table start address as the source address.
DDAR_0 = &TDR_0
Set the address of TDR_0 as destination address.
DTCR_0 = 128
Total amount for transfer: 128 bytes
DACR_0 = H' 00200000
DSAR_0 increment/decrement setting: Increment
DDAR_0 increment/decrement setting: Fixed address
DMRSR_0 = 146
DMAC activation source: SCI_0 transmission data empty interrupt (TXI0 interrupt)
End

5.6.4 dmtend0_int Function

1. Functional overview
   Handler for the DMAC_0 transfer end interrupt. Sets TEI0 interrupt requests enabled, TXI0 interrupt requests disabled, and DMAC_0 transfer end interrupt requests disabled.
2. Argument
   None
3. Return value
   None
4. Description of internal registers used
   The internal registers used in this sample task are described below. The settings shown in these tables are the values used in this sample task and differ from the initial values.

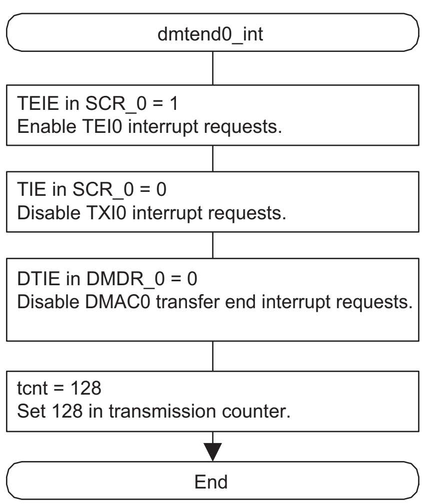
- Serial control register_0 (SCR_0) Number of bits: 8 Address: H'FFFF82

Bit	Bit Name	Setting	R/W	Description
7	TIE	0	R/W	Transmit Interrupt Enable 0: Disables TXI interrupt requests. 1: Enables TXI interrupt requests.
2	TEIE	1	R/W	Transmit End Interrupt Enable 0: Disables TEI interrupt requests. 1: Enables TEI interrupt requests.

- DMA mode control register_0 (DMDR_0) Number of bits: 32 Address: H'FFFC14

Bit	Bit Name	Setting	R/W	Description
8	DTIE	0	R/W	Data Transfer End Interrupt Enable 0: Disables transfer end interrupt requests. 1: Enables transfer end interrupt requests.

5. Flowchart



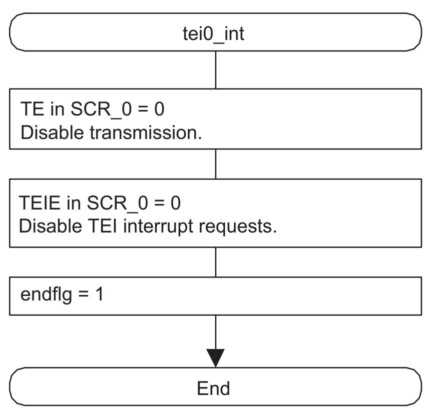
5.6.5 tei0_int Function

1. Functional overview
   Handler for SCI_0 transmission end interrupts (TEI0 interrupt). Sets to SCI_0 transmission and TEI0 interrupt requests disabled.
2. Argument
   None
3. Return value
   None
4. Description of internal registers used
   The internal registers used in this sample task are described below. The settings shown in these tables are the values used in this sample task and differ from the initial values.

- Serial control register_0 (SCR_0) Number of bits: 8 Address: H'FFFF82

Bit	Bit Name	Setting	R/W	Description
5	TE	0	R/W	Transmit Enable 0: Disables transmission. 1: Enables transmission.
2	TEIE	0	R/W	Transmit End Interrupt Enable 0: Disables TEI interrupt requests. 1: Enables TEI interrupt requests.

5. Flowchart



6. Documents for Reference (Note)

- Hardware Manual
  H8SX/1653 Group Hardware Manual
  The most up-to-date version of this document is available on the Renesas Technology Website.

- Technical News/Technical Update
  The most up-to-date information is available on the Renesas Technology Website.

Website and Support

Renesas Technology Website
http://www.renesas.com/

Inquiries
http://www.renesas.com/inquiry
csc@renesas.com

Revision Record

Rev.	Date	Description	
		Page	Summary
1.00	Aug.23.07	—	First edition issued