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H8SX Family

Using the DMAC to Drive Continuous SCI Transmission and Reception in Asynchronous Mode

Introduction

Asynchronous transfer is used to transmit and receive 128 bytes of data. Using the DMAC to handle the transfer (transmission and reception) of data enables continuous transmission and reception with no CPU intervention.

Target Device

H8SX/1653

Contents

1. Specification

- Asynchronous transfer is used to transmit and receive 128 bytes of data. Using the DMAC to handle the transfer (transmission and reception) of data enables continuous transmission and reception with no CPU intervention.
- An example of connection for this sample task is shown in figure 1.
- Table 1 shows the communications format.
- After a power-on reset of the master side, the SCI and DMAC modules are set up. The same side outputs a high-level trigger on pin P13, after which operations for the asynchronous transmission and reception of 128 bytes of data proceed.
- After a power-on reset of the slave side, the SCI and DMAC modules are set up and the state of pin P13/$\overline{\text{IRQ3}}$ is polled. When a high-level trigger is input on this pin, the slave side starts operations for the asynchronous transmission and reception of 128 bytes of data.
- In this sample task, the DMAC modules on each side are interrupt-activated to asynchronously handle transmission and reception of the 128 bytes of data.

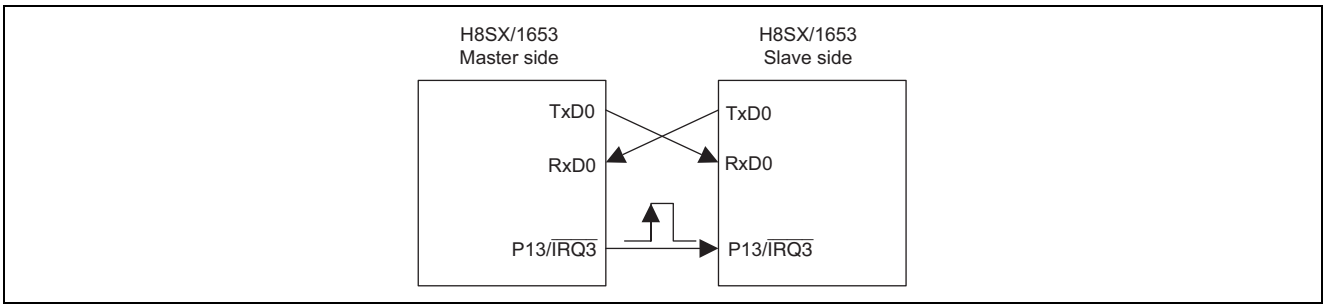


Figure 1 Asynchronous Serial Transmission and Reception

Table 1 Format for Asynchronous Serial Transmission and Reception

Format	Setting
Pϕ	32 MHz
Serial communications mode	Asynchronous
Clock source	Internal baud rate generator
Transfer rate	38,400 bps
Data length	8 bits
Parity bit	None
Stop bit	1 bit
Serial/parallel conversion format	LSB first

2. Applicable conditions

Table 2 Applicable conditions

Item	Setting	
Operating frequency	Input clock	: 16 MHz
	System clock (Iϕ)	: 32 MHz (input clock frequency × 2)
	Peripheral module clock (Pϕ)	: 32 MHz (input clock frequency × 2)
	External bus clock (Bϕ)	: 32 MHz (input clock frequency × 2)
Operating mode	Mode 6 (MD2 = 1, MD1 = 1, and MD0 = 0, MD_CLK = 0)	

3. Description of Modules Used

3.1 Description in Outline

Peripheral modules of the H8SX/1653 which are used in this sample task are shown in figure 2.

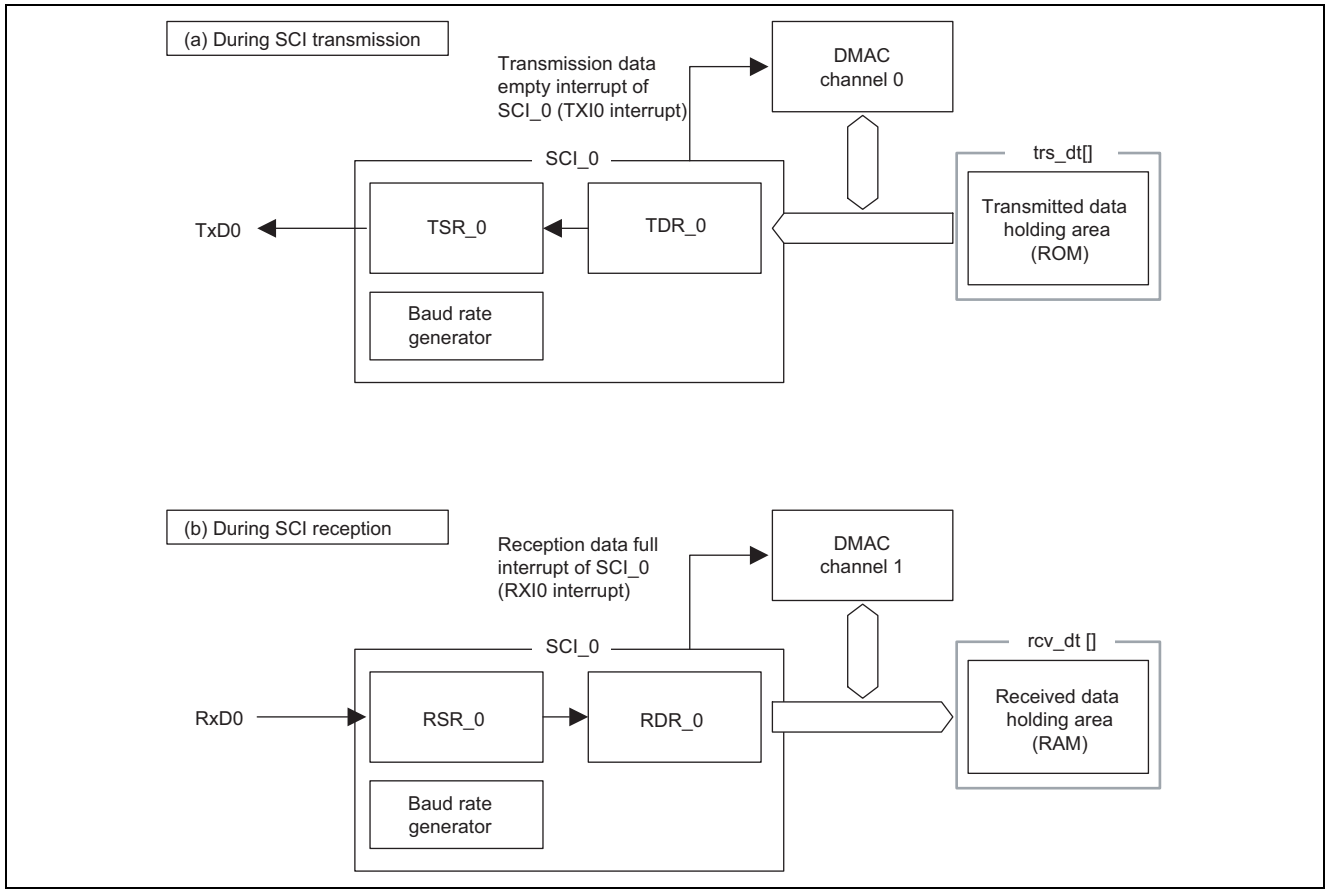


Figure 2 Functions of the H8SX/1653

The description which concerns the blocks shown in figure 2 is stated below.

1. SCI_0
   Transmits and receives data with timing provided by the asynchronous communications.
   a. During SCI transmission
      - When TSR_0 is not full, data for transmission are written to TDR_0, transferred to TSR_0, and then output on the TxD0 pin.
      - When the data are transferred from TDR_0 to TSR_0, a transmission data empty interrupt (TXI0 interrupt) from SCI_0 is generated.
   b. During SCI reception
      - After one frame of data has been received via the RxD0 pin, the received data are transferred from RSR_0 to RDR_0.
      - Once the data have been successfully received and then transferred from RSR_0 to RDR_0, a reception data full interrupt (RXI0 interrupt) from SCI_0 is generated.

2. DMAC channels 0 and 1
   a. During SCI transmission
      - Channel 0 is activated by the transmission data empty interrupt (TXI0 interrupt) from SCI_0 and transfers data from the area where data for transmission are stored to the TDR_0 register.
   b. During SCI reception
      - Channel 1 is activated by the reception data full interrupt (RXI0 interrupt) from SCI_0 and transfers data from RDR_0 to the area where received data is to be stored.

3.2 Description of SCI_0

In this sample task, SCI_0 is used for asynchronous serial data transmission and reception. Figure 3 is a block diagram for SCI_0.

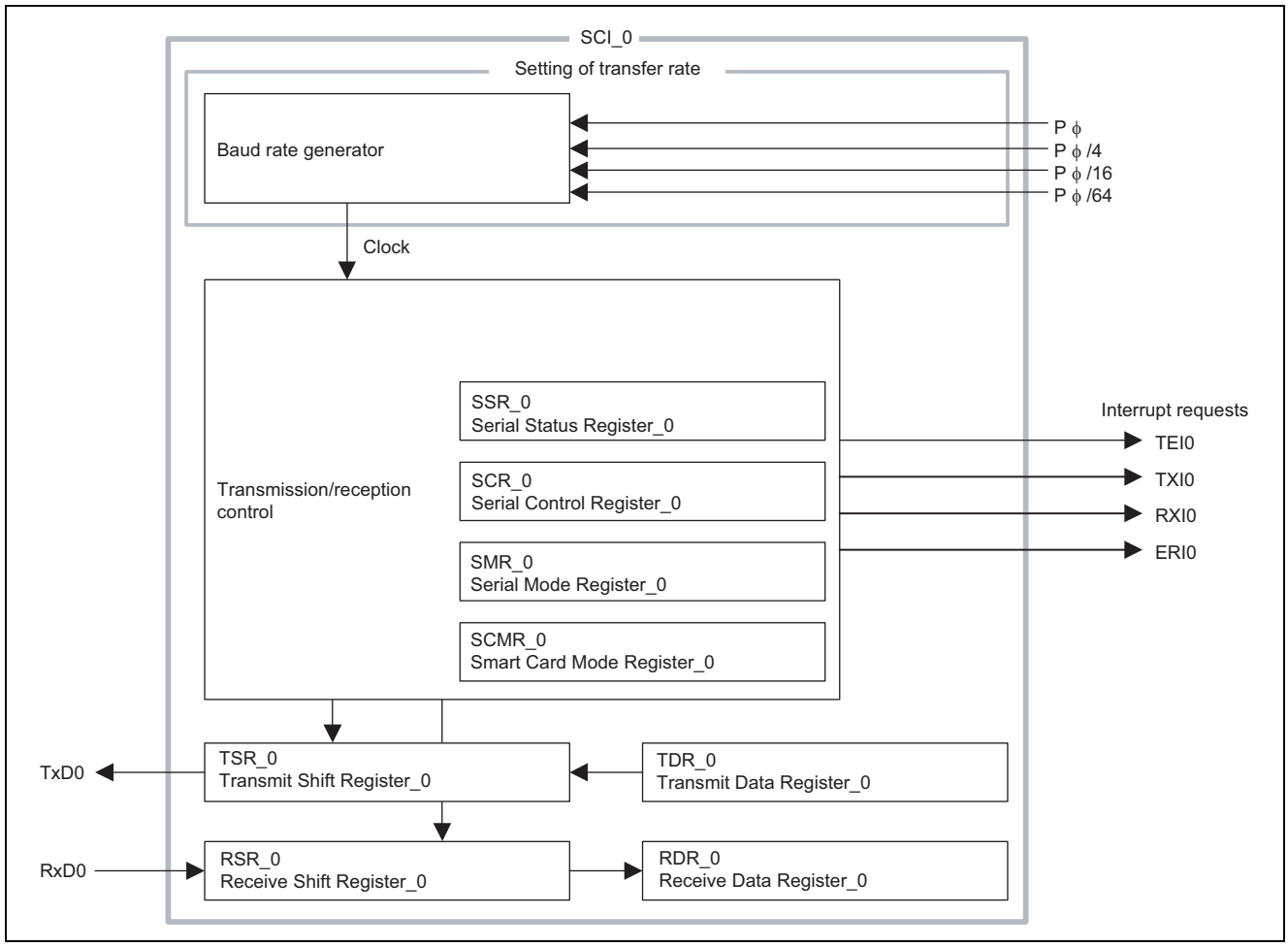


Figure 3 Block Diagram of SCI_0

The description which concerns the blocks shown in figure 3 is stated below.

- On-chip peripheral clock Pϕ
  This is the base clock for the operation of on-chip peripheral functions and is generated by a clock oscillator.
- Receive shift register_0 (RSR_0)
  RSR_0 is used to receive serial data. Serial data on RSR_0 are input via the RxD0 pin. When one frame of data has been received, the data bits are automatically transferred to the receive data register (RDR_0). RDR_0 is not accessible by the CPU.
- Receive data register_0 (RDR_0)
  RDR_0 is an 8-bit register and used to store received data. After RSR_0 has received one frame, the data bits are automatically transferred from RSR_0 to RDR_0. Since RSR_0 and RDR_0 function as a double buffer, continuous reception is possible. RDR_0 is for reception only, and so is seen as a read-only register by the CPU.
- Transmit shift register_0 (TSR_0)
  TSR_0 is used to transmit serial data. In transmission, data are transferred from the transmit data register (TDR_0) to TSR_0, and then output on the TxD0 pin. TSR_0 is not directly accessible from the CPU.
- Transmit data register_0 (TDR_0)
  TDR_0 is an 8-bit register and used to store data for transmission. When SCI_0 detects that TSR_0 is empty, data that have been written to TDR_0 are automatically transferred to TSR_0. Since TDR_0 and TSR_0 function as double buffer, if the next data for transmission has already been written to TDR_0 when one frame of data is transmitted, the written data are transferred to TSR_0. This allows continual transmission. Although TDR_0 can be read from or written to by the CPU at all times, only write data for transmission after having confirmed setting of the TDRE bit in the serial status register (SSR_0) to 1.
- Serial mode register_0 (SMR_0)
  SMR_0 is an 8-bit register and used to select the format of serial data communications and the clock source for the on-chip baud-rate register.
- Serial control register_0 (SCR_0)
  SCR_0 is used to control transmission, reception, and interrupts, and to select the clock source for transmission and reception.
- Serial status register_0 (SSR_0)
  SSR_0 consists of status flags for SCI_0 and multiprocessor bits for transmission and reception. TDRE, RDRF, ORER, PER, and FER can only be cleared.
- Smart card mode register_0 (SCMR_0)
  SCMR_0 is used to select the smart-card interface mode for SCMR_0, and to set up the format for the smart-card mode. For this task, the setting in SCMR_0 selects the normal asynchronous or clock synchronous mode.
- Bit rate register_0 (BRR_0)
  BRR_0 is an 8-bit register that adjusts the bit rate.

3.3 Channels 0 and 1 of the DMAC

In this sample task, DMAC channel 0 is activated by the TXI0 interrupt of SCI_0 and DMAC channel 1 is activated by the RXI0 interrupt of SCI_0. A block diagram of the DMAC is given in figure 4.

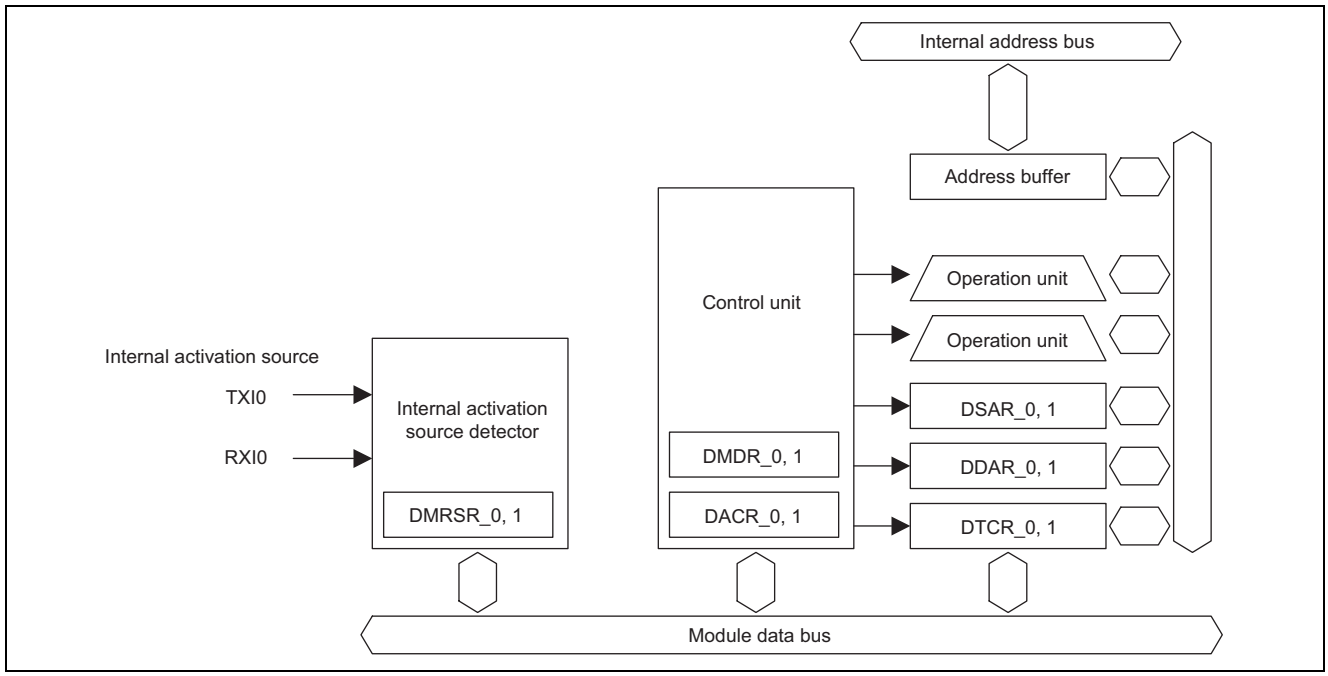


Figure 4 Block Diagram of the DMAC

The description with reference to figure 4 is stated below.

- DMA source address register_0 (DSAR_0)
- DMA source address register_1 (DSAR_1)
  DSARs are 32-bit readable/writable registers and specify the source address for the transfer. Each register is equipped with an address-updating function, so the source address is updated to that for the next transfer each time a transfer operation takes place.

- DMA destination address register_0 (DDAR_0)
- DMA destination address register_1 (DDAR_1)
  DDARs are 32-bit readable/writable registers and specify the destination address for the transfer. Each register is equipped with an address-updating function, so the destination address is updated to that for the next transfer each time a transfer operation takes place.

- DMA transfer count register_0 (DTCR_0)
- DMA transfer count register_1 (DTCR_1)
  DTCRs are 32-bit readable/writable registers and specify the amount of data to be transferred (total size for transfer). After each data transfer operation, the value is reduced by the amount that corresponds to the transferred amount of data. In this sample task, both are set for 128 bytes of data, and the byte is selected as the unit of data access. One is subtracted from the value on each DMAC operation, to indicate the amount still to be transferred.

- DMA mode control register_0 (DMDR_0)
- DMA mode control register_1 (DMDR_1)
  DMDRs control DMAC operation.

- DMA address control register_0 (DACR_0)
- DMA address control register_1 (DACR_1)
  DACRs set the operating mode and transfer method.

- DMA module request select register_0 (DMRSR_0)
- DMA module request select register_1 (DMRSR_1)
  DMRSRs set the activation source.

4. Principles of Operation

4.1 Outline

An outline of operation for this sample task is given in figure 5. 128-byte blocks of data are simultaneously transferred in both directions between the master and slave sides.

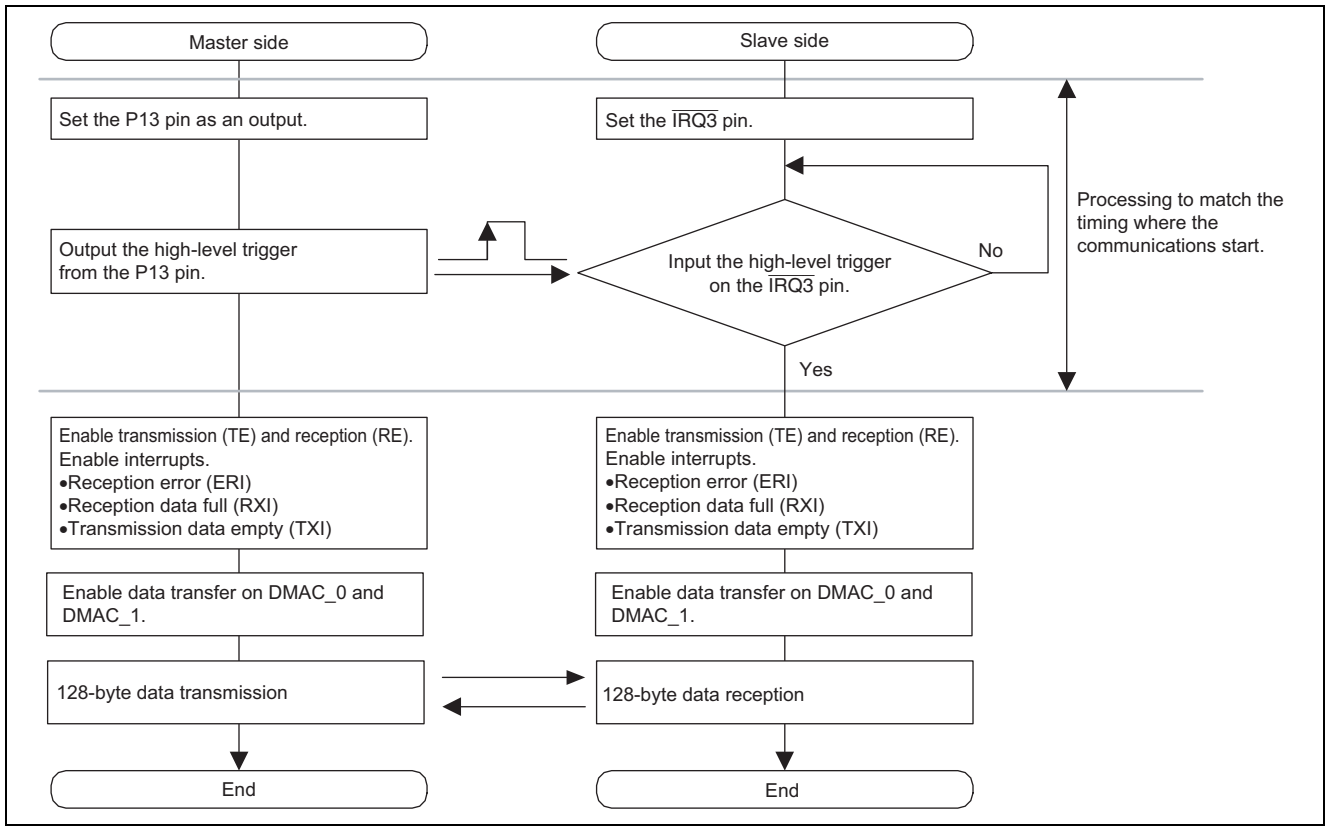


Figure 5 Outline of Operation

4.2 Transmission

4.2.1 Transmission Start

The timing of start of transmission operations is illustrated in figure 6. Table 3 is a list of the hardware and software processing at the numbered points in figure 6.

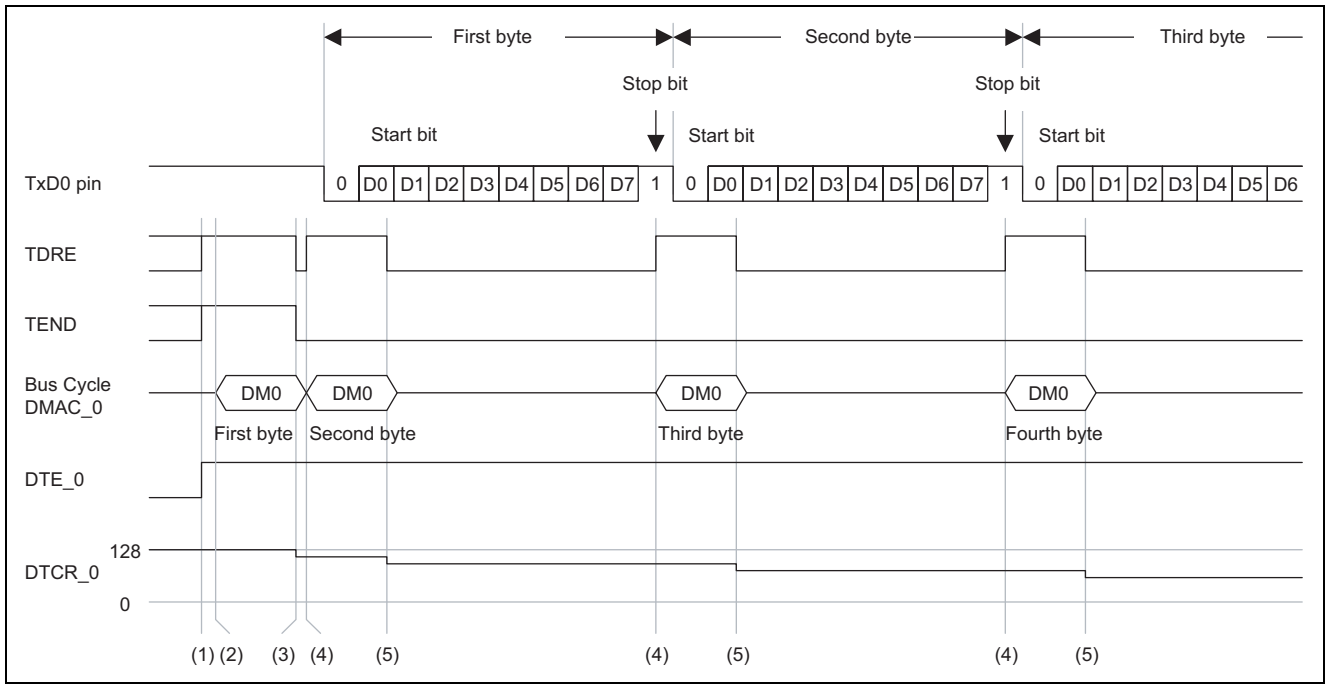


Figure 6 Timing of Transmission Start

Table 3 Processing

	Hardware Processing	Software Processing
(1)	Power-on reset	Initial settings*
(2)	a. Activate DMAC_0, and transfer data for transmission from transmitted data holding area to TDR_0.	None.
(3)	a. Clear TDRE to 0. b. Count the TDCR_0. c. Transfer the contents of TDR_0 to TSR_0.	None.
(4)	a. Set TDRE to 1. b. Activate DMAC_0, and transfer the data from the transmitted data holding area to TDR_0. c. Output the contents of TSR_0 on pin TxD0.	None.
(5)	a. Clear TDRE to 0. b. DTCR_0 counts down. c. Transfer the contents of TDR_0 to TSR_0.	None.

Note: * Initial settings

DMAC_0 settings

a. Source for activation: TXI0 interrupt. The flag (TDRE) for the TXI0 interrupt source is cleared on completion of the DMA transfer.
b. Source address: First address of the area where the data for transmission are stored. Incrementation is selected as the address incrementation or decrementation setting.
c. Destination address: Address of TDR_0. Fixed address is selected as the address incrementation or decrementation setting.
d. Total amount for transfer: 128 bytes
e. DMA data transfer is enabled (DTE_0 = 1).

SCR_0 settings

a. Asynchronous mode. When Pϕ = 32 MHz, Set the transfer rate to 38,400 bps.
b. TXI0 interrupt requests are enabled.
c. Set SCI_0 to enable transmit operations.

4.2.2 Transmission End

The timing of end of transmission operations is illustrated in figure 7. Table 4 is a list of the hardware and software processing at the numbered points in figure 7.

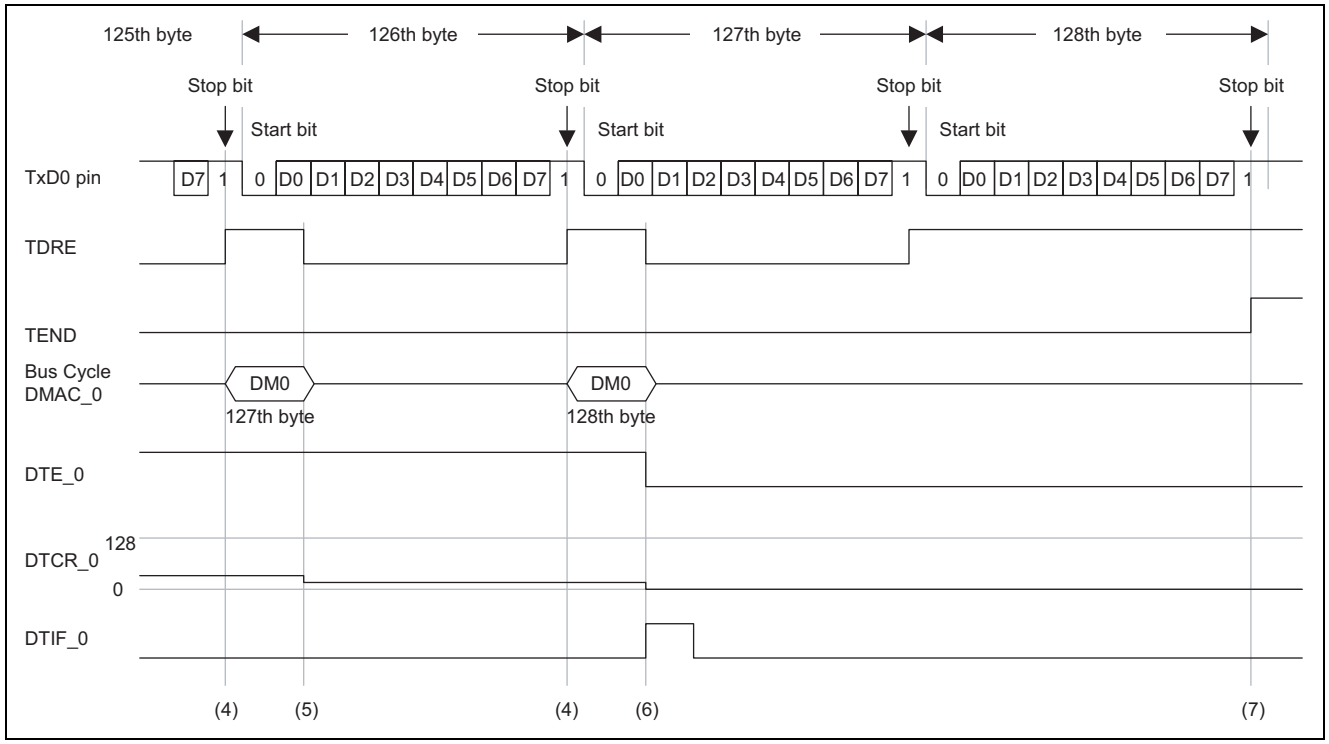


Figure 7 Timing of Transmission End

Table 4 Processing

	Hardware Processing	Software Processing
(4)	a. Set TDRE to 1. b. Activate DMAC_0, and transfer data for transmission from transmitted data holding area to TDR_0. c. Output the contents of TSR_0 on pin TxD0.	None.
(5)	a. Clear TDRE to 0. b. DTCR_0 counts down. c. Transfer the contents of TDR_0 to TSR_0.	None.
(6)	a. Clear TDRE to 0. b. DTCR_0 counts down. (DTCR_0 = 0) c. Disable the DMA data transfer. (DTE_0 = 0) d. Transfer the contents of TDR_0 to TSR_0.	DMAC_0 transfer end interrupt a. Enable TEI0 interrupt request. b. Disable TXI0 interrupt request. c. Disable DMAC_0 transfer end interrupt request.
(7)	a. Set TEND to 1.	TEI0 Interrupt a. Stop SCI_0 transmission operation. b. Disable TEI0 interrupt request.

4.3 Reception

The timing of reception operation is illustrated in figure 8. Table 5 is a list of the hardware and software processing at numbered points in figure 8.

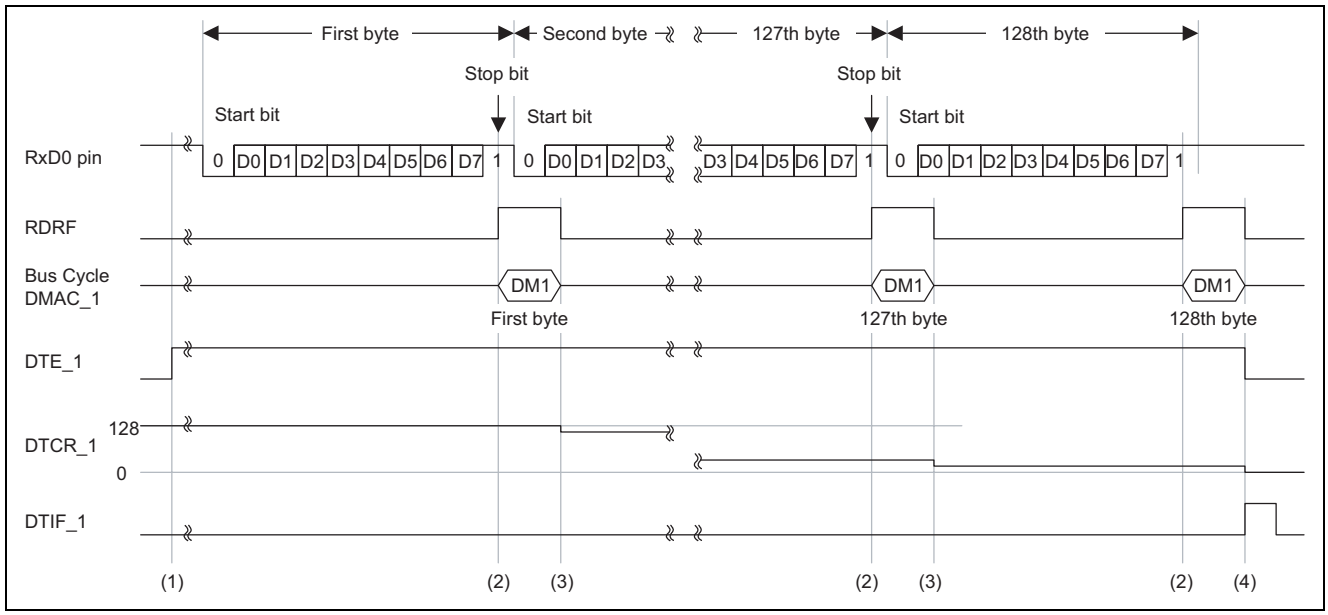


Figure 8 Timing of Reception

Table 5 Processing

	Hardware Processing	Software Processing
(1)	Power-on reset	Initial settings*
(2)	a. Set RDRF to 1. b. End reception normally and transfer the received data from RSR_0 to RDR_0. c. Activate DMAC_1 and transfer the received data from RDR_0 to received data holding area.	None.
(3)	a. Clear RDRF to 0. b. DTCR_1 counts down.	None.
(4)	a. DTCR_1 counts down. (DTCR_1 = 0)	DMAC_1 transfer end interrupt a. Disable reception of SCI_0 (RE = 0). b. Disable interrupt requests of RXI0 and ERI0. c. Disable DMAC_1 transfer end interrupt request.

Note: * Initial settings

DMAC_0 settings

a. Source for activation: RXI0 interrupt. The flag (RDRF) for the RXI0 interrupt source is cleared on completion of the DMA transfer.
b. Source address: Address of RDR_0. Fixed address is selected as the address incrementation or decrementation setting.
c. Destination address: First address of the area where the data for transmission are stored. Incrementation is selected as the address incrementation or decrementation setting.
d. Total amount for transfer: 128 bytes
e. DMA data transfer is enabled (DTE_1 = 1).

SCR_0 settings

a. Asynchronous mode. When Pϕ = 32 MHz, Set the transfer rate to 38,400 bps.
b. RXI0 interrupt requests are enabled.
c. Set SCI_0 to enable transmit operations.

5. Description of Software

5.1 Operating Environment

Table 6 Operating Environment

Item	Description
Development tool	High-performance Embedded Workshop Ver.4.01.01
C/C++ compiler	H8S, H8/300 Series C/C++ Compiler Ver.6.01.02 (manufactured by Renesas Technology)
Compiler options	-cpu = h8sxa:24:md, -code = machinecode, -optimize = 1, -regparam = 3 -speed = (register, shift, struct, expression)

Table 7 Section Settings

Address	Section Name	Description
H'001000	P	Program area
	C	Constant area
H'FF2000	B	Not initialized data area (RAM area)

Table 8 Vector Table for Interrupt Exception Handling

Interrupt Exception Source		Vector No.	Vector Address	Function to Interrupt Destination
Reset		0	H'000000	init
DMAC_0	DMTEND0	128	H'000200	dmtend0_int
DMAC_1	DMTEND1	129	H'000204	dmtend1_int
SCI_0	ERI0	144	H'000240	eri0_int
SCI_0	TEI0	147	H'00024C	tri0_int

5.2 List of Functions

Table 9 lists the functions used in this sample task. Figure 9 shows the structure of hierarchy.

Table 9 List of Functions

Function Name	Description
init	Initialization routine: Releases from the module stop mode, makes the clock settings, and calls the main function.
main	Master side (MASTER) main routine Selects asynchronous SCI, calls functions DMAC0_trs_init and DMAC1_rcv_init. Produces a high-level trigger on pin P13. Makes settings for the transmission and reception of 128 bytes of data.
	Slave side (SLAVE) main routine Selects asynchronous SCI, calls functions DMAC0_trs_init and DMAC1_rcv_init. Produces a high-level trigger on $\overline{\text{IRQ3}}$ pin. Makes settings for the transmission and reception of 128 bytes of data.
DMAC0_trs_init	DMAC_0 initialization Select TXI0-interrupt-triggered processing of transfer from the area where data for transmission are stored to TDR_0.
DMAC1_rcv_init	DMAC_1 initialization Select RXI0-interrupt-triggered processing of transfer from RDR_0 to the area where received data are to be stored.
dmtend0_int	DMAC_0 transfer end interrupt Set TEI0 interrupt request enabled, TXI0 interrupt request disabled, DMAC_0 transfer end interrupt request disabled.
dmtend1_int	DMAC_1 transfer end interrupt Set reception in SCI_0, interrupt requests of RXI0 and ERI0, and DMAC_1 transfer end interrupt request disabled.
eri0_int	SCI_0 reception error interrupt (ERI0 interrupt) Write error data to RAM and initialize SSR_0.
tei0_int	SCI_0 transmission end interrupt (TEI0 interrupt) Set transmission in SCI_0 and TEI0 interrupt request disabled.

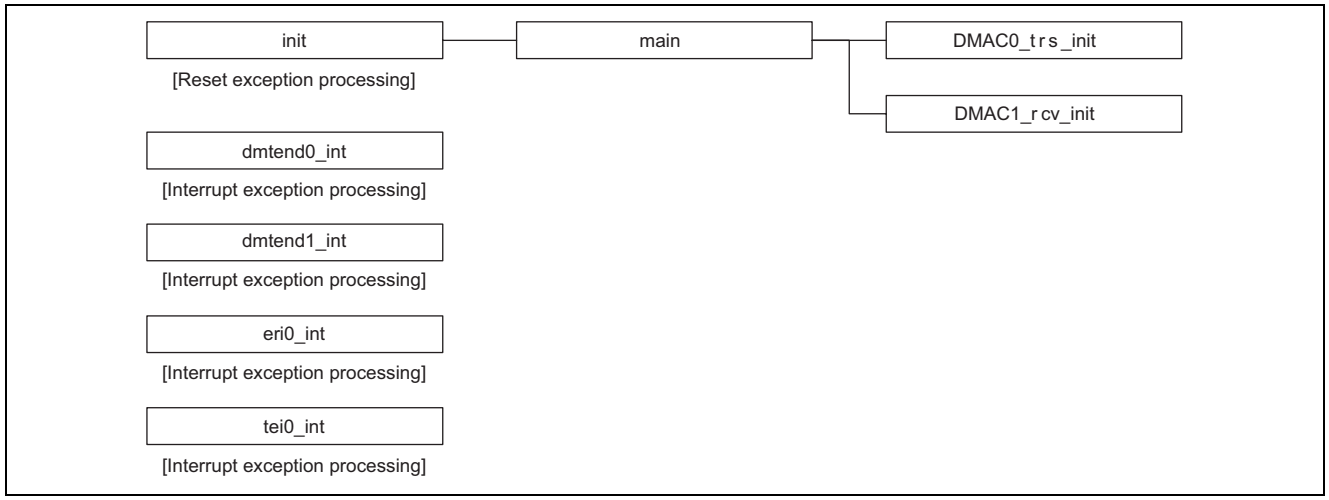


Figure 9 Structure of Hierarchy

5.3 RAM Usage

Table 10 RAM Usage

Type	Variable Name	Description	Used in
unsigned char	endflg	Transmission end flag 0: Transmission in progress 1: Transmission ended	main, tei0_int
unsigned char	errbuf	Reception error buffer The contents of SSR_0 are stored when an overrun, framing, or parity error occurs.	main, eri0_int
unsigned char	tcnt	Transmission counter	main, dmtend0_int
unsigned char	rcnt	Reception counter	main, dmtend1_int
unsigned char	rcv_dt[128]	Received data holding area (RAM)	main, DMAC1_rcv_int

5.4 Constant

Table 11 Constant

Type	Variable Name	Settings	Description	Used in
unsigned char	trs_dt[128]	H'00, H'01, H'02, … ……H'7E, H'7F	Transmitted data holding area (RAM)	main, DMAC0_trs_int

5.5 Macro Definitions

Table 12 Macro Definitions

Identifier	Description	Used in
MASTER	Generates the master-side program.	main
SLAVE	Generates the slave-side program.	main

5.6 Symbolic Constant

Table 13 List of Symbolic Constant

Constant Name	Setting	Description
NUM	128	Sets the number of data for transmission and reception.

5.7 Description of Functions

5.7.1 init Function

1. Functional overview
   Initialization routine. (Releases the module stop mode, sets the clock, and calls the main function.)
2. Arguments
   None
3. Return value
   None
4. Description of internal registers used
   The internal registers used in this sample task are described below. Note that the settings shown below are not the initial values but the values used in this sample task.

- Mode control register (MDCR) Number of bits: 16 Address: H'FFFDC0

Bit	Bit Name	Setting	R/W	Description
15	MDS7	Undefined*	R	Indicates the value set by a mode pin (MD3). When MDCR is read, the input level on the MD3 pin is latched. This latching is released by a reset.
11	MDS3	Undefined*	R	Mode Select 3 to 0
10	MDS2	Undefined*	R	These bits indicate the operating mode selected by the mode pins (MD2 to MD0; see table 14). When MDCR is read, the signal levels input on pins MD2 to MD0 are latched into these bits. The latch is released by a reset.
9	MDS1	Undefined*	R	
8	MDS0	Undefined*	R	

Note: * Determined by the settings on pins MD3 to MD0.

Table 14 Values of Bits MDS3 to MDS0

MCU Operating Mode	Mode Pins			MDCR			
	MD2	MD1	MD0	MDS3	MDS2	MDS1	MDS0
2	0	1	0	1	1	0	0
4	1	0	0	0	0	1	0
5	1	0	1	0	0	0	1
6	1	1	0	0	1	0	1
7	1	1	1	0	1	0	0

- System clock control register (SCKCR) Number of bits: 16 Address: H'FFFDC4

Bit	Bit Name	Setting	R/W	Description
10	ICK2	0	R/W	System Clock (Iϕ) Select
9	ICK1	0	R/W	These bits select the frequency of the system clock
8	ICK0	1	R/W	provided to the CPU, DMAC, and DTC. 001: Input clock × 2
6	PCK2	0	R/W	Peripheral Module Clock (Pϕ) Select
5	PCK1	0	R/W	These bits select the frequency of the peripheral module
4	PCK0	1	R/W	clock. 001: Input clock × 2
2	BCK2	0	R/W	External Bus Clock (Bϕ) Select
1	BCK1	0	R/W	These bits select the frequency of the external bus clock.
0	BCK0	1	R/W	001: Input clock × 2

- MSTPCRA, MSTPCRB, and MSTPCRC control the module stop mode. Setting a bit to 1 makes the corresponding module enter the module stop mode, while clearing the bit to 0 releases the module from module stop mode.
- Module stop control register A (MSTPCRA) Number of bits: 16 Address: H'FFFDC8

Bit	Bit Name	Setting	R/W	Description
15	ACSE	0	R/W	All-Module-Clock-Stop Mode Enable Enables/disables all-module-clock-stop mode for reducing current drawn by stopping the operation of bus controller and I/O ports when the CPU executes the SLEEP instruction after the module stop mode has been set for all of the on-chip peripheral modules controlled by MSTPCR. 0: Disables all-module-clock-stop mode 1: Enabled all-module-clock-stop mode
13	MSTPA13	0	R/W	DMA controller (DMAC)
12	MSTPA12	1	R/W	Data transfer controller (DTC)
9	MSTPA9	1	R/W	8-bit timer unit (TMR_3, TMR_2)
8	MSTPA8	1	R/W	8-bit timer unit (TMR_1 and TMR_0)
5	MSTPA5	1	R/W	D/A converter (channels 1 and 0)
3	MSTPA3	1	R/W	A/D converter (unit 0)
0	MSTPA0	1	R/W	16-bit timer pulse unit (TPU channels 5 to 0)

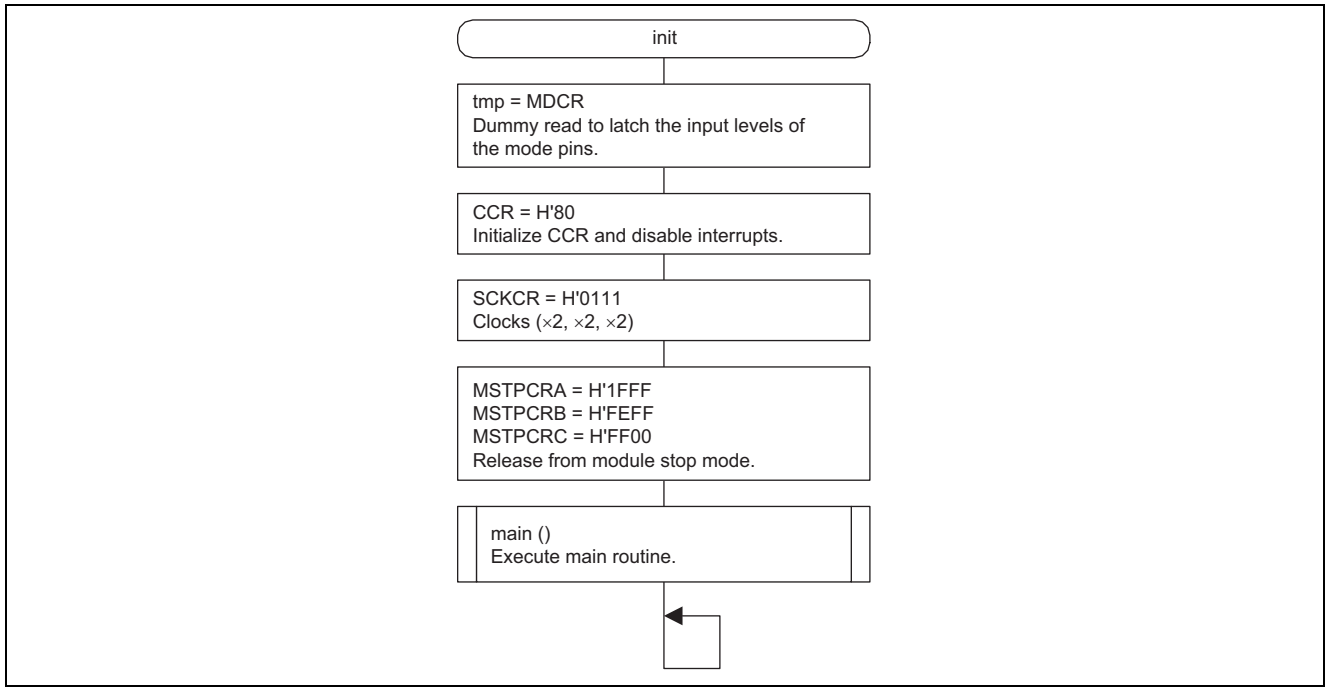
- Module stop control register B (MSTPCRB) Number of bits: 16 Address: H'FFFDCA

Bit	Bit Name	Setting	R/W	Description
15	MSTPB15	1	R/W	Programmable pulse generator (PPG)
12	MSTPB12	1	R/W	Serial communications interface_4 (SCI_4)
10	MSTPB10	1	R/W	Serial communications interface_2 (SCI_2)
9	MSTPB9	1	R/W	Serial communications interface_1 (SCI_1)
8	MSTPB8	0	R/W	Serial communications interface_0 (SCI_0)
7	MSTPB7	1	R/W	I^2C bus interface_1 (IIC_1)
6	MSTPB6	1	R/W	I^2C bus interface_0 (IIC_0)

- Module stop control register C (MSTPCRC) Number of bits: 16 Address: H'FFFDCC

Bit	Bit Name	Setting	R/W	Description
15	MSTPC15	1	R/W	Serial communications interface_5 (SCI_5), (IrDA)
14	MSTPC14	1	R/W	Serial communications interface_6 (SCI_6)
13	MSTPC13	1	R/W	8-bit timer unit (TMR_4, TMR_5)
12	MSTPC12	1	R/W	8-bit timer unit (TMR_6, TMR_7)
11	MSTPC11	1	R/W	Universal serial bus interface (USB)
10	MSTPC10	1	R/W	Cyclic redundancy checker
4	MSTPC4	0	R/W	On-chip RAM_4 (H'FF2000 to H'FF3FFF)
3	MSTPC3	0	R/W	On-chip RAM_3 (H'FF4000 to H'FF5FFF)
2	MSTPC2	0	R/W	On-chip RAM_2 (H'FF6000 to H'FF7FFF)
1	MSTPC1	0	R/W	On-chip RAM_1 (H'FF8000 to H'FF9FFF)
0	MSTPC0	0	R/W	On-chip RAM_0 (H'FFA000 to H'FFBFFF)

5. Flowchart



5.7.2 Master-side (MASTER) main Function

1. Functional overview
   Main routine. (Sets the asynchronous SCI, calls functions DMAC0_trs_init and DMAC1_rcv_init, outputs high-level trigger on P13 pin, and sets transmission and reception of 128-byte data.)
2. Arguments
   None
3. Return values
   None
4. Description of internal registers used
   The internal registers used in this sample task are described below. Note that the settings shown below are not the initial values but the values used in this sample task.

- Port 1 data direction register (P1DDR) Number of bits: 8 Address: H'FFFB80

Bit	Bit Name	Setting	R/W	Description
3	P13DDR	1	W	0: P13 pin is an input. 1: P13 pin is an output.

- Port 2 input buffer control register (P2ICR) Number of bits: 8 Address: H'FFFF91

Bit	Bit Name	Setting	R/W	Description
1	P21ICR	1	R/W	0: Input buffer for P21 (RxD0) pin is disabled. Input signal is fixed to the high level. 1: Input buffer for P21 (RxD0) pin is enabled. The pin state reflects the peripheral modules.

- DMA mode control register_0 (DMDR_0) Number of bits: 32 Address: H'FFFC14

Bit	Bit Name	Setting	R/W	Description
31	DTE	1	R/W	Data Transfer Enable 0: Disables data transfer. 1: Enables data transfer.

- DMA mode control register_1 (DMDR_1) Number of bits: 32 Address: H'FFFC34

Bit	Bit Name	Setting	R/W	Description
31	DTE	1	R/W	Data Transfer Enable 0: Disables data transfer. 1: Enables data transfer.

- Port 1 data register (P1DR) Number of bits: 8 Address: H'FFFF50

Bit	Bit Name	Setting	R/W	Description
3	P13DR	0/1	R/W	0: P13 pin is set to a low level. 1: P13 pin is set to a high level.

- Serial mode register_0 (SMR_0) Number of bits: 8 Address: H'FFFF80

Bit	Bit Name	Setting	R/W	Description
7	C/$\overline{A}$	0	R/W	Communication mode: 0: Asynchronous 1: clock synchronous
6	CHR	0	R/W	Character Length 0: Selects 8 bits as the data length. 1: Selects 7 bits as the data length.
5	PE	0	R/W	Parity Enable 0: No parity bit. 1: Parity bit included.
3	STOP	0	R/W	Stop Bit Length Selects the length of the stop-bit field in transmission. 0: 1 stop bit 1: 2 stop bits In reception, only the first of the stop bits is checked, and when the second stop bit is 0, it is treated as the start bit of the next frame to be transmitted.
1	CKS1	0	R/W	Clock Select 1, 0
0	CKS0	0	R/W	These bits select the clock source for the baud rate generator. 00: Pϕ clock (n = 0) For the relation between the settings of these bits and the baud rate, see section 14.3.9, Bit Rate Register (BRR) in the hardware manual. n is the decimal display of the value of n in BRR (see section 14.3.9, Bit Rate Register (BRR) in the hardware manual.)

- Bit rate register_0 (BRR_0) Number of bits: 8 Address: H'FFFF81
  Function: BRR_0 is used to adjust the bit rate. When Pϕ = 32 MHz, CKS1 and CKS0 in SMR_0 = B'00 and BRR_0 = 25 will set the bit rate to 38,400 bps.
  Setting: 25

- Serial control register_0 (SCR_0) Number of bits: 8 Address: H'FFFF82

Bit	Bit Name	Setting	R/W	Description
7	TIE	0/1	R/W	Transmit Interrupt Enable 0: Disables TXI interrupt requests. 1: Enables TXI interrupt requests.
6	RIE	0/1	R/W	Receive Interrupt Enable 0: Disables RXI and ERI interrupt requests. 1: Enables RXI and ERI interrupt requests.
5	TE	0/1	R/W	Transmit Enable 0: Disables transmission. 1: Enables transmission.
4	RE	0/1	R/W	Receive Enable 0: Disables reception. 1: Enables reception.
2	TEIE	0	R/W	Transmit End Interrupt Enable 0: Disables TEI interrupt requests. 1: Enables TEI interrupt requests.
1 0	CKE1 CKE0	0 0	R/W	Clock Enable 1, 0 Selects the clock source. 00: Internal baud rate generator. 1X: Timer clock input or average transfer rate generator.

Note X: Don't care.

- Serial status register_0 (SSR_0) Number of bits: 8 Address: H'FFFF84

Bit	Bit Name	Setting	R/W	Description
7	TDRE	Undefined	R/(W)*	Transmit Data Register Empty Indicates whether TDR contains data for transmission. [Setting conditions] • Clearing of the TE bit in SCR to 0 • Transfer of data from TDR to TSR [Clearing conditions] • Writing of 0 to TDRE after having read TDRE = 1 (when using an interrupt and having the CPU clear it, be sure to read the flag after having written 0 to it.) • Generation of a TXI interrupt request allowing DMAC to write transmit data to TDR
6	RDRF	0	R/(W)*	Receive Data Register Full Indicates whether RDR holds received data. [Setting conditions] • The normal end of serial reception and the transfer of received data from RSR to RDR. [Clearing conditions] • Writing of 0 to RDRF after having read RDRF = 1 (when using an interrupt and having the CPU clear it, be sure to read the flag after having written 0 to it.) • The RDRF flag is not affected and retains its previous value even though the RE bit in SCR is cleared to 0. Note that when the next reception is completed while the RDRF flag is being set to 1, an overrun error occurs and the received data are lost.
5	ORER	0	R/(W)*	Overrun Error [Setting condition] • Occurrence of an overrun during reception [Clearing condition] • Writing of 0 to ORER after having read ORER = 1 (when using an interrupt and having the CPU clear it, be sure to read the flag after having written 0 to it.)
4	FER	0	R/(W)*	Framing Error [Setting condition] • Occurrence of a framing error during reception [Clearing condition] • Writing of 0 to FER after having read FER = 1 (when using an interrupt and having the CPU clear it, be sure to read the flag after having written 0 to it.)
3	PER	0	R/(W)*	Parity Error [Setting condition] • Occurrence of a parity error during reception [Clearing condition] • Writing of 0 to PER after having read PER = 1 (when using an interrupt and having the CPU clear it, be sure to read the flag after having written 0 to it.)

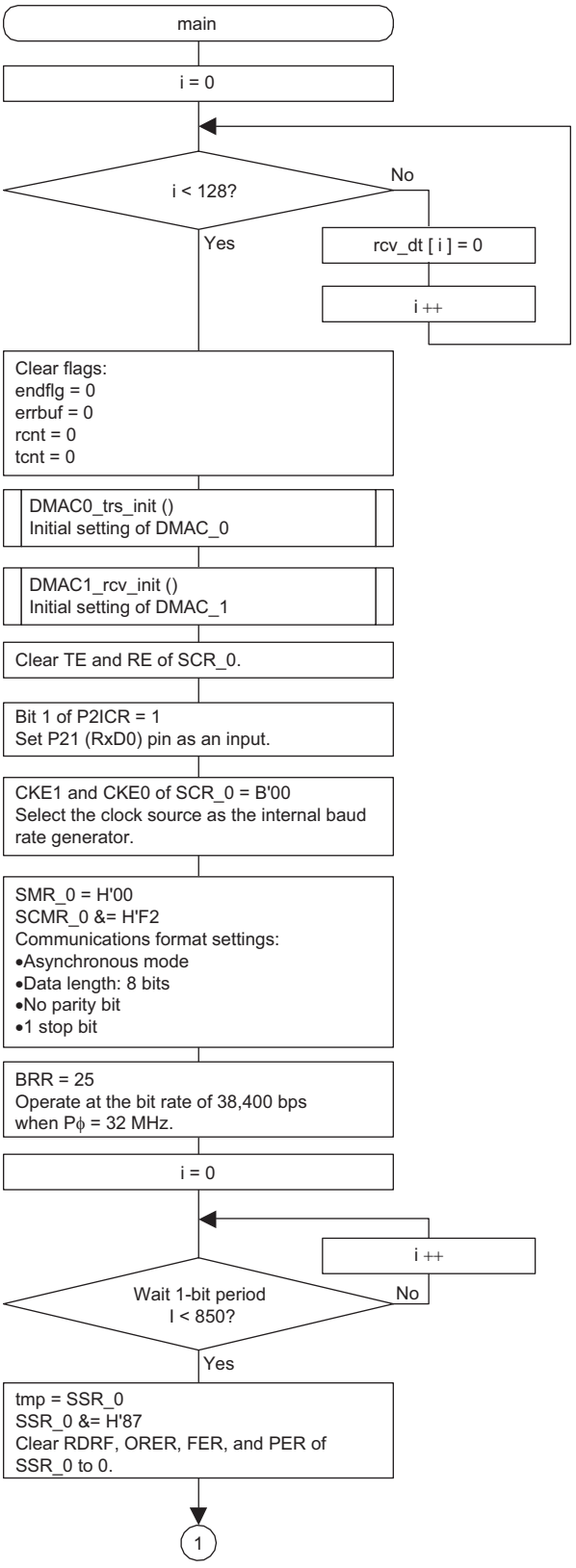
Bit	Bit Name	Setting	R/W	Description
2	TEND	Undefined	R	Transmit End [Setting conditions] • Clearing of the TE bit in SCR to 0 • TDRE = 1 on transmission of the last bit of a character [Clearing conditions] • Writing of 0 to TDRE flag after having read TDRE = 1 • Generation of a TXI interrupt request allowing DMAC to write data to TDR

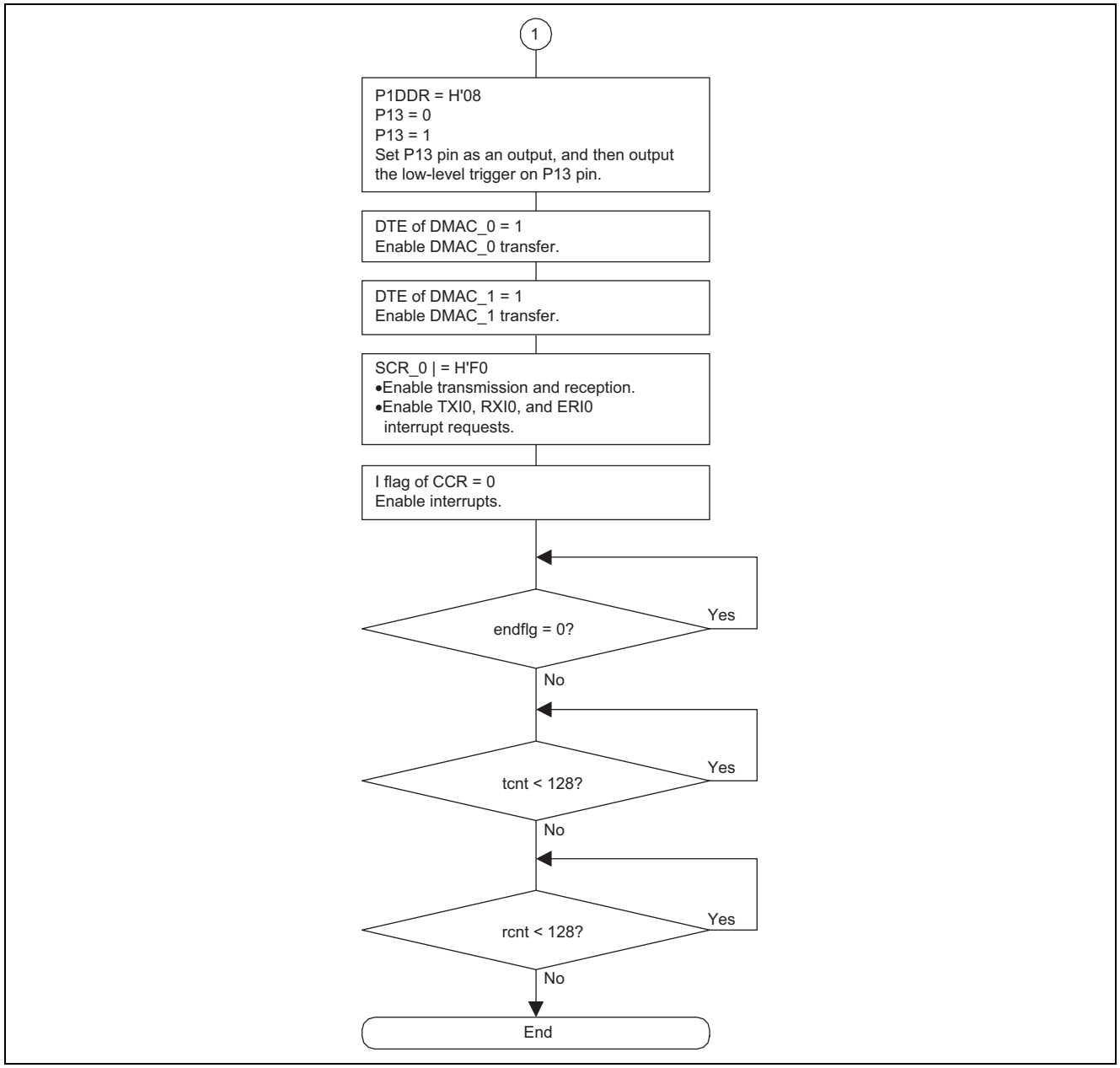
Note: * Only 0 can be written here, to clear the flag.

- Smart card mode register_0 (SCMR_0) Number of bits: 8 Address: H'FFFF86

Bit	Bit Name	Setting	R/W	Description
0	SMIF	0	R/W	Smart Card Interface Mode Select 0: Operation is in the normal asynchronous or clock synchronous mode. 1: Operation is in smart card interface mode.

5. Flowchart


main
i = 0
i < 128?
No
Yes
rcv_dt [i] = 0
i ++
Clear flags:
endflg = 0
errbuf = 0
rcnt = 0
tcnt = 0
DMAC0_trs_init ()
Initial setting of DMAC_0
DMAC1_rcv_init ()
Initial setting of DMAC_1
Clear TE and RE of SCR_0.
Bit 1 of P2ICR = 1
Set P21 (RxD0) pin as an input.
CKE1 and CKE0 of SCR_0 = B'00
Select the clock source as the internal baud rate generator.
SMR_0 = H'00
SCMR_0 &= H'F2
Communications format settings:
•Asynchronous mode
•Data length: 8 bits
•No parity bit
•1 stop bit
BRR = 25
Operate at the bit rate of 38,400 bps when Pϕ = 32 MHz.
i = 0
i ++
Wait 1-bit period
I < 850?
No
Yes
tmp = SSR_0
SSR_0 &= H'87
Clear RDRF, ORER, FER, and PER of SSR_0 to 0.
1


1
P1DDR = H'08
P13 = 0
P13 = 1
Set P13 pin as an output, and then output the low-level trigger on P13 pin.
DTE of DMAC_0 = 1
Enable DMAC_0 transfer.
DTE of DMAC_1 = 1
Enable DMAC_1 transfer.
SCR_0 | = H'F0
•Enable transmission and reception.
•Enable TXI0, RXI0, and ERI0 interrupt requests.
I flag of CCR = 0
Enable interrupts.
endflg = 0?
Yes
No
tcnt < 128?
Yes
No
rcnt < 128?
Yes
No
End

5.7.3 Slave-Side (SLAVE) main Function

1. Functional overview
   Main routine. (Sets the asynchronous SCI, calls functions DMAC0_trs_init and DMAC1_rcv_init, judges input of high-level trigger on $\overline{\text{IRQ3}}$ pin, and sets transmission and reception of 128-byte data.)
2. Arguments
   None
3. Return values
   None
4. Description of internal registers used
   The internal registers used in this sample task are described below. Note that the settings shown below are not the initial values but the values used in this sample task.

- Port 1 input buffer control register (P1ICR) Number of bits: 8 Address: H'FFFB90

Bit	Bit Name	Setting	R/W	Description
3	P13ICR	1	R/W	0: Input buffer for P13 pin is disabled. Input signal is fixed to the high level. 1: Input buffer for P13 pin is enabled. The pin state reflects the peripheral modules.

- Port 2 input buffer control register (P2ICR) Number of pins: 8 Address: H'FFFF91

Bit	Bit Name	Setting	R/W	Description
1	P21ICR	1	R/W	0: Input buffer for P21 (RxD0) pin is disabled. Input signal is fixed to the high level. 1: Input buffer for P21 (RxD0) pin is enabled. The pin state reflects the peripheral modules.

- Port function control register C (PFCRC) Number of pins: 8 Address: H'FFFBCC

Bit	Bit Name	Setting	R/W	Description
3	ITS3	0	R/W	$\overline{\text{IRQ3}}$ Pin Select 0: Set P13 pin as an $\overline{\text{IRQ3-A}}$ input. 1: Set P53 pin as an $\overline{\text{IRQ-3-B}}$ input.

- DMA mode control register_0 (DMDR_0) Number of bits: 32 Address: H’FFFC14

Bit	Bit Name	Setting	R/W	Description
31	DTE	1	R/W	Data Transfer Enable 0: Disables data transfer. 1: Enables data transfer.

- DMA mode control register_1 (DMDR_1) Number of bits: 32 Address: H’FFFC34

Bit	Bit Name	Setting	R/W	Description
31	DTE	1	R/W	Data Transfer Enable 0: Disables data transfer. 1: Enables data transfer

- IRQ sense control register L (ISCRL) Number of bits: 16 Address: H'FFFD6A

Bit	Bit Name	Setting	R/W	Description
7	IRQ3SR	1	R/W	IRQ3 Sense Control Rise
6	IRQ3SF	0		IRQ3 Sense Control Fall 10: Generates interrupt requests at the rising edge of $\overline{IRQ3}$.

- IRQ status register (ISR) Number of bits: 16 Address: H'FFFF36

Bit	Bit Name	Setting	R/W	Description
0	IRQ3F	0	R/(W)*	IRQ3 Flag 0: No occurrence of IRQ3 interrupt 1:Occurrence of IRQ3 interrupt

Note: * Only 0 can be written here, to clear the flag.

- Serial mode register_0 (SMR_0) Number of bits: 8 Address: H'FFFF80

Bit	Bit Name	Setting	R/W	Description
7	C/$\overline{A}$	0	R/W	Communication mode: 0: Asynchronous 1: Clock synchronous
6	CHR	0	R/W	Character Length 0: Selects 8 bits as the data length. 1: Selects 7 bits as the data length.
5	PE	0	R/W	Parity Enable 0: No parity bit. 1: Parity bit included.
3	STOP	0	R/W	Stop Bit Length Selects the length of the stop-bit field in transmission. 0: 1 stop bit 1: 2 stop bits In reception, only the first of the stop bits is checked, and when the second stop bit is 0, it is treated as the start bit of the next frame to be transmitted.
1	CKS1	0	R/W	Clock Select 1, 0
0	CKS0	0	R/W	These bits select the clock source for the baud rate generator. 00: Pϕ clock (n = 0) For the relation between the settings of these bits and the baud rate, see section 14.3.9, Bit Rate Register (BRR) in the hardware manual. n is the decimal display of the value of n in BRR (see section 14.3.9, Bit Rate Register (BRR) in the hardware manual.)

- Bit rate register_0 (BRR_0) Number of bits: 8 Address: H'FFFF81
  Function: BRR_0 is used to adjust the bit rate. When Pϕ = 32 MHz, CKS1 and CKS0 in SMR_0 = B'00 and BRR_0 = 25 will set the bit rate to 38,400 bps.
  Setting: 25

- Serial control register_0 (SCR_0) Number of bits: 8 Address: H'FFFF82

Bit	Bit Name	Setting	R/W	Description
7	TIE	0/1	R/W	Transmit Interrupt Enable 0: Disables TXI interrupt requests. 1: Enables TXI interrupt requests.
6	RIE	0/1	R/W	Receive Interrupt Enable 0: Disables RXI and ERI interrupt requests. 1: Enables RXI and ERI interrupt requests.
5	TE	0/1	R/W	Transmit Enable 0: Disables transmission. 1: Enables transmission.
4	RE	0/1	R/W	Receive Enable 0: Disables reception. 1: Enables reception.
2	TEIE	0	R/W	Transmit End Interrupt Enable 0: Disables TEI interrupt requests. 1: Enables TEI interrupt requests.
1 0	CKE1 CKE0	0 0	R/W	Clock Enable 1, 0 Selects the clock source. 00: Internal baud rate generator. 1X: Timer clock input or average transfer rate generator.

Note X: Don't care.

- Serial status register_0 (SSR_0) Number of bits: 8 Address: H'FFFF84

Bit	Bit Name	Setting	R/W	Description
7	TDRE	Undefined	R/(W)*	Transmit Data Register Empty Indicates whether TDR contains data for transmission. [Setting conditions] • Clearing of the TE bit in SCR to 0 • Transfer of data from TDR to TSR [Clearing conditions] • Writing of 0 to TDRE after having read TDRE = 1 (when using an interrupt and having the CPU clear it, be sure to read the flag after having written 0 to it). • Generation of a TXI interrupt request allowing DMAC to write transmit data to TDR
6	RDRF	0	R/(W)*	Receive Data Register Full Indicates whether RDR holds received data. [Setting conditions] • The normal end of serial reception and the transfer of received data from RSR to RDR. [Clearing conditions] • Writing of 0 to RDRF after having read RDRF = 1 (when using an interrupt and having the CPU clear it, be sure to read the flag after having written 0 to it.) • The RDRF flag is not affected and retains its previous value even though the RE bit in SCR is cleared to 0. Note that when the next reception is completed while the RDRF flag is being set to 1, an overrun error occurs and the received data are lost.
5	ORER	0	R/(W)*	Overrun Error [Setting condition] • Occurrence of an overrun during reception [Clearing condition] • Writing of 0 to ORER after having read ORER = 1 (when using an interrupt and having the CPU clear it, be sure to read the flag after having written 0 to it.)
4	FER	0	R/(W)*	Framing Error [Setting condition] • Occurrence of a framing error during reception [Clearing condition] • Writing of 0 to FER after having read FER = 1 (when using an interrupt and having the CPU clear it, be sure to read the flag after having written 0 to it.)
3	PER	0	R/(W)*	Parity Error [Setting condition] • Occurrence of a parity error during reception [Clearing condition] • Writing of 0 to PER after having read PER = 1 (when using an interrupt and having the CPU clear it, be sure to read the flag after having written 0 to it.)

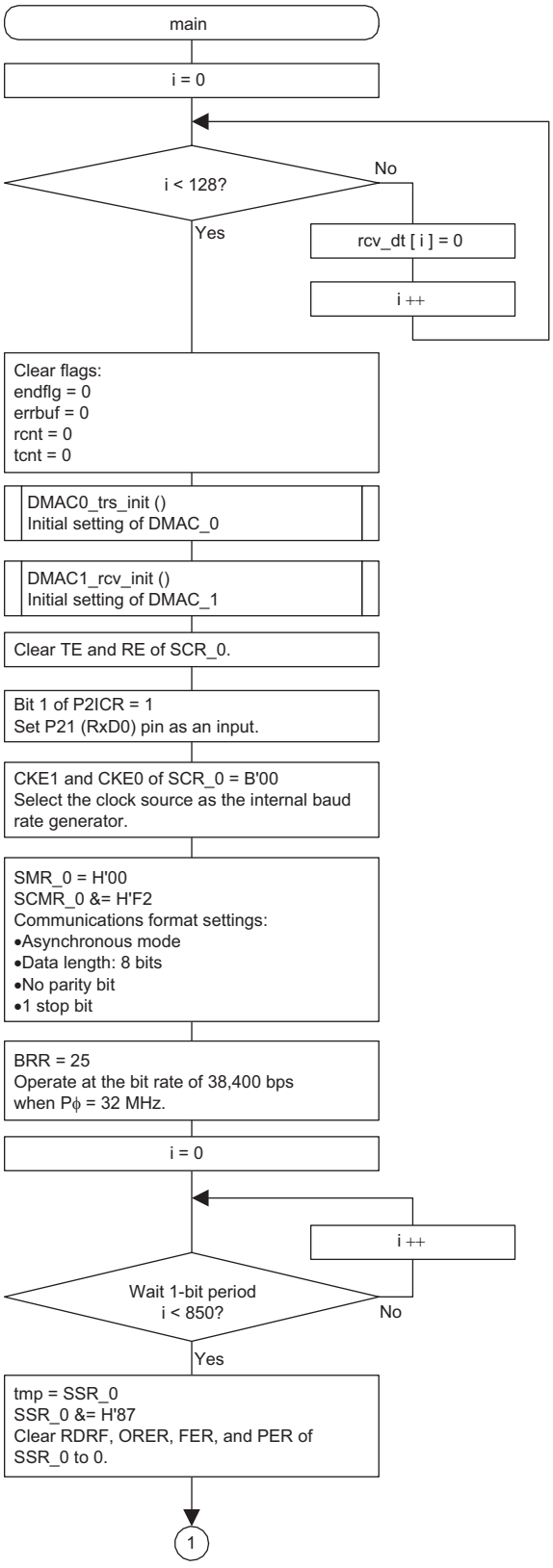
Bit	Bit Name	Setting	R/W	Description
2	TEND	Undefined	R	Transmit End [Setting conditions] • Clearing of the TE bit in SCR to 0 • TDRE = 1 on transmission of the last bit of a character [Clearing conditions] • Writing of 0 to TDRE flag after having read TDRE = 1 • Generation of a TXI interrupt request allowing DMAC to write data to TDR

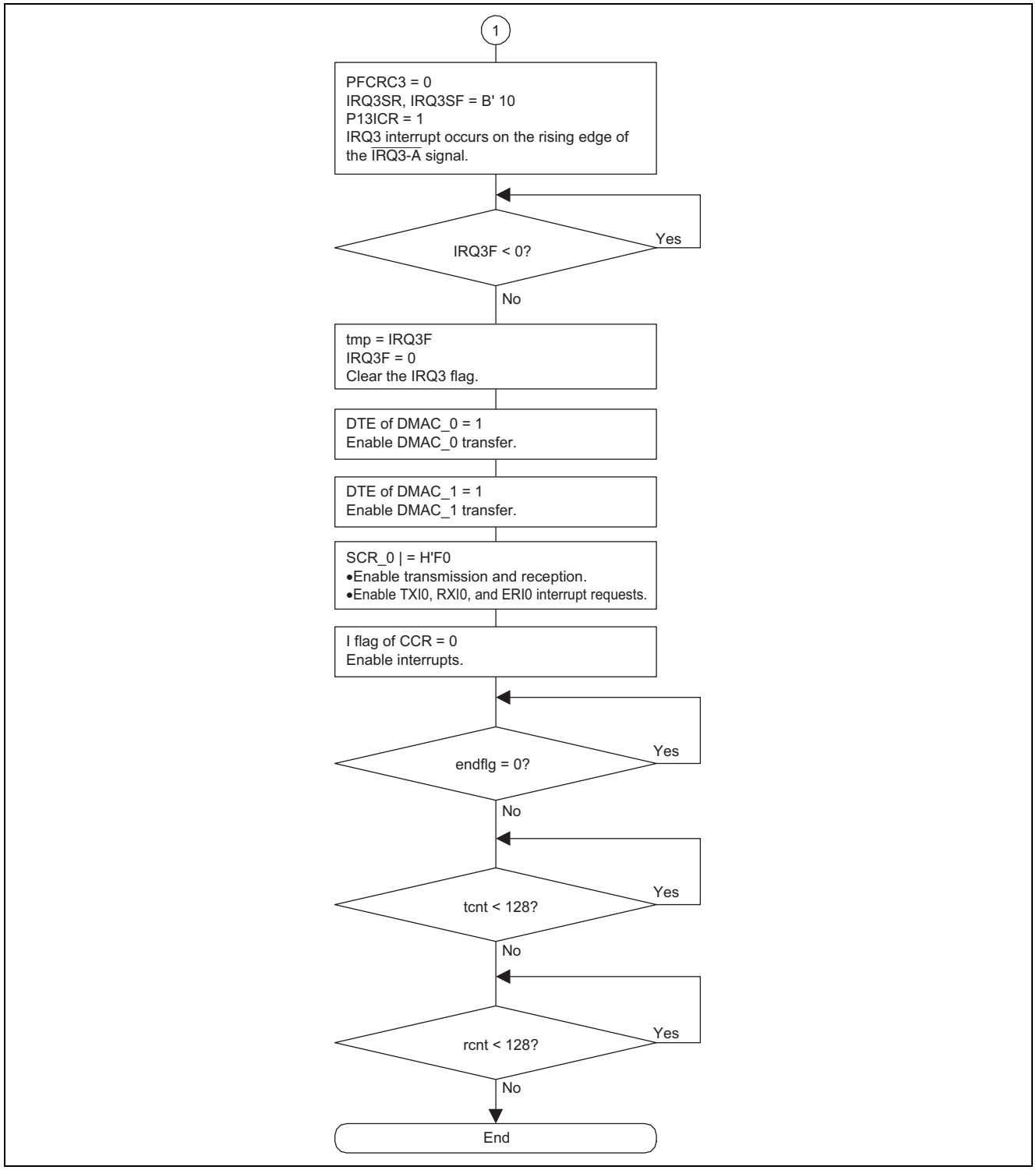
Note: * Only 0 can be written here, to clear the flag.

- Smart card mode register_0 (SCMR_0) Number of bits: 8 Address: H'FFFF86

Bit	Bit Name	Setting	R/W	Description
0	SMIF	0	R/W	Smart Card Interface Mode Select 0: Operation is in the normal asynchronous or clock synchronous mode. 1: Operation is in smart card interface mode.

5. Flowchart


main
i = 0
i < 128?
No
Yes
rcv_dt [i] = 0
i ++
Clear flags:
endflg = 0
errbuf = 0
rcnt = 0
tcnt = 0
DMAC0_trs_init ()
Initial setting of DMAC_0
DMAC1_rcv_init ()
Initial setting of DMAC_1
Clear TE and RE of SCR_0.
Bit 1 of P2ICR = 1
Set P21 (RxD0) pin as an input.
CKE1 and CKE0 of SCR_0 = B'00
Select the clock source as the internal baud rate generator.
SMR_0 = H'00
SCMR_0 &= H'F2
Communications format settings:
•Asynchronous mode
•Data length: 8 bits
•No parity bit
•1 stop bit
BRR = 25
Operate at the bit rate of 38,400 bps when Pϕ = 32 MHz.
i = 0
i ++
Wait 1-bit period
i < 850?
No
Yes
tmp = SSR_0
SSR_0 &= H'87
Clear RDRF, ORER, FER, and PER of SSR_0 to 0.
1


1
PFCRC3 = 0
IRQ3SR, IRQ3SF = B' 10
P13ICR = 1
IRQ3 interrupt occurs on the rising edge of the IRQ3-A signal.
IRQ3F < 0?
Yes
No
tmp = IRQ3F
IRQ3F = 0
Clear the IRQ3 flag.
DTE of DMAC_0 = 1
Enable DMAC_0 transfer.
DTE of DMAC_1 = 1
Enable DMAC_1 transfer.
SCR_0 | = H'F0
•Enable transmission and reception.
•Enable TXI0, RXI0, and ERI0 interrupt requests.
I flag of CCR = 0
Enable interrupts.
endflg = 0?
Yes
No
tcnt < 128?
Yes
No
rcnt < 128?
Yes
No
End

5.7.4 DMAC0_trs_init Function

1. Functional overview
   DMAC_0 initialization. Sets the transfer processing by TXI0 interrupts from the transmitted data holding area to TDR_0.
2. Arguments
   None
3. Return values
   None
4. Description of internal registers used
   The internal registers used in this sample task are described below. Note that the settings shown below are not the initial values but the values used in this sample task.

- DMA source address register_0 (DSAR_0) Number of bits: 32 Address: H'FFFC00
  Function: DSAR_0 specifies the source address for the transfer.
  Setting: &trs_dt

- DMA destination address register_0 (DDAR_0) Number of bits: 32 Address: H'FFFC04
  Function: DDAR_0 specifies the destination address for the transfer.
  Setting: &TDR_0

- DMA transfer count register_0 (DTCR_0) Number of bits: 32 Address: H'FFFC0C
  Function: DTCR_0 selects the amount of data to be transferred (total amount for transfer).
  Setting: 128

- DMA mode control register_0 (DMDR_0) Number of bits: 32 Address: H'FFFC14

Bit	Bit Name	Setting	R/W	Description
31	DTE	0	R/W	Data Transfer Enable 0: Disables data transfer. 1: Enables data transfer.
26	NRD	0	R/W	Next Request Delay 0: Starts accepting the next transfer request after completion of the current transfer. 1: Starts accepting the next transfer request one cycle after completion of the current round of transfer.
17	ESIF	0	R/(W)*	Transfer Escape Interrupt Flag 0: A transfer escape end interrupt request has not been issued. 1: A transfer escape end interrupt request has been issued.
16	DTIF	0	R/(W)*	Data Transfer Interrupt Flag 0: A transfer end interrupt request has not been issued by the transfer counter. 1: A transfer end interrupt request has been issued by the transfer counter.
15	DTSZ1	0	R/W	Data Access Size 1 and 0
14	DTSZ0	0	R/W	01: Data access size for transfer is in bytes (8 bits).
13	MDS1	0	R/W	Transfer Mode Select 1 and 0
12	MDS0	0	R/W	00: Sets the normal transfer mode.
9	ESIE	0	R/W	Transfer Escape Interrupt Enable 0: Disables transfer escape interrupt requests. 1: Enables transfer escape interrupt requests.
8	DTIE	1	R/W	Data Transfer End Interrupt Enable 0: Disables transfer end interrupt requests. 1: Enables transfer end interrupt requests.
7	DTF1	1	R/W	Data Transfer Factor 1 and 0
6	DTF0	0	R/W	10: DMAC activation source is an on-chip module interrupt.
5	DTA	1	R/W	Data Transfer Acknowledge When DTF1 and DTF0 are set to H'10, which selects execution of DMA transfer in response to an internal module interrupt, this bit enables or disables clearing of the source flag selected by DMRSR. 0: Source flag for the internal module interrupt is not cleared. 1: Source flag for the internal module interrupt is cleared.

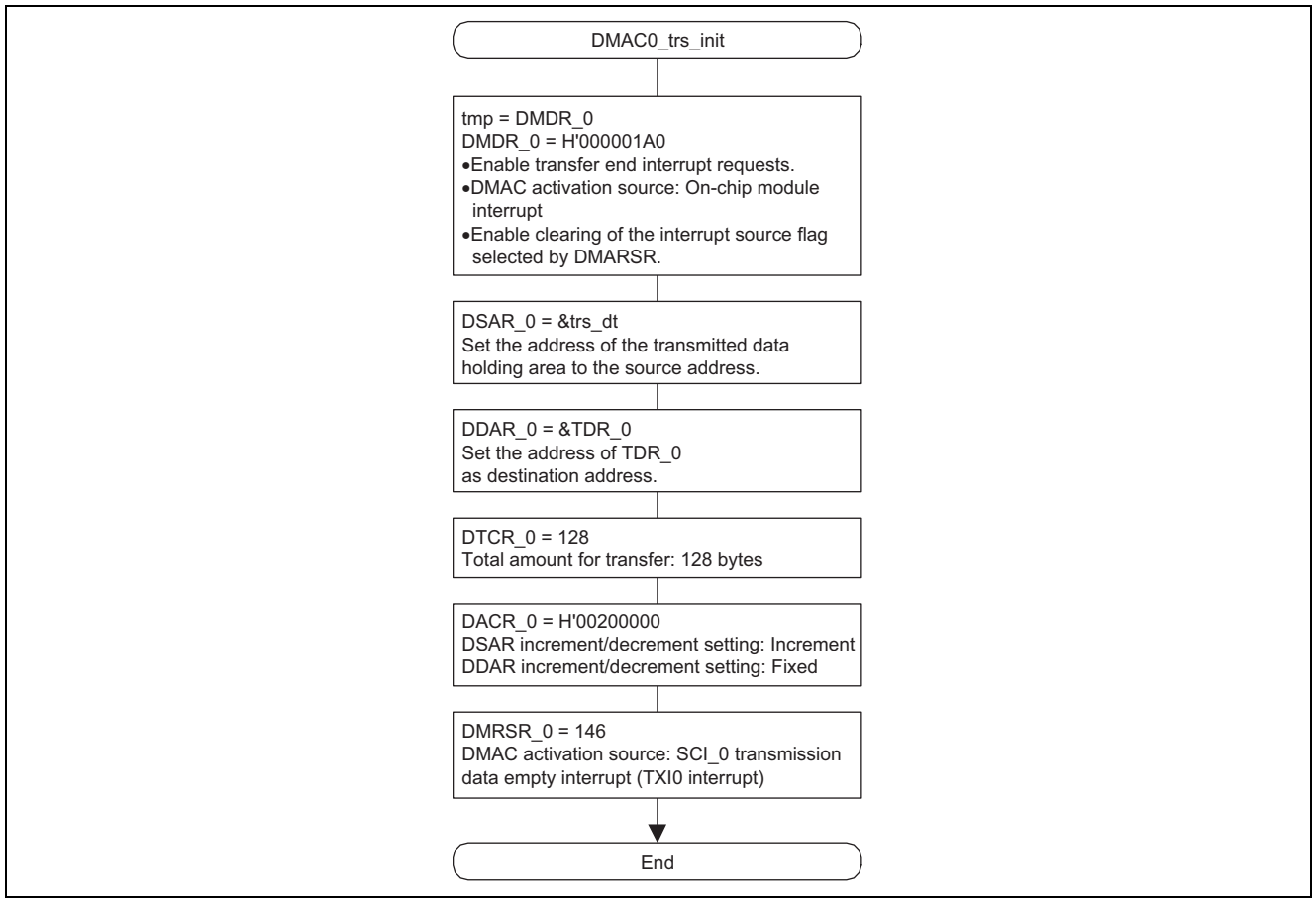
Note: * Only 0 can be written here, to clear the flag.

- DMA address control register_0 (DACR_0) Number of bits: 32 Address: H'FFFC18

Bit	Bit Name	Setting	R/W	Description
31	AMS	0	R/W	Address Mode Select 0: Dual address mode 1: Single address mode
21	SAT1	1	R/W	Source Address Update Mode 1 and 0
20	SAT0	0	R/W	10: Increment the source address.
17	DAT1	0	R/W	Destination Address Update Mode 1 and 0
16	DAT0	0	R/W	00: Destination address is fixed.

- DMA module request select register_0 (DMRSR_0) Number of bits: 8 Address: H'FFFD20
  Function: DMRSR_0 specifies the source of on-chip module interrupts. The setting 146 corresponds to DMAC activation by SCI_0 transmission data empty interrupts (TXI0 interrupts).
  Settings: 146

5. Flowchart



5.7.5 DMAC1_rcv_init Function

1. Functional overview
   DMAC_1 initialization. Sets the transfer processing by RXI0 interrupts from RDR_0 to received data holding area.
2. Arguments
   None
3. Return values
   None
4. Description of internal registers used
   The internal registers used in this sample task are described below. Note that the settings shown below are not the initial values but the values used in this sample task.

- DMA source address register_1 (DSAR_1) Number of bits: 32 Address: H'FFFC20
  Function: DSAR_1 specifies the source address for the transfer.
  Setting: &RDR_0

- DMA destination address register_1 (DDAR_1) Number of bits: 32 Address: H'FFFC24
  Function: DDAR_1 specifies the destination address for the transfer.
  Setting: &rcv_dt

- DMA transfer count register_1 (DTCR_1) Number of bits: 32 Address: H'FFFC2C
  Function: DTCR_1 selects the amount of data to be transferred (total amount for transfer).
  Setting: 128

- DMA mode control register_1 (DMDR_1) Number of bits: 32 Address: H'FFFC34

Bit	Bit Name	Setting	R/W	Description
31	DTE	0	R/W	Data Transfer Enable 0: Disables data transfer. 1: Enables data transfer.
26	NRD	0	R/W	Next Request Delay 0: Starts accepting the next transfer request after completion of the current transfer. 1: Starts accepting the next transfer request one cycle after completion of the current round of transfer.
17	ESIF	0	R/(W)*	Transfer Escape Interrupt Flag 0: A transfer escape end interrupt request has not been issued. 1: A transfer escape end interrupt request has been issued.
16	DTIF	0	R/(W)*	Data Transfer Interrupt Flag 0: A transfer end interrupt request has not been issued by the transfer counter. 1: A transfer end interrupt request has been issued by the transfer counter.
15	DTSZ1	0	R/W	Data Access Size 1 and 0
14	DTSZ0	0	R/W	01: Data access size for transfer is in bytes (8 bits).
13	MDS1	0	R/W	Transfer Mode Select 1 and 0
12	MDS0	0	R/W	00: Sets the normal transfer mode.
9	ESIE	0	R/W	Transfer Escape Interrupt Enable 0: Disables transfer escape interrupt requests. 1: Enables transfer escape interrupt requests.
8	DTIE	1	R/W	Data Transfer End Interrupt Enable 0: Disables transfer end interrupt requests. 1: Enables transfer end interrupt requests.
7	DTF1	1	R/W	Data Transfer Factor 1 and 0
6	DTF0	0	R/W	10: DMAC activation source is an on-chip module interrupt.
5	DTA	1	R/W	Data Transfer Acknowledge When DTF1 and DTF0 are set to H'10, which selects execution of DMA transfer in response to an internal module interrupt, this bit enables or disables clearing of the source flag selected by DMRSR. 0: Source flag for the internal module interrupt is not cleared. 1: Source flag for the internal module interrupt is cleared.

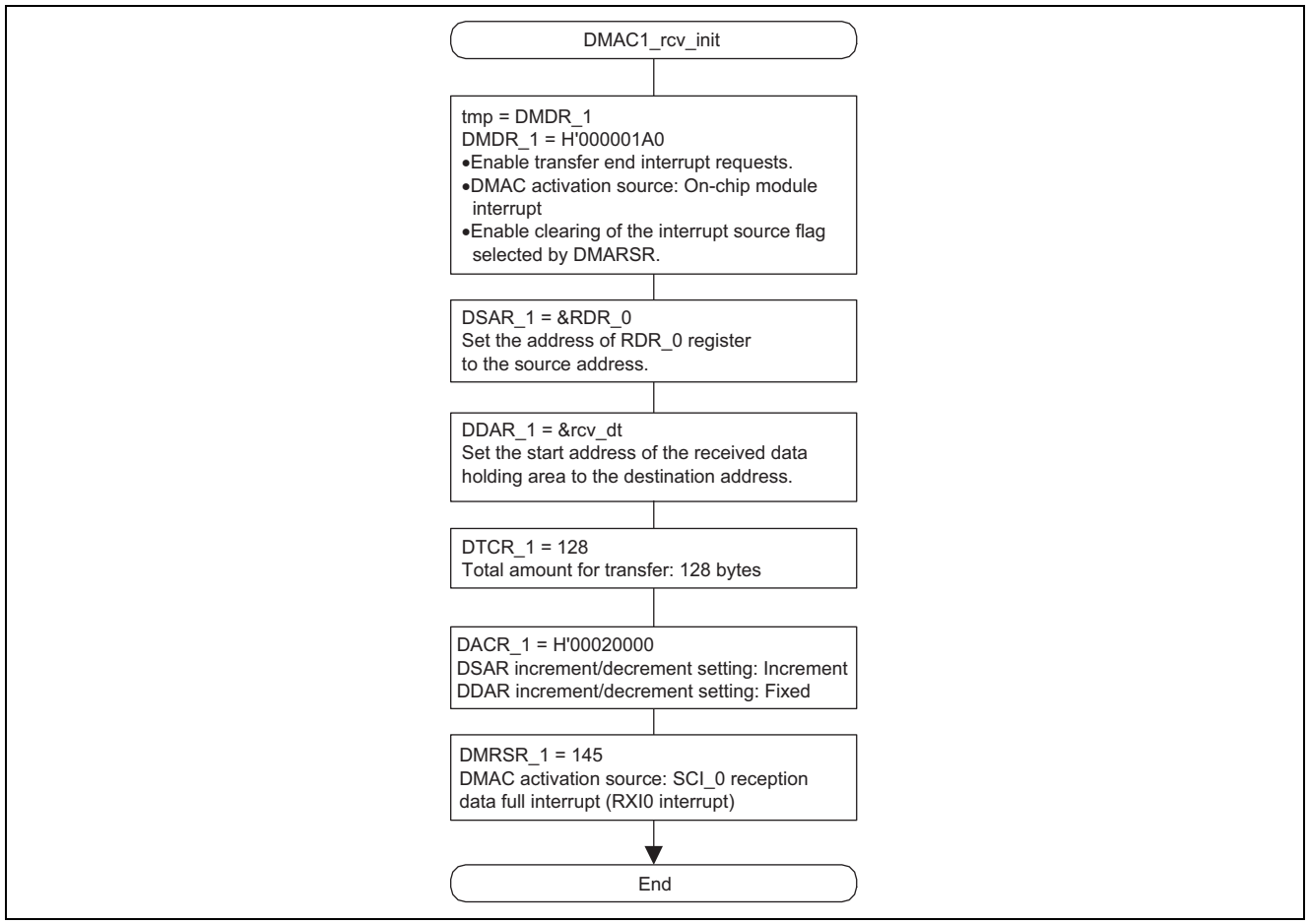
Note: * Only 0 can be written here, to clear the flag.

- DMA address control register_1 (DACR_1) Number of bits: 32 Address: H'FFFC38

Bit	Bit Name	Setting	R/W	Description
31	AMS	0	R/W	Address Mode Select 0: Dual address mode 1: Single address mode
21	SAT1	0	R/W	Source Address Update Mode 1 and 0
20	SAT0	0	R/W	10: Increment the source address.
17	DAT1	1	R/W	Destination Address Update Mode 1 and 0
16	DAT0	0	R/W	10: Destination address is incremented.

- DMA module request select register_1 (DMRSR_1) Number of bits: 8 Address: H'FFFD21
  Function: DMRSR_1 specifies the source of on-chip module interrupts. The setting 145 corresponds to DMAC activation by SCI_0 reception data full interrupts (RXI0 interrupts).
  Settings: 145

5. Flowchart



5.7.6 dmtend0_init Function

1. Functional overview
   Handler for the DMAC_0 transfer end interrupt. (TEI0 interrupt requests enabled, TXI0 interrupt requests disabled, and DMAC_0 transfer end interrupt requests disabled.)
2. Arguments
   None
3. Return values
   None
4. Description of internal registers used
   The internal registers used in this sample task are described below. Note that the settings shown below are not the initial values but the values used in this sample task.

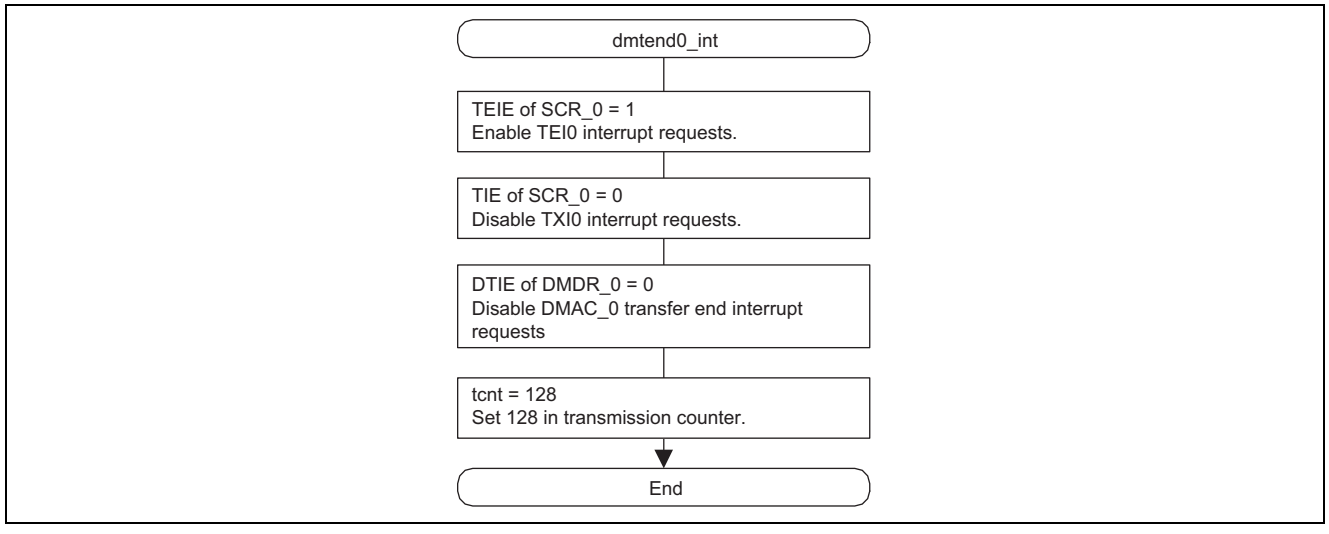
- Serial control register_0 (SCR_0) Number of bits: 8 Address: H'FFFF82

Bit	Bit Name	Setting	R/W	Description
7	TIE	0	R/W	Transmit Interrupt Enable 0: Disables TXI interrupt requests. 1: Enables TXI interrupt requests.
2	TEIE	1	R/W	Transmit End Interrupt Enable 0: Disables TEI interrupt requests. 1: Enables TEI interrupt requests.

- DMA mode control register_0 (DMDR_0) Number of bits: 32 Address: H'FFFC14

Bit	Bit Name	Setting	R/W	Description
8	DTIE	1	R/W	Data Transfer End Interrupt Enable 0: Disables transfer end interrupt requests. 1: Enables transfer end interrupt requests.

5. Flowchart



5.7.7 dmtend1_init Function

1. Functional overview
   Handler for the DMAC_1 transfer end interrupt. (The reception in SCI_0, RXI0 and ERI0 interrupt requests, and DMAC_1 transfer end interrupt requests disabled.)
2. Arguments
   None
3. Return values
   None
4. Description of internal registers used
   The internal registers used in this sample task are described below. Note that the settings shown below are not the initial values but the values used in this sample task.

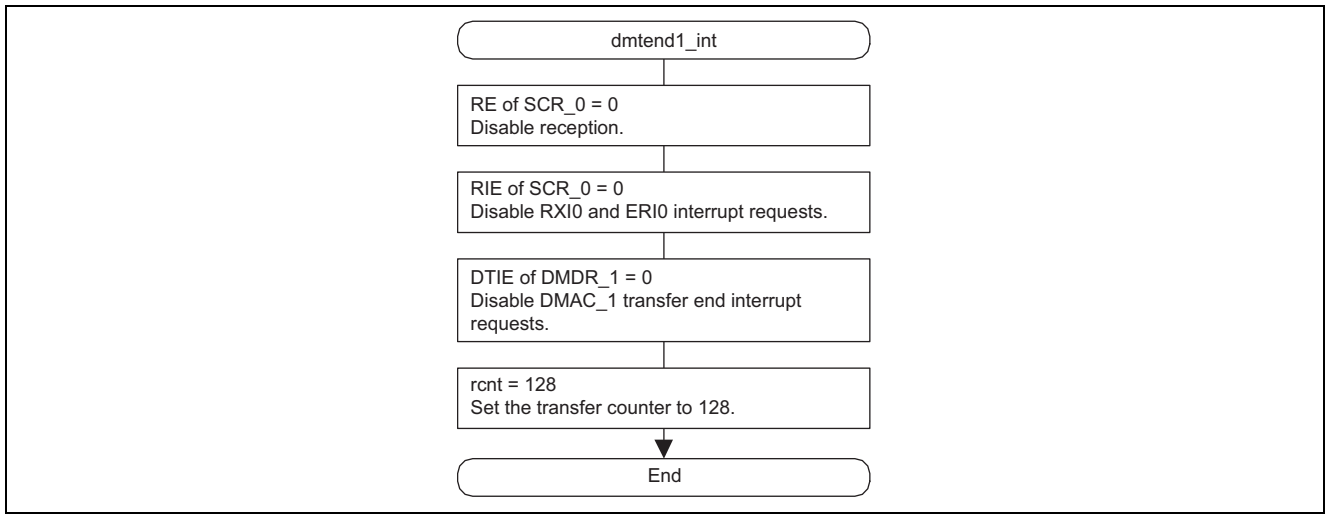
- Serial control register_0 (SCR_0) Number of bits: 8 Address: H'FFFF82

Bit	Bit Name	Setting	R/W	Description
6	RIE	0	R/W	Receive Interrupt Enable 0: Disables RXI and ERI interrupt requests. 1: Enables RXI and ERI interrupt requests.
4	RE	0	R/W	Receive Enable 0: Disables reception. 1: Enables reception.

- DMA mode control register_1 (DMDR_1) Number of bits: 32 Address: H'FFFC34

Bit	Bit Name	Setting	R/W	Description
8	DTIE	0	R/W	Data Transfer End Interrupt Enable 0: Disables transfer end interrupt requests. 1: Enables transfer end interrupt requests.

5. Flowchart



5.7.8 eri0_int Function

1. Functional overview
   Handler for the SCI_0 reception error interrupts (ERI0 interrupts). Writes error data to RAM and initializes SSR_0.
2. Arguments
   None
3. Return values
   None
4. Description of internal registers used
   The internal registers used in this sample task are described below. Note that the settings shown below are not the initial values but the values used in this sample task.

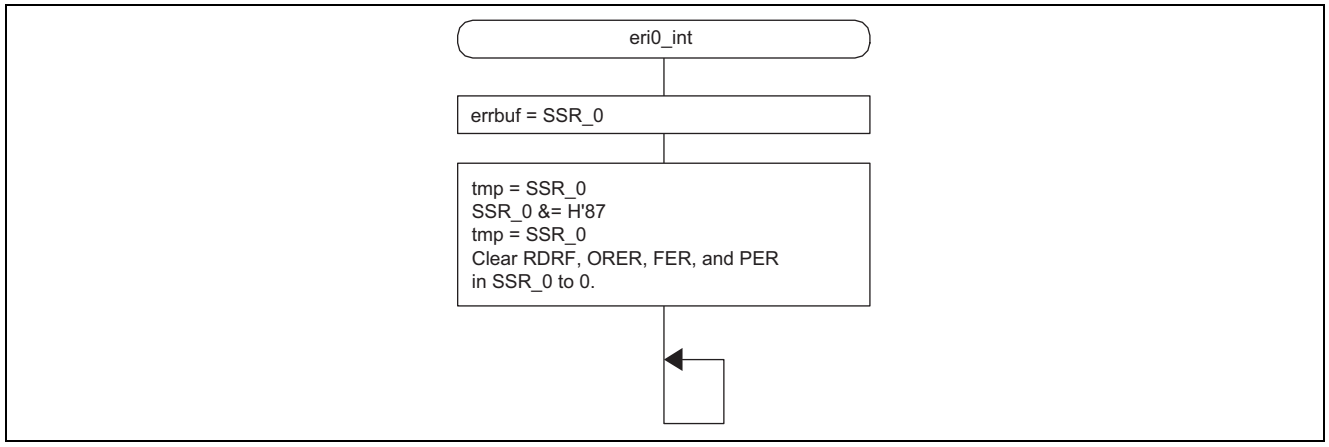
- Serial status register_0 (SSR_0) Number of bits: 8 Address: H'FFFF84

Bit	Bit Name	Setting	R/W	Description
6	RDRF	0	R/(W)*	Receive Data Register Full Indicates whether RDR holds received data. [Setting conditions] • The normal end of serial reception and the transfer of received data from RSR to RDR. [Clearing conditions] • Writing of 0 to RDRF after having read RDRF = 1 (when using an interrupt and having the CPU clear it, be sure to read the flag after having written 0 to it.) • The RDRF flag is not affected and retains its previous value even though the RE bit in SCR is cleared to 0. Note that when the next reception is completed while the RDRF flag is being set to 1, an overrun error occurs and the received data are lost.
5	ORER	0	R/(W)*	Overrun Error [Setting condition] • Occurrence of an overrun during reception [Clearing condition] • Writing of 0 to ORER after having read ORER = 1 (when using an interrupt and having the CPU clear it, be sure to read the flag after having written 0 to it.)

Bit	Bit Name	Setting	R/W	Description
4	FER	0	R/(W)*	Framing Error [Setting condition] • Occurrence of a framing error during reception [Clearing condition] • Writing of 0 to FER after having read FER = 1 (When using an interrupt and clearing by CPU, be sure to read a flag after having written 0.)
3	PER	0	R/(W)*	Parity Error [Setting condition] • Occurrence of a parity error during reception [Clearing condition] • Writing of 0 to PER after having read PER = 1 (when using an interrupt and having the CPU clear it, be sure to read the flag after having written 0 to it.)

Note: * Only 0 can be written here, to clear the flag.

5. Flowchart



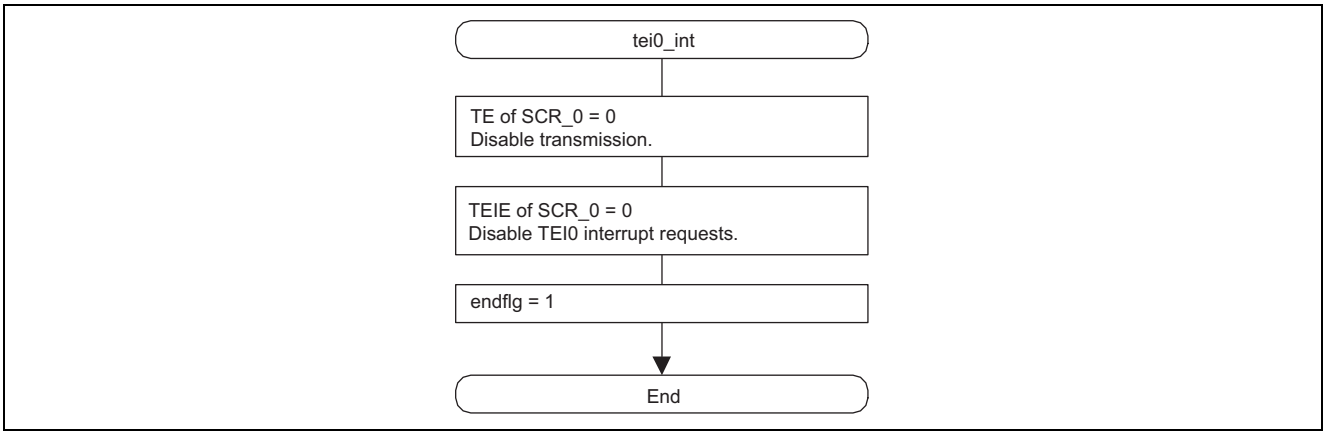
5.7.9 tei0_int Function

1. Functional overview
   Handler for the SCI_0 transmission end interrupts (TEI0 interrupts). (The transmission in SCI_0 and TEI0 interrupt requests disabled.)
2. Arguments
   None
3. Return values
   None
4. Description of internal registers used
   The internal registers used in this sample task are described below. Note that the settings shown below are not the initial values but the values used in this sample task.

- Serial control register_0 (SCR_0) Number of bits: 8 Address: H'FFFF82

Bit	Bit Name	Setting	R/W	Description
5	TE	0	R/W	Transmit Enable 0: Disables transmission. 1: Enables transmission.
2	TEIE	0	R/W	Transmit End Interrupt Enable 0: Disables TEI interrupt requests. 1: Enables TEI interrupt requests.

5. Flowchart



6. Documents for Reference (Note)

- Hardware manual
  H8SX/1653 Group Hardware Manual
  The most up-to-date version of this document is available on the Renesas Technology Website.
- Technical News/Technical Update
  The most up-to-date information is available on the Renesas Technology Website.

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