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APPLICATION NOTE

Using Compare Match Function for PWM Output

Introduction

Using Compare Match Function for PWM Output

Target Device

H8/300H Tiny Series H8/3664

Contents

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1. Specifications

1. Using Compare Match Function for PWM Output
2. The output PWM waveform's cycle is set in timer constant register A (TCORA).
3. How long the output PWM waveform is high (high width) is set in timer constant register B (TCORB).
4. In this sample task, a PWM waveform with a 2.04-ms cycle and a duty cycle delayed by 6.25% (must be between 6.25% and 93.75%) every cycle, is output.

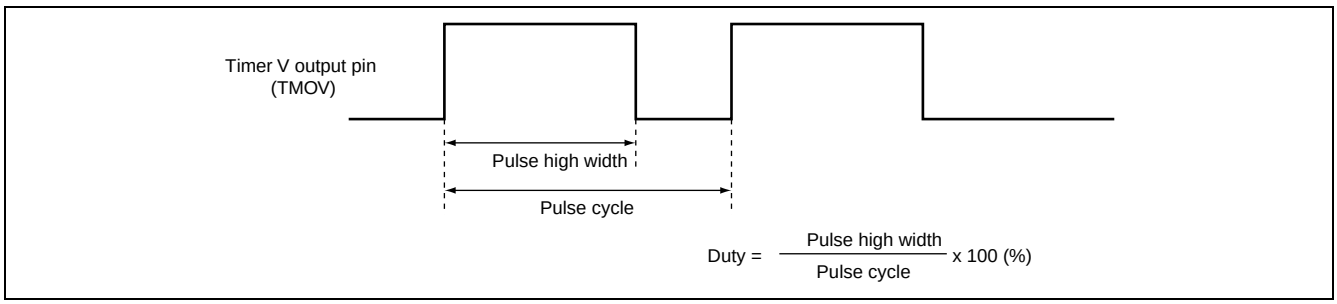


Figure 1.1 PWM Output

2. Description of Functions Used

In this sample task, a PWM waveform is output from the TMOV output pin by the compare match function of timer V.

Figure 2.1 is a block diagram of the compare match function of timer V. The elements of the block diagram are described below.

- The system clock (ϕ) is a 16-MHz OSC clock that is used as a reference clock for operating the CPU and peripheral functions.
- Prescaler S (PSS) is a 13-bit counter with clock input of ϕ. PSS is incremented every cycle.
- Timer counter V (TCNTV) is an 8-bit readable/writable up-counter that is incremented by internal or external clock input. The clock source can be selected from a total of nine clocks: six clocks obtained by dividing the system clock (ϕ), and three external clocks.
- Timer control register V0 (TCRV0) is an 8-bit readable/writable register that selects the TCNTV input clock, controls clearing of TCNTV, and enables individual interrupt requests. In this sample task, system clock/128 is selected as the TCNTV input clock, compare match A is selected as the clearing condition of TCNTV, and interrupt requests by compare match A are enabled.
- Timer control/status register V (TCSRV) is an 8-bit register that sets compare match flags and the timer overflow flag, and controls compare match output. In this sample task, 0 is output from the TMOV pin when compare match B occurs, and 1 is output from the TMOV pin when compare match A occurs.
- Timer control register V1 (TCRV1) is an 8-bit readable/writable register that selects the TCNTV input clock together with TCRV0.
- Timer constant register A (TCORA) is an 8-bit readable/writable register that is compared with TCNTV at all times. When the TCORA and TCNTV contents match, compare match A occurs, and as a result, 1 is output from the TMOV pin and TCNTV is cleared to H'00.

- Timer constant register B (TCORB) is an 8-bit readable/writable register that is compared with TCNTV at all times. When the TCORB and TCNTV contents match, compare match B occurs, and as a result, 0 is output from the TMOV pin.
- The TCNTV contents are compared with the TCORA and TCORB contents at all times. When the TCNTV contents match the TCORA and TCORB contents, compare match flag A (CMFA) and compare match flag B (CMFB) in TCSRV are set to 1, respectively. If the corresponding compare match interrupt enable A (CMIEA) or compare match interrupt enable B (CMIEB) in TCRV0 is set to 1 at this time, a CPU interrupt is requested.
- A PWM waveform is output from the timer V output (TMOV) pin.

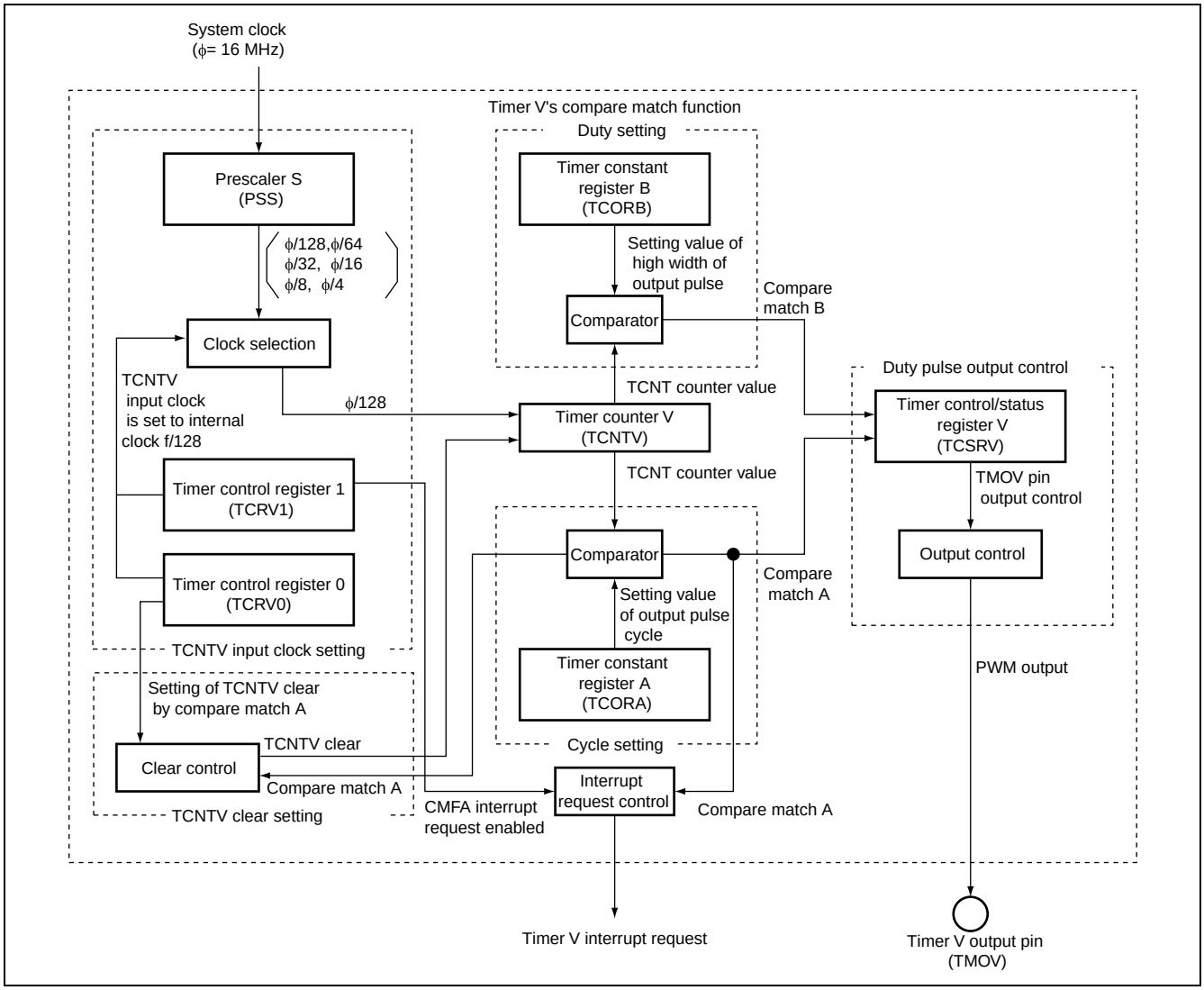


Figure 2.1 Timer V's Compare Match Function

Figure 2.2 shows how to set the cycle and duty cycle of the output PWM waveform in this sample task.

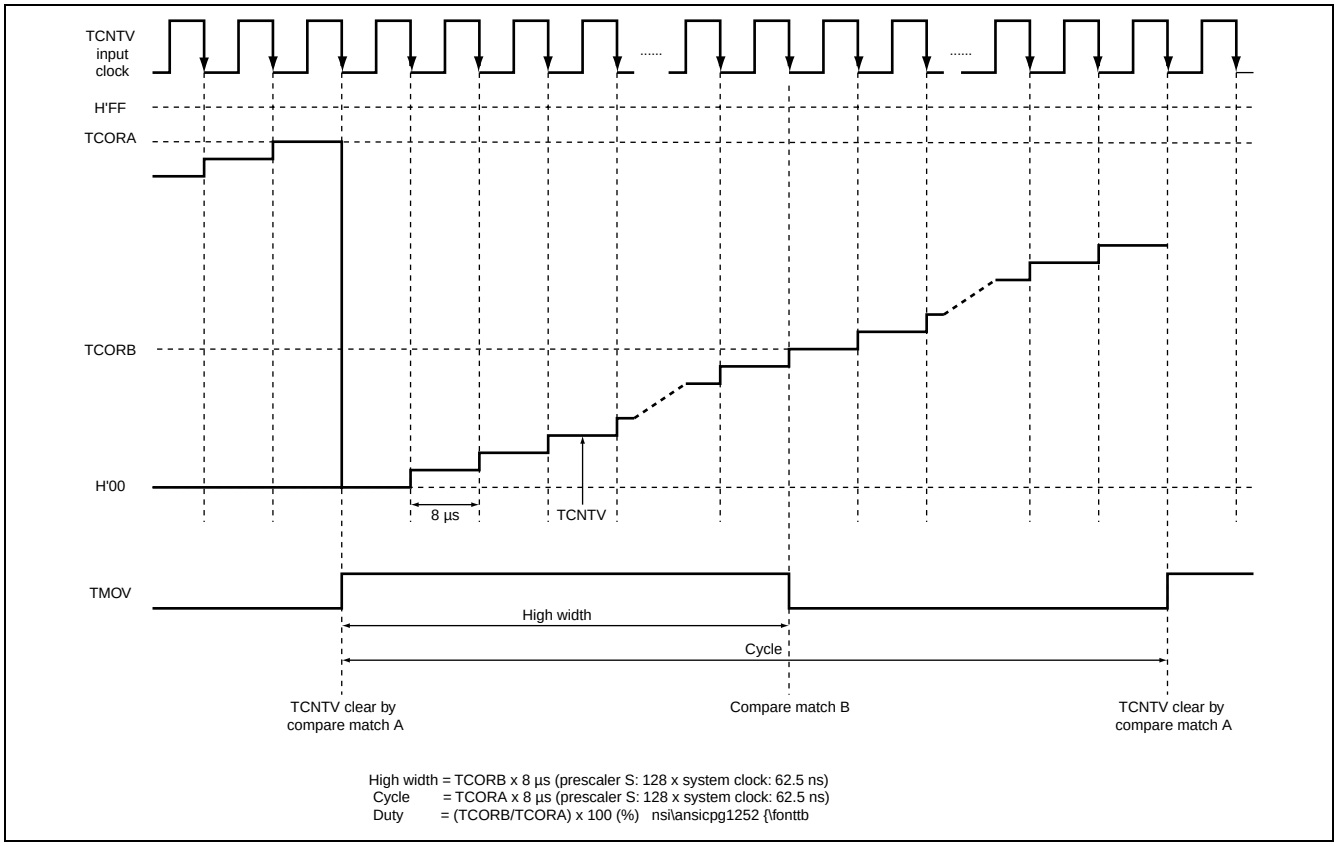


Figure 2.2 Setting of Cycle and Duty of PWM Waveform

Figure 2.3 shows the timing for rewriting TCORB to increase the duty cycle.

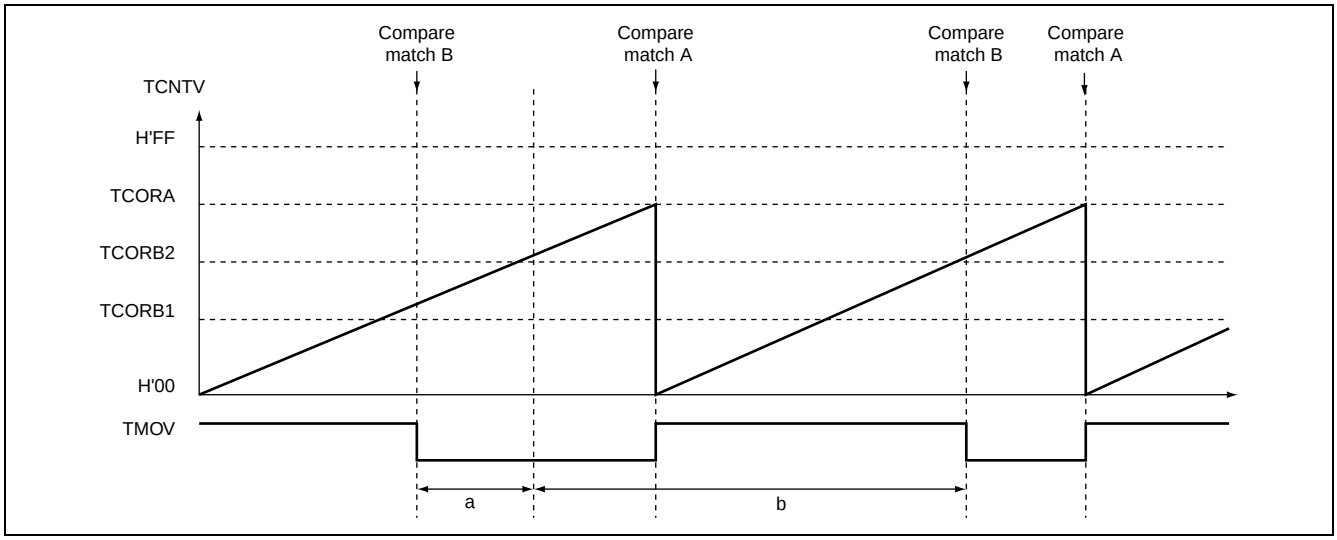


Figure 2.3 TCORB Rewrite Timing for Higher Duty Cycle

- TCORB is updated to the new value immediately after being written to. Therefore, if TCORB is rewritten during period a in figure 2.3 to increase the duty cycle, compare match B occurs consecutively, and a normal PWM waveform is not output. Accordingly, TCORB must be rewritten during period b, as shown in figure 2.3.
- In this sample task, TCORB is rewritten during the compare match A interrupt handling using a compare match A interrupt.

Figure 2.4 shows the timing for rewriting TCORB to reduce the duty cycle.

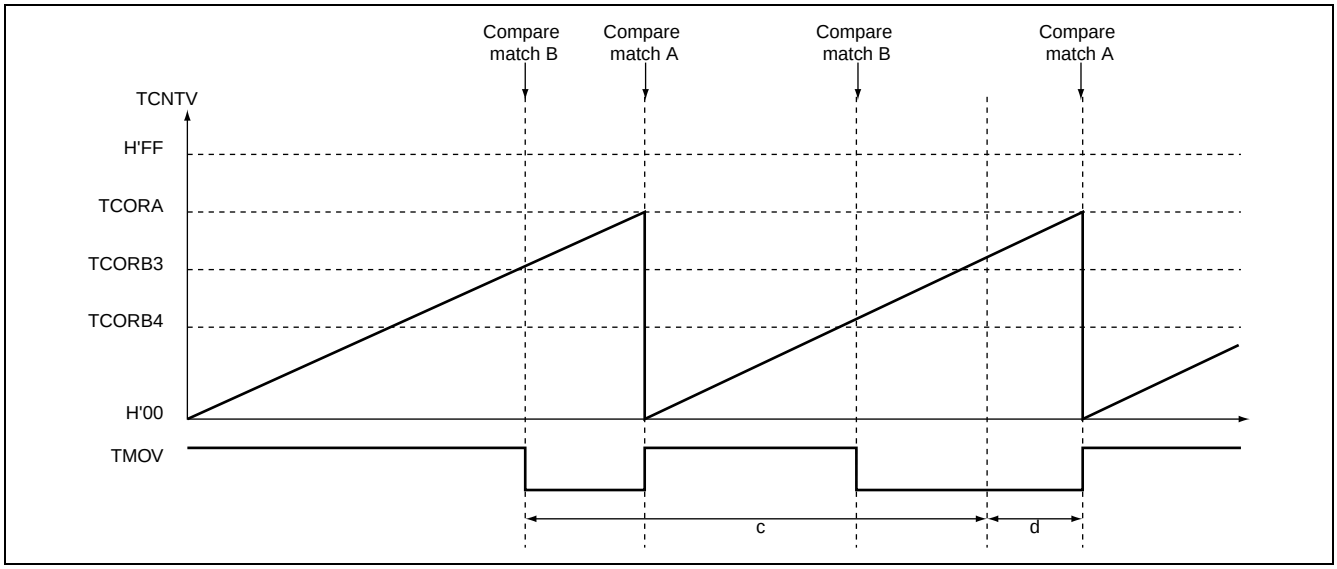


Figure 2.4 TCORB Rewrite Timing for Lower Duty Cycle

- TCORB is updated to the new value immediately after being written to. Therefore, if TCORB is rewritten during period d in figure 2.4 to reduce the duty cycle, the following compare match B does not occur, and a normal PWM waveform is not output. Accordingly, TCORB must be rewritten during period c, as shown in figure 2.4.
- In this sample task, TCORB is rewritten during the compare match A interrupt handling using a compare match A interrupt.

Table 2.1 lists the function allocation for this sample task. The functions listed in table 2.1 are allocated so that a PWM is output by the compare match function of timer V.

Table 2.1 Function Allocation

Function	Description
PSS	13-bit counter with system clock input
TCNTV	8-bit counter with clock input of system clock/128
TCORA	Sets the PWM output cycle
TCORB	Sets the high width of PWM output
TCRV0	Selects the TCNTV input clock and TCNTV clearing
TCRV1	Selects the TCNTV input clock
TCSRV	Controls compare match output
TMOV	PWM output pin

3. Description of Operations

Figure 3.1 shows this sample task's principle of operation. The hardware and software processing shown in figure 3.1 applies the compare match function of timer V for PWM output.

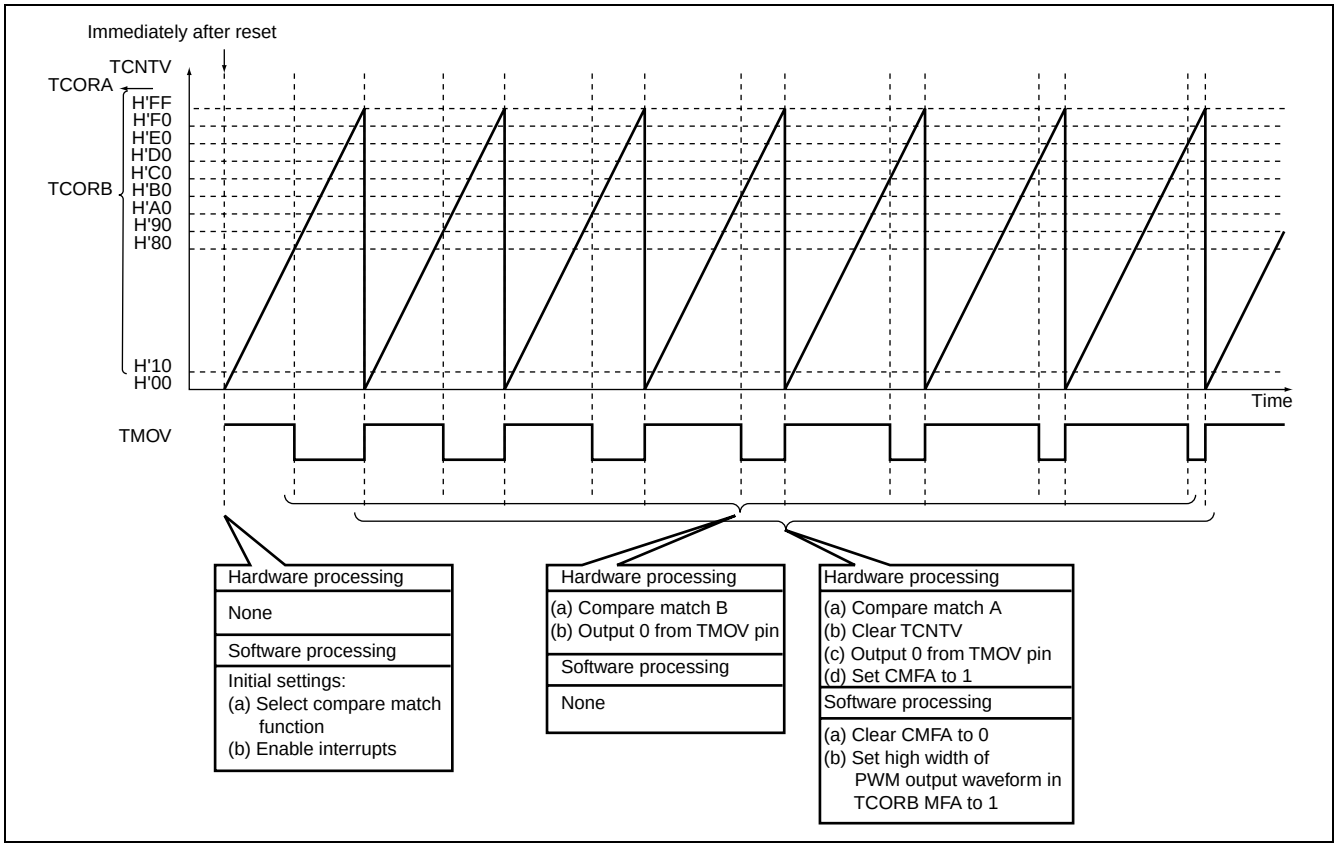


Figure 3.1 Operation Principle: Using Compare Match Function of Timer V for PWM Output

4. Description of Software

4.1 Description of Modules

Table 4.1 describes the software used in this sample task.

Table 4.1 Description of Modules

Module Name	Label Name	Function
Main routine	main	Selects the compare match function and enables interrupts.
Compare match A	tvint	During the timer V interrupt handling routine, rewrites TCORB.

4.2 Description of Arguments

No arguments are used in this sample task.

4.3 Description of Internal Registers

Table 4.2 describes the internal registers used in this sample task.

Table 4.2 Description of Internal Registers

Register	Name	Function	Address	Setting
TCRV0	CMIEA	Timer control register V0 (compare match interrupt enable A):	H'FFA0	
		When CMIEA is set to 1, CMFA interrupt requests are enabled.	Bit 6	1
		Timer control register V0 (counter clear 1 and 0):	H'FFA0	
	CCLR1	When CCLR1 is cleared to 0 and CCLR0 is set to 1, TCNTV is cleared by compare match A.	Bit 4	CCLR1 = 0
	CCLR0		Bit 3	CCLR1 = 1
		Timer control register V0 (clock select 2 to 0):	H'FFA0	
	CKS2	When CKS2 is cleared to 0, and CKS1, CKS0, and ICKS0 (in TCRV1) are all set to 1, TCNTV is incremented at the falling edge of system clock/128.	Bit 2	CKS2 = 0
	CKS1		Bit 1	CKS1 = 1
	CKS0		Bit 0	CKS0 = 1
TCSRV	CMFA	Timer control/status register V (compare match flag A):	H'FFA1	
		When CMFA is cleared to 0, compare match A has not occurred.	Bit 6	0
		When CMFA is set to 1, compare match A has occurred.		
		Timer control/status register V (output select 3 to 0):	H'FFA1	
	OS3	When OS3 and OS0 are both cleared to 0, and OS2 and OS1 are both set to 1, the TMOV pin output is 0 at compare match B and 1 at compare match A.	Bit 3	OS3 = 0
	OS2		Bit 2	OS2 = 1
	OS1		Bit 1	OS1 = 1
	OS0		Bit 0	OS0 = 0

Table 4.2 Description of Internal Registers (cont)

Register Name		Function	Address	Setting
TCORA		Time constant register A: When TCORA is set to H'FF, compare match A occurs when the TCNTV value has become H'FF.	H'FFA2	H'FF
TCORB		Time constant register B: When TCORB is set to H'80, compare match B occurs when the TCNTV value has become H'80.	H'FFA3	H'80
TNCTV		Timer counter V: 8-bit up-counter incremented by clock input of system clock/128	H'FFA4	H'00
TCRV1	ICKS0	Timer control register V1 (internal clock select 0): When ICKS0 is set to 1, the TCNTV clock source is set to system clock/128.	H'FFA5 Bit 0	 1

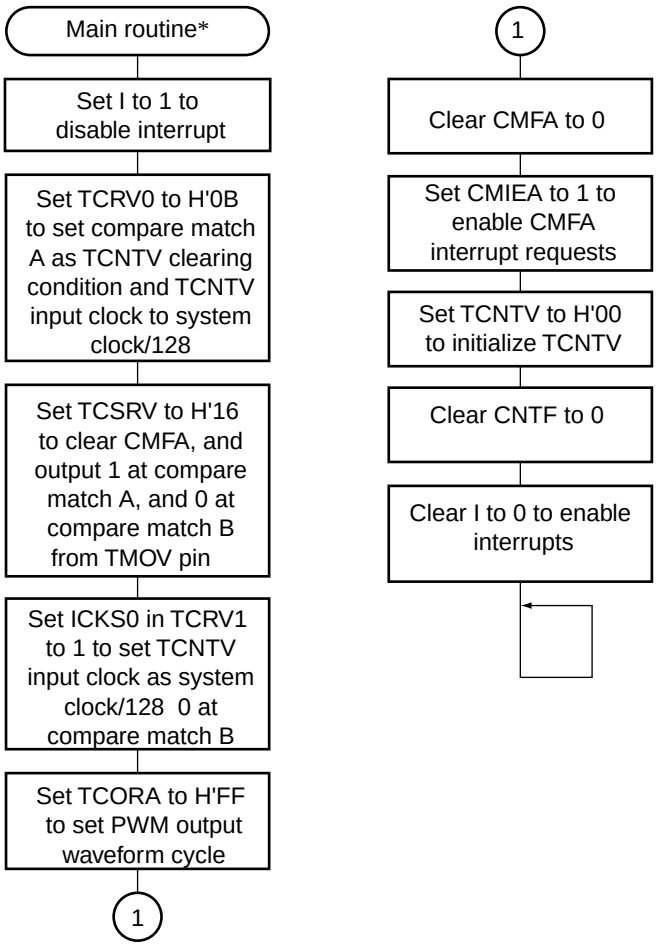
4.4 Description of RAM

Table 4.3 describes the RAM used in this sample task.

Table 4.3 Description of RAM

Label Name		Function	Address	Used in
USRF	CNTF	Flag for judging whether or not to increment or decrement the TCORB value	H'FB80 Bit 0	Main routine Compare match A

5. Flowcharts



Note: * In this sample task, the stack pointer is set in INIT.SRC (assembly).

Figure 5.1 Flowchart for Main Routine

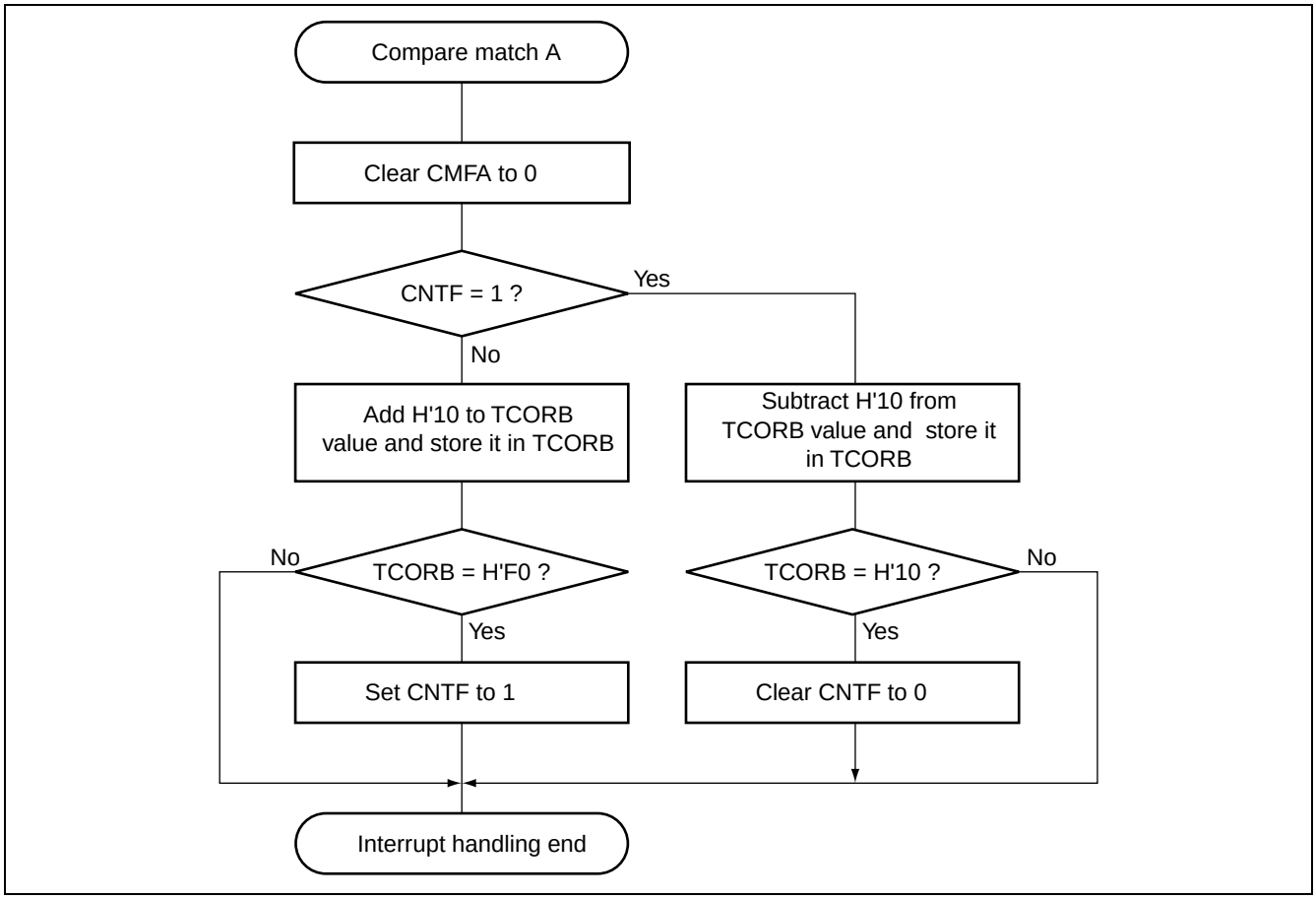


Figure 5.2 Flowchart for Timer V Interrupt Handling Routine

6. Program Listing

INIT.SRC (Program listing)

```
      .EXPORT  _INIT
      .IMPORT  _main
  ;
      .SECTION    P,CODE
  _INIT:
      MOV.W    #H'FF80,R7
      LDC.B    #B'10000000,CCR
      JMP      @_main
  ;
      .END
```

```
/************************************************************/
/*                                                          */
/*    H8/300H Tiny Series -H8/3664-                         */
/*    Application Note                                      */
/*                                                          */
/*    'PWM Output by Compare Match Function'                */
/*                                                          */
/*    Function                                              */
/*    :Timer V Compare Match                                */
/*                                                          */
/*    External Clock : 16MHz                                */
/*    Internal Clock : 16MHz                                */
/*    Sub Clock      : 32.768kHz                            */
/*                                                          */
/************************************************************/

#include    <machine.h>
```

```
/************************************************************/
/*    Symbol Defnition                                      */
/************************************************************/

struct BIT {
    unsigned char    b7:1;      /* bit7 */
    unsigned char    b6:1;      /* bit6 */
    unsigned char    b5:1;      /* bit5 */
    unsigned char    b4:1;      /* bit4 */
    unsigned char    b3:1;      /* bit3 */
    unsigned char    b2:1;      /* bit2 */
    unsigned char    b1:1;      /* bit1 */
    unsigned char    b0:1;      /* bit0 */
};

#define        TCRV0       *(volatile unsigned char *)0xFFA0   /* Time Constant Register V0        */
#define        TCRV0_BIT   (*(struct BIT *)0xFFA0)             /* Timer Control Register V0        */
#define        CMIEB       TCRV0_BIT.b7                        /* Compare Match Interrupt Enable B */
#define        CMIEA       TCRV0_BIT.b6                        /* Compare Match Interrupt Enable A */
#define        OVIE        TCRV0_BIT.b5                        /* Timer Overflow Interrupt Enable  */
#define        CCLR1       TCRV0_BIT.b4                        /* Counter Clear 1                  */
#define        CCLR0       TCRV0_BIT.b3                        /* Counter Clear 0                  */
#define        CKS2        TCRV0_BIT.b2                        /* Clock Select 2                   */
#define        CKS1        TCRV0_BIT.b1                        /* Clock Select 1                   */
#define        CKS0        TCRV0_BIT.b0                        /* Clock Select 0                   */
#define        TCSRV       *(volatile unsigned char *)0xFFA1   /* Timer Control/Status Register V  */
#define        TCSRV_BIT   (*(struct BIT *)0xFFA1)             /* Timer Control/Status Register V  */
#define        CMFB        TCSRV_BIT.b7                        /* Compare Match Flag B             */
#define        CMFA        TCSRV_BIT.b6                        /* Compare Match Flag A             */
#define        OVF         TCSRV_BIT.b5                        /* Timer Overflow Flag              */
#define        OS3         TCSRV_BIT.b3                        /* Output Select 3                  */
#define        OS2         TCSRV_BIT.b2                        /* Output Select 2                  */
#define        OS1         TCSRV_BIT.b1                        /* Output Select 1                  */
#define        OS0         TCSRV_BIT.b0                        /* Output Select 0                  */
#define        TCORA       *(volatile unsigned char *)0xFFA2   /* Time Constant Register A         */
#define        TCORB       *(volatile unsigned char *)0xFFA3   /* Time Constant Register B         */
#define        TCNTV       *(volatile unsigned char *)0xFFA4   /* Timer Counter V                  */
#define        TCRV1_BIT   (*(struct BIT *)0xFFA5)             /* Timer Control Register V1        */
#define        TVEG1       TCRV1_BIT.b4                        /* TRGV Input Edge Select 1         */
```

```
#define        TVEG0       TCRV1_BIT.b3                      /* TRGV Input Edge Select 0         */
#define        TRGE        TCRV1_BIT.b2                      /* TRGV Input Enable                */
#define        ICKS0       TCRV1_BIT.b0                      /* Internal Clock Select 0          */

#pragma        interrupt    (tvint)
/************************************************************/
/*     Function Definition                                  */
/************************************************************/
extern    void    INIT ( void );                             /* SP Set                           */
void      main     ( void );
void      tvint    ( void );

/************************************************************/
/*    RAM define                                            */
/************************************************************/
unsigned char    USRF;                                      /* User Flag Erea                   */

#define        USRF_BIT    (*(struct BIT *)&USRF)
#define        CNTF        USRF_BIT.b0                       /* Counter Flag                     */

/************************************************************/
/*    Vector Address                                        */
/************************************************************/
#pragma    section        V1                                /* VECTOR SECTOIN SET               */
void (*const VEC_TBL1[])(void) = {
/* 0x00 - 0x0f */
    INIT                                                    /* 00 Reset                         */
};
#pragma    section        V2                                /* VECTOR SECTOIN SET               */
void (*const VEC_TBL2[])(void) = {
    tvint                                                   /* 2C Timer V Interrupt             */
};
#pragma    section                                          /* P                                */
```

```
/************************************************************/
/*    Main Program                                          */
/************************************************************/
void main ( void )
{
    set_imask_ccr(1);                                   /* Interrupt Disable                */

    TCRV0 = 0x0B;                                       /* Initialize Compare Match Function  */
    TCSRV = 0x16;                                       /* Initialize TMOV Pin Output Level   */
    ICKS0 = 1;                                          /* Initialize TCNT Input Clock Period */

    TCORA = 0xFF;                                       /* Initialize Compare Match A Value   */
    TCORB = 0x80;                                       /* Initialize Compare Match B Value   */

    CMFA = 0;                                           /* Clear Compare Match Flag A         */
    CMIEA = 1;                                          /* Compare Match A Interrupt Enable   */

    TCNTV = 0;                                          /* Initialize TCNTV                   */

    CNTF = 0;                                           /* Clear CNTF to 0                    */

    set_imask_ccr(0);                                   /* Interrupt Enable                   */

    while(1)    {
        ;
        }
}
```

```
/*********************************************************/
/*    Timer V Interrupt                                  */
/*********************************************************/
void tvint ( void )
{

    CMFA = 0;                                   /* Clear CMFA to 0                */

    if ( CNTF == 1){                            /* CNTF = 1 ?                     */
        TCORB -= 0x10;                          /* Decrement High Width           */
        if ( TCORB == 0x10 ){                   /* High Width = H'10 ?            */
            CNTF = 0;                           /* Clear CNTF to 0                */

        }
    }
    else{
        TCORB += 0x10;                          /* Increment High Width           */
        if ( TCORB == 0xF0 ){                   /* High Width = H'F0 ?            */
            CNTF = 1;                           /* Set CNTF at 1                  */

        }
    }
}
```

Link Address Setting:

Section Name	Address
CV1	H'0000
CV2	H'002C
P	H'0100
B	H'FB80