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H8SX Family

Using the Average Transfer Rate Generator in Transmission and Reception via the SCI (Serial Communications Interface): Interrupt Volume

Introduction

In the H8SX/1653, an average transfer rate generator can be selected as the clock source for serial communications interfaces 5 and 6 (SCI_5 and 6) in the asynchronous mode. In this sample task, the average transfer rate generator is used to drive the transfer of data at a rate of 921.569 kbps for the simultaneous transmission and reception of 128-byte blocks of data.

Target Device

H8SX/1653

Contents

1. Specifications

An average transfer rate generator can be selected as the clock source in the asynchronous mode on SCI_5 and 6 of the H8SX/1653. In this sample task, data are transferred at a rate of 921.569 kbps by using the average transfer rate generator of SCI_5 with the peripheral clock (Pϕ) running at 16 MHz, enabling the simultaneous transmission and reception of 128-byte blocks of data.

- Connect the H8SX/1653 as shown in figure 1.
- Table 1 shows the communications format.
- After a power-on reset of the master side, pin P13 on the same side outputs a low-level trigger, and the master side starts operations for the simultaneous reception and transmission of 128-byte blocks of data.
- When the low-level trigger is input to the $\overline{\text{IRQ3}}$ pin on the slave side, the slave side starts operations for the simultaneous transmission and reception of 128-byte blocks of data.
- In this sample task, simultaneous transmission and reception of the 128-byte blocks is handled by interrupt-exception processing.

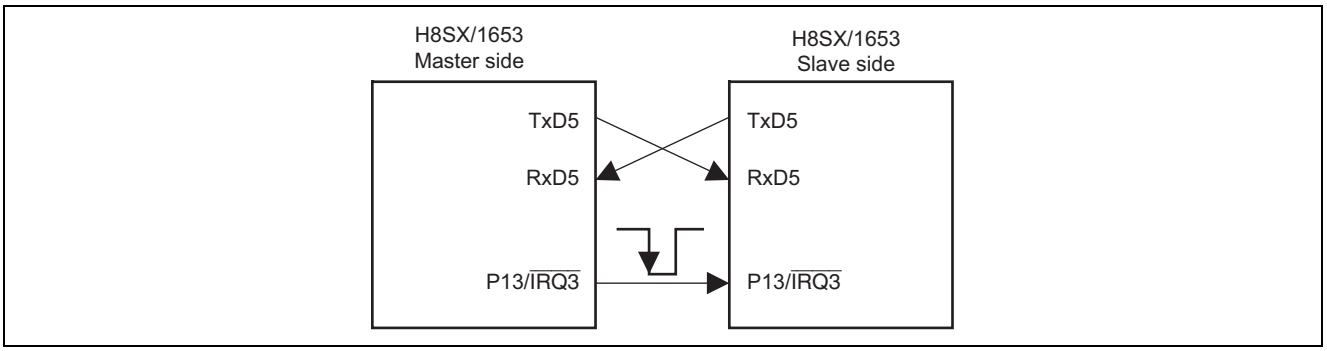


Figure 1 Setup for Asynchronous Communications with Timing from the Average Transfer Rate Generator

Table 1 Communications Format

Item	Setting
Pϕ	16 MHz
Serial communications mode	Asynchronous
Clock source	Average transfer rate generator
Transfer rate	921.569 kbps
Data length	8 bits
Parity bit	None
Stop bit	1 bit
Format for serial/parallel conversion	LSB first

2. Applicable Conditions

Table 2 Applicable Conditions

Item	Description	
Operating frequency	Input clock:	16 MHz
	System clock (Iϕ):	16 MHz
	Peripheral module clock (Pϕ):	16 MHz
	External bus clock (Bϕ):	16 MHz
Operating mode	Mode 6 (MD2 = 1, MD1 = 1, MD0 = 0) MD_CLK = 0	
Development tool	High-performance Embedded Workshop Ver. 4.00.02	
C/C++ compiler	Renesas Technology Corp. H8S, H8/300 Series C/C++ Compiler Ver. 6.01.00	
Compiler options	-cpu = h8sxa:24:md, -code = machinecode, -optimize = 1, -regparam = 3, -speed = (register, shift, struct, expression)	

Table 3 Section Settings

Address	Section Name	Description
H'001000	P	Program area
	C	Data table storage
H'FF2000	B	Non-initialized data area (RAM area)

3. Description of Modules Used

3.1 SCI_5

In this sample task, SCI_5 is used for asynchronous serial data transmission. Figure 2 is a block diagram of SCI_5. The following is a description of the functions in the diagram.

- On-Chip Peripheral Clock Pϕ
  This is the base clock for the operation of on-chip peripheral functions and is generated by a clock oscillator.
- Receive Shift Register (RSR_5)
  This register is used to receive serial data. Serial data on RSR_5 are input via the RxD5 pin. When one frame of data has been received, the data bits are automatically transferred to the Receive Data Register (RDR_5). RSR_5 is not accessible by the CPU.
- Receive Data Register (RDR_5)
  Received data are stored in this 8-bit register. After RSR_5 has received one frame, the data bits are automatically transferred from RSR_5 to RDR_5. Since RSR_5 and RDR_5 function as a double buffer, continuous reception is possible. RDR_5 is for reception only, and so is seen as a read-only register by the CPU.
- Transmit Shift Register (TSR_5)
  This register is used to transmit serial data. In transmission, data are transferred from the Transmit Data Register (TDR_5) to TSR_5, and then output on the TxD5 pin. TSR_5 is not directly accessible from the CPU.
- Transmit Data Register (TDR_5)
  Data for transmission are stored in this 8-bit register. When SCI_5 detects that TSR_5 is empty, data that have been written to TDR_5 are automatically transferred to TSR_5. Since TDR_5 and TSR_5 function as a double buffer, if the next byte is written to TDR_5 before transmission of the frame including the byte currently in TSR_5 is complete, the byte can be transferred to TSR_5 immediately on completion of the transmission. This allows continual transmission. Although TDR can be read from or written to by the CPU at all times, only write data for transmission data after having confirmed setting of the TDRE bit in the Serial Status Register (SSR_5) to 1.
- Serial Mode Register (SMR_5)
  This 8-bit register is used to select the format of serial data communications and the clock source for the on-chip baud-rate generator.
- Serial Control Register (SCR_5)
  This register is used to control transmission, reception, and interrupts, and to select the clock source for transmission and reception.
- Serial Status Register (SSR_5)
  This register consists of status flags for SCI_5 and multiprocessor bits for transmission and reception. TDRE, RDRF, ORER, PER, and FER can only be cleared.
- Smart Card Mode Register (SCMR_5)
  This register is used to select the smart-card or normal interface mode for SCMR_5, and to set up the format for the smart-card mode. For this task, the setting in SCMR_5 selects the normal asynchronous or clock synchronous mode.
- Serial Extended Mode Register (SEMR_5)
  SEMR_5 and SEMR_6 are used to select the clock source for SCI_5 and SCI_6 in the asynchronous mode. The base (peripheral) clock is automatically specified when average transfer rate operation is selected. TMO output from timer units 2 and 3 can also be set as the base clock for serial transfer. Otherwise, specific average transfer rates are selectable according to whether the peripheral-clock frequency is 8, 10.667, 12, 16, 24, or 32 MHz. Table 4 shows the relationship between Pϕ and average transfer rate.

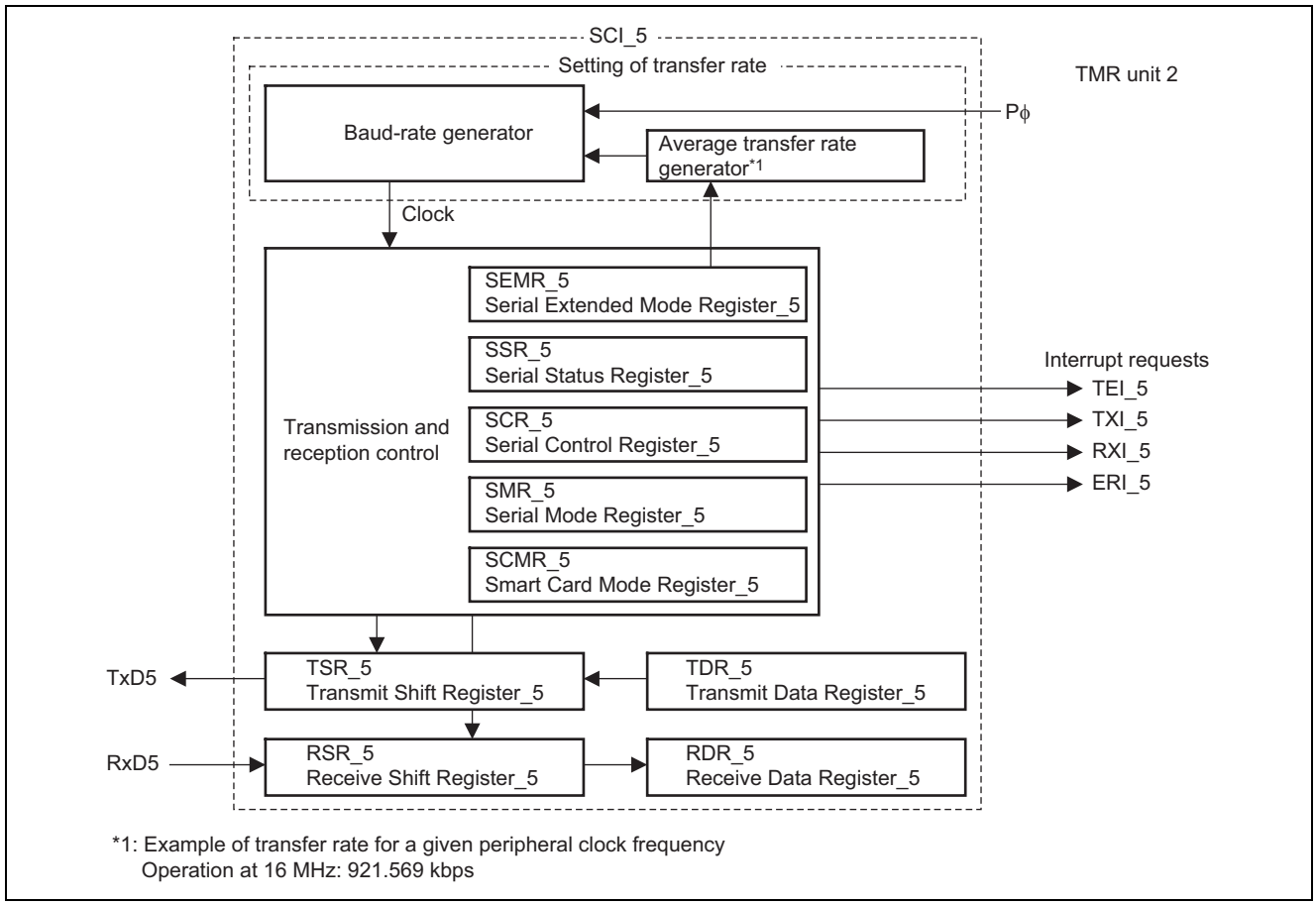


Figure 2 SCI_5 Block Diagram

Table 4 Transfer Rates of Average Transfer Rate Generators on SCI_5 and 6

Pϕ (MHz)	Average Transfer Rate (kbps)
8	460.784
10.667	115.152 460.606
12	230.263 460.526
16	115.196 460.784 720 921.569
24	115.132 460.526 720 921.053
32	720

4. Description of Operation

4.1 Outline

Figure 3 shows the operation of this task in outline. When 128 bytes of data is transmitted from the master side to the slave side, the same bytes of data is returned from the slave side to the master side.

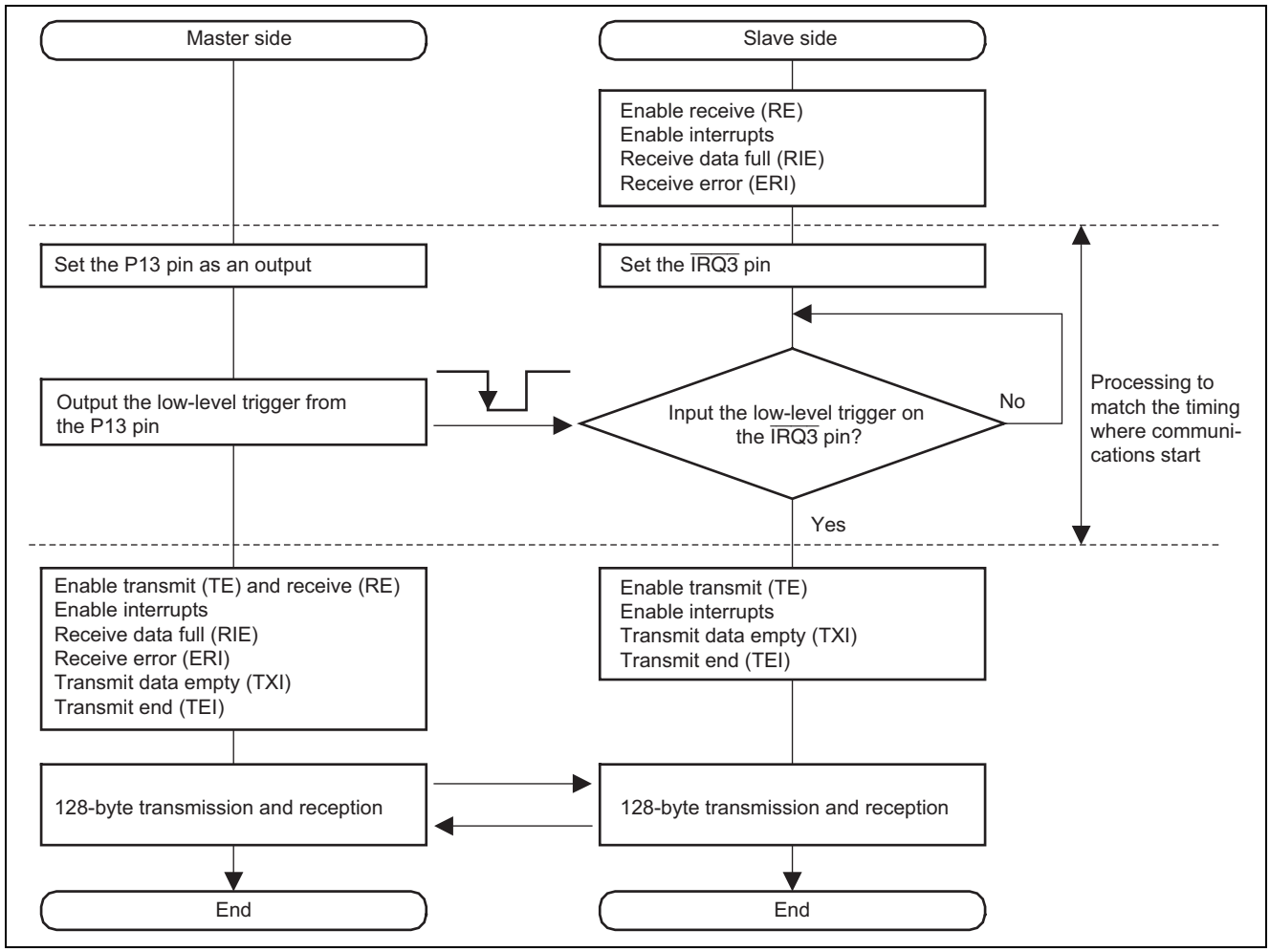


Figure 3 Outline of Operations

4.2 Transmission

The timing of transmission operations is shown in figure 4. Table 5 is a list of the hardware and software processing at the numbered points in figure 4.

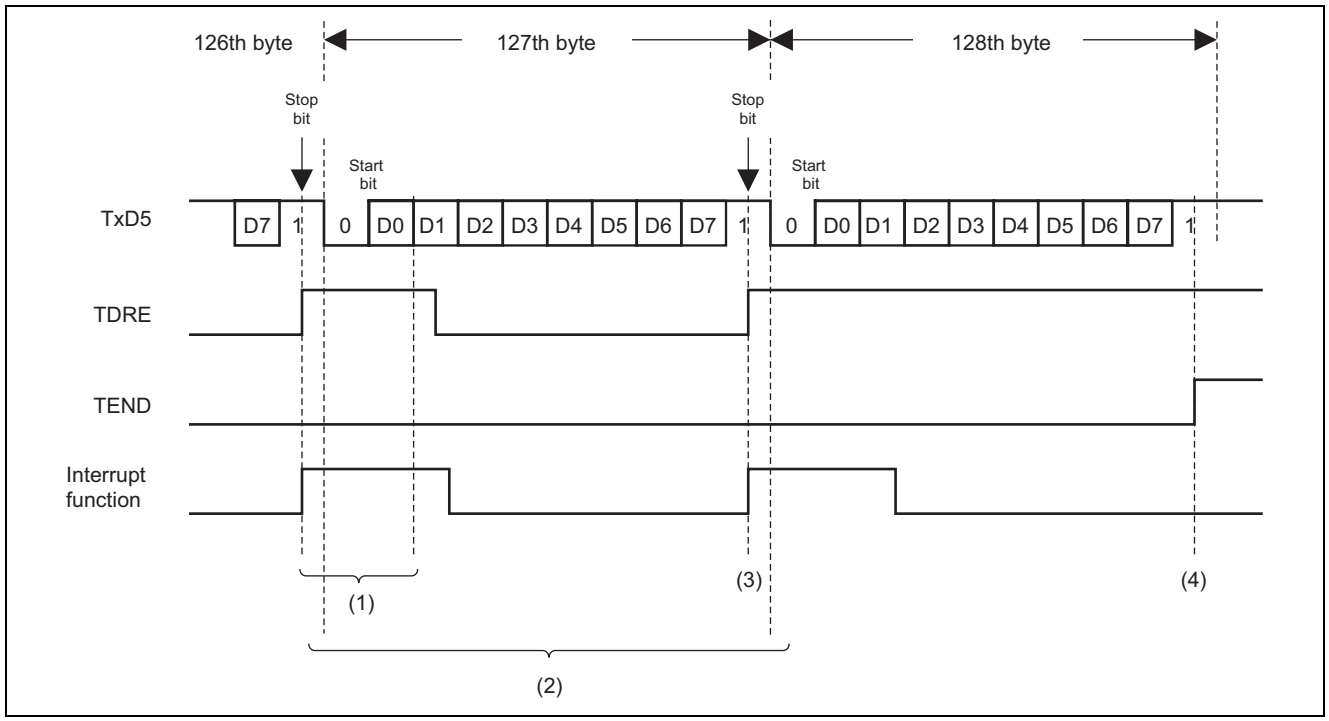


Figure 4 Timing of Transmission

Table 5 Processing

	Hardware Processing	Software Processing
(1)	a. Set TDRE to 1.	TXI interrupt processing a. Write data for transmission to TDR_5. b. Clear TDRE to 0.
(2)	a. Transfer the contents of TDR_5 to TSR_5. b. Output the contents of TSR_5 on the TxD5 pin	No processing
(3)	a. Set TDRE to 1.	TXI interrupt processing a. Write data for transmission to TDR_5. b. Clear TDRE to 0. c. Disable TXI interrupts.
(4)	a. Set TDRE to 1. b. Set TEND to 1.	TEI interrupt processing a. Clear TEND to 0. b. Clear TE to 0. c. Disable TEI interrupts.

4.3 Reception

The timing of reception operations is shown in figure 5. Table 6 is a list of the hardware and software processing at the numbered points in figure 5.

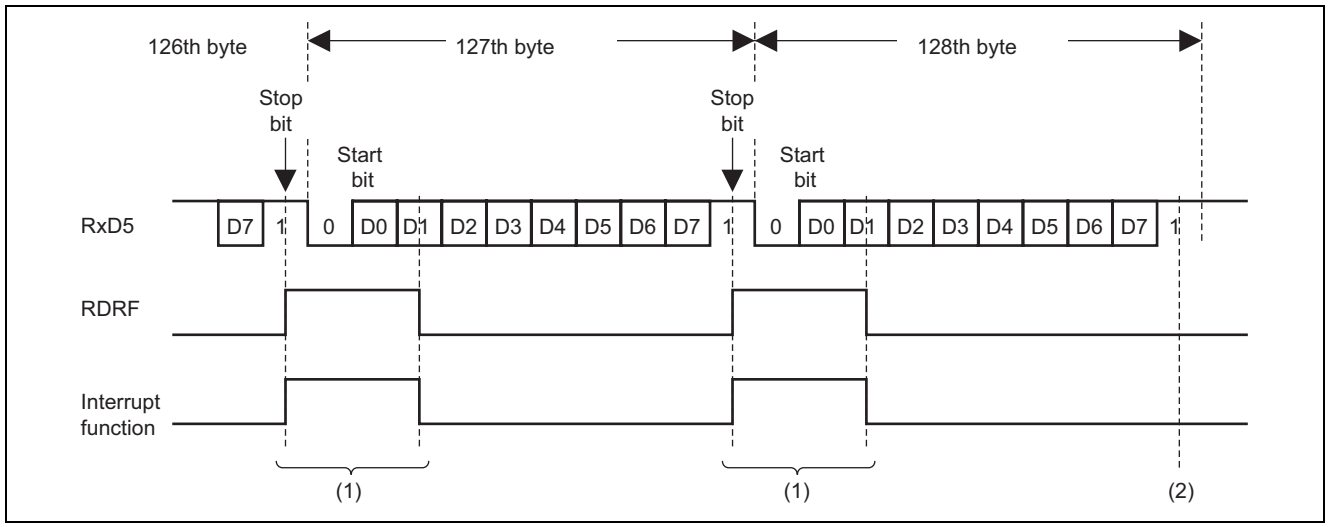


Figure 5 Timing of Reception

Table 6 Processing

	Hardware Processing	Software Processing
(1)	a. Set RDRF to 1. b. Each time a byte is successfully received in RSR_5, transfer it to RDR_5.	RXI interrupt processing a. Read received data from RDR_5. b. Clear RDRF to 0.
(2)	a. Set RDRF to 1. b. Each time a byte is successfully received in RSR_5, transfer it to RDR_5.	RXI interrupt processing a. Read received data from RDR_5. b. Clear RDRF to 0. c. Clear RE to 0. d. Disable RXI and ERI interrupts.

4.4 Example of Internal Base Clock When Pϕ = 16 MHz and ACS3 to 0 = B'0011

Figure 6 shows an example of the internal base clock when Pϕ = 16 MHz and ACS3 to 0 = B'0011 = 16 MHz and ACS3 to 0 = B'0011 = 16 MHz and ACS3 to ACS0 = B'0011. When Pϕ =16 MHz and ACS3 to 0 = B'0011, Pϕ is divided by two and the cycle retention rate is 47/51. The following is the average transfer rate calculated from Pϕ and the cycle retention rate.

$$\text{Average transfer rate} = \frac{\text{Base clock frequency for average-rate transfer}}{8} = \frac{\frac{P\phi}{2} \times \frac{47}{51}}{8} = \frac{7.3725\ \text{MHz}}{8} = 921.569\ \text{kbps}$$

4.5 One-Bit Period for Communications Data

The one-bit period corresponds to eight cycles of the internally generated base clock, but the actual period will differ according to whether or not a cycle of the frequency-divided peripheral clock has been omitted from the internal base clock. Therefore, the 1-bit interval is either of the following.

$$\text{Higher period for one bit: } \frac{1}{P\phi/2} \times 9 \text{ frequency-divided peripheral clock cycles} = 1.125\ \mu s$$

$$\text{Lower period for one bit: } \frac{1}{P\phi/2} \times 8 \text{ frequency-divided peripheral clock cycles} = 1.0\ \mu s$$

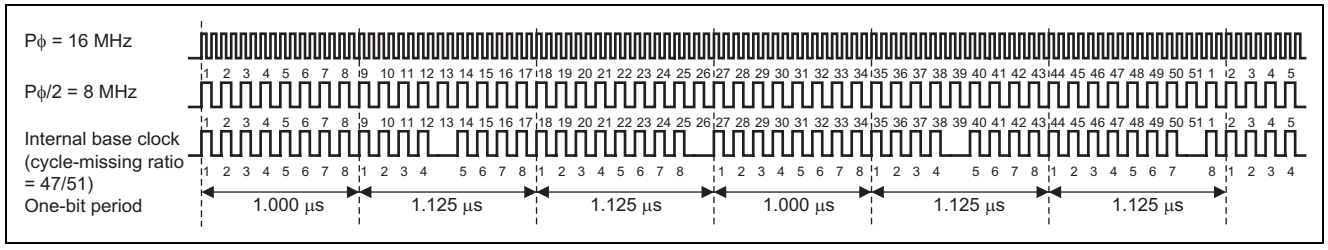


Figure 6 Example of Internal-Base-Clock Generation When Pf = 16 MHz and ACS3 to 0 = B'0011

5. Description of Software

5.1 List of Functions

Functions used in this sample task are listed in table 7.

The hierarchical structure of this sample task is shown in figure 7.

Table 7 List of Functions

Function Name	Description
Init	Initialization routine Takes the module out of module stopped mode, performs clock settings, and calls the main function
main	Main routine Makes initial SCI settings for communications at the transfer rate of 921.569 kbps when operating at Pϕ = 16 MHz.
rxi5_int	Receive Data Full Interrupt Stores the data received from RDR_5 in RAM.
txi5_int	Transmit Data Empty Interrupt Gets the data for transmission from RAM, writes the data to TDR_5, and executes transmission.
eri5_int	Receive error interrupt handler In cases of error in reception, writes the contents of SSR_5 to RAM and then initializes SSR_5
tei5_int	Transmission end interrupt handler Disables TEI interrupt requests. Sets endflg to 1.

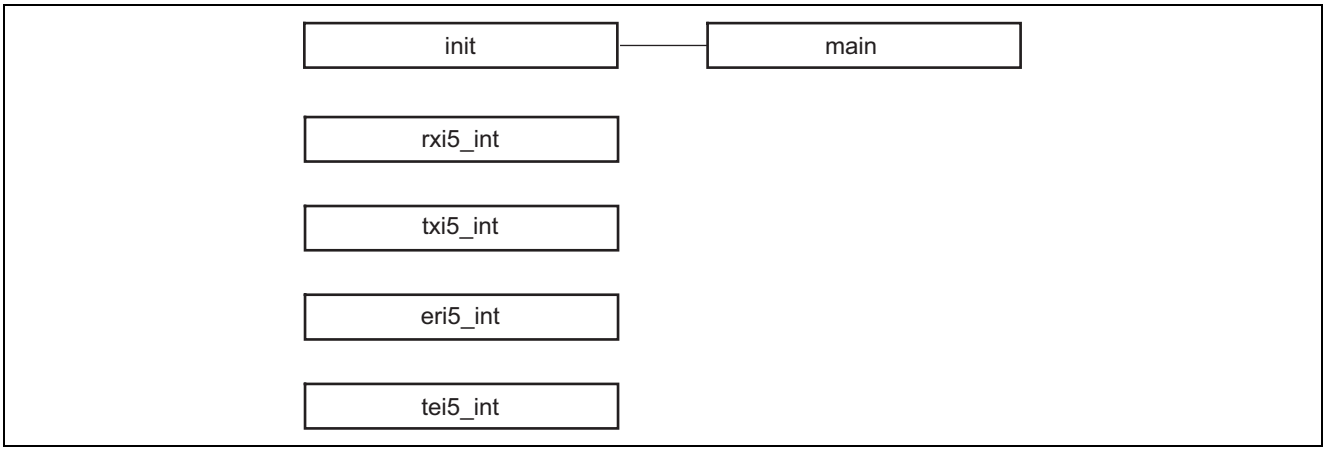


Figure 7 Hierarchical Structure

5.2 Vector Table

Table 8 Exception Handling Vector Table

Exception Handling Source	Vector Number	Vector Table Address	Vector Table Address Handling Function
Reset	0	H'000000	initinit
SCI_5 RXI5	220	H'000370	rxi5_init
SCI_5 TXI5	221	H'000374	txi5_init
SCI_5 ERI5	222	H'000378	eri5_init
SCI_5 TEI5	223	H'00037C	tei5_init

5.3 RAM Usage

Table 9 RAM Usage

Type	Variable Name	Contents	Used In
unsigned char	Endflg	Transmit end flag 0: Transmission in progress 1: Transmission has ended	main, tei5_int
unsigned char	Errbuf	Receive error buffer Stores the contents of SSR_5 when an overrun error, framing error, or parity error occurs	main, eri5_int
unsigned char	Tcnt	Transmit counter	main, txi5_int
unsigned char	Rcnt	Receive counter	main, rxi5_int
unsigned char	rvc_dt[128]	RAM area for storing received data	main, rxi5_int

5.4 Data Table

Table 10 Data Table

Type	Variable Name	Contents	Used In
unsigned char	trs_dt[128]	ROM area where data for transmission are stored. 128 bytes of data: H'00, H'01, …, H'7F	main, txi5_int

5.5 Defined Macros

Table 11 Defined Macros

Identifier	Contents	Used In
MASTER	If this is defined, compilation generates the master-side program.	Main
SLAVE	If this is defined, compilation generates the slave-side program.	Main

5.6 Description of Functions

5.6.1 init Function

1. Overview
   Initialization routine. Takes the module out of module stopped mode, sets the clock, and calls the main function.
2. Arguments
   None
3. Return value
   None
4. Description of internal register usage
   Usage of internal registers in this task is described below. The given settings are those used in the task and differ from the initial settings.

- **System Clock Control Register (SCKCR) Address: H'FFFDC4**

Bit	Bit Name	Setting	R/W	Description
10	ICK2	0	R/W	System clock (Iϕ) select
9	ICK1	1	R/W	Selects the frequency of the CPU, DMAC, DTC module and
8	ICK0	0	R/W	system clock. 010: Input clock x 1
6	PCK2	0	R/W	Peripheral module clock (Pϕ) select
5	PCK1	1	R/W	Selects the frequency of the peripheral module clock
4	PCK0	0	R/W	010: Input clock x 1
2	BCK2	0	R/W	External bus clock (Bϕ) select
1	BCK1	1	R/W	Selects the frequency of the external bus clock
0	BCK0	0	R/W	010: Input clock x 1

- Registers MSTPCRA, MSTPCRB, and MSTPCRC control module stop mode. Setting a bit to 1 makes the corresponding module enter the module stop mode, while clearing the bit to 0 takes the module out of stop mode.

- **Module Stop Control Register A (MSTPCRA) Address: H'FFFDC8**

Bit	Bit Name	Setting	R/W	Description
15	ACSE	0	R/W	All-Module-Clock-Stop Mode Enable Enables/disables all-module-clock-stop mode for reducing current drawn by stopping the bus controller and I/O port operations when the CPU executes the SLEEP instruction after the module stop mode has been set for all the on-chip peripheral modules controlled by MSTPCR. 0: All-module-clock-stop mode disabled 1: All-module-clock-stop mode enabled
13	MSTPA13	1	R/W	DMA controller (DMAC)
12	MSTPA12	1	R/W	Data transfer controller (DTC)
9	MSTPA9	1	R/W	8-bit timer (TMR_3, TMR_2)
8	MSTPA8	1	R/W	8-bit timer (TMR_1, TMR_0)
5	MSTPA5	1	R/W	D/A converter channels 1, 0
3	MSTPA3	1	R/W	A/D converter (unit 0)
0	MSTPA0	1	R/W	16-bit timer pulse unit (TPU channels 5 to 0)

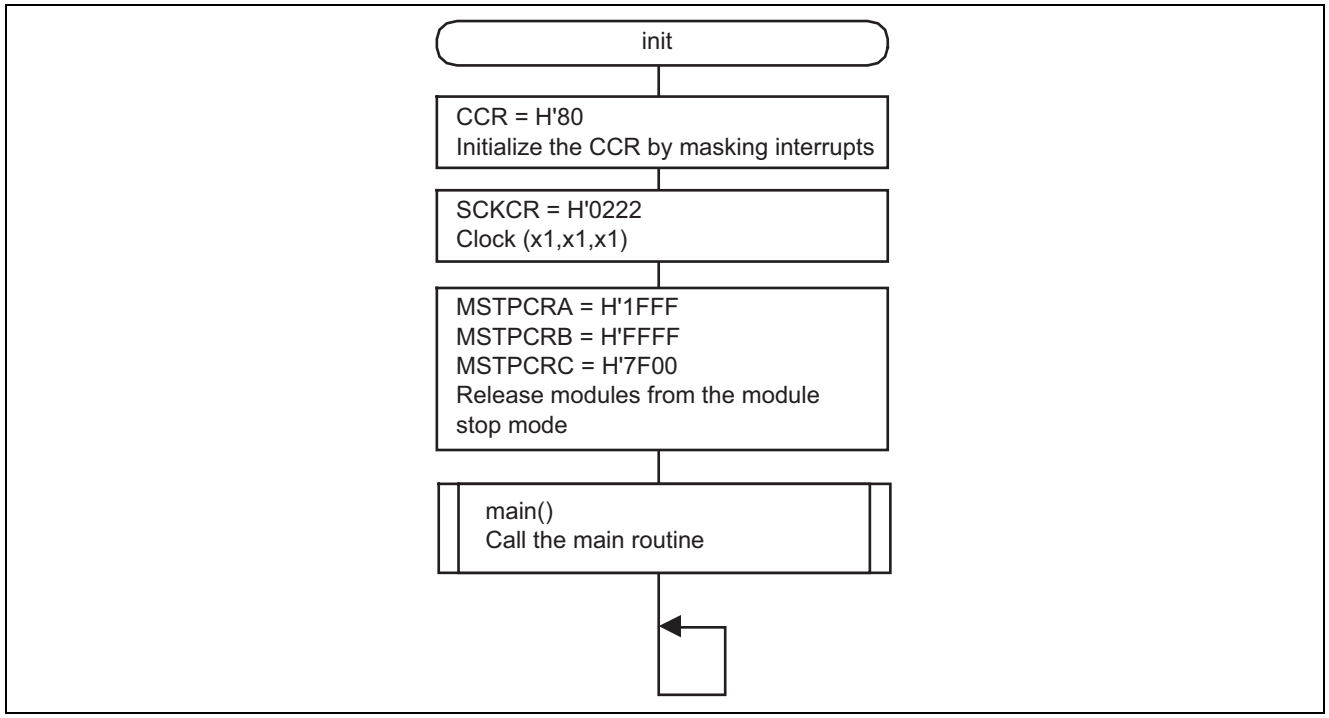
- **Module Stop Control Register B (MSTPCRB) Address: H'FFFDCA**

Bit	Bit Name	Setting	R/W	Description
15	MSTPB15	1	R/W	Programmable pulse generator (PPG)
12	MSTPB12	1	R/W	Serial Communication Interface_4 (SCI_4)
10	MSTPB10	1	R/W	Serial Communication Interface_2 (SCI_2)
9	MSTPB9	1	R/W	Serial Communication Interface_1 (SCI_1)
8	MSTPB8	1	R/W	Serial Communication Interface_0 (SCI_0)
7	MSTPB7	1	R/W	I^2C Bus Interface_1 (IIC_1)
6	MSTPB6	1	R/W	I^2C Bus Interface_0 (IIC_0)

- **Module Stop Control Register C (MSTPCRC) Address: H'FFFDCC**

Bit	Bit Name	Setting	R/W	Description
15	MSTPC15	0	R/W	Serial communications interface_5 (SCI_5) and (IrDA)
14	MSTPC14	1	R/W	Serial communications interface_6 (SCI_6)
13	MSTPC13	1	R/W	8-bit timers (TMR_4 and TMR_5)
12	MSTPC12	1	R/W	8-bit timers (TMR_6 and TMR_7)
11	MSTPC11	1	R/W	Universal Serial Bus interface (USB)
10	MSTPC10	1	R/W	Cyclic redundancy checker
4	MSTPC4	0	R/W	On-chip RAM_4 (H'FF2000 to H'FF3FFF)
3	MSTPC3	0	R/W	On-chip RAM_3 (H'FF4000 to H'FF5FFF)
2	MSTPC2	0	R/W	On-chip RAM_2 (H'FF6000 to H'FF7FFF)
1	MSTPC1	0	R/W	On-chip RAM_1 (H'FF8000 to H'FF9FFF)
0	MSTPC0	0	R/W	On-chip RAM_0 (H'FFA000 to H'FFBFFF)

5 Flowchart



5.6.2 main Function

1. Overview
   Main routine. Sets the average transfer rate in SCI, transmits and receives a total of 256 bytes of data.
2. Arguments
   None
3. Return value
   None
4. Description of internal register usage
   Usage of internal registers in this task is described below. The given settings are those used in the task and differ from the initial settings.

- **Port 1 Data Direction Register (P1DDR) Address: H'FFFB80**

Bit	Bit Name	Setting	R/W	Description
3	P13DDR	1	W	0: P13 pin is an input. 1: P13 pin is an output.

- **Port 1 Input Buffer Control Register (P1ICR) Address: H'FFFB90**

Bit	Bit Name	Setting	R/W	Description
5	P15ICR	1	R/W	0: P15 pin input buffer is disabled. Input signal is fixed to the high level. 1: P15 pin input buffer is valid. The pin state reflects the peripheral modules.
3	P13ICR	1	R/W	0: P13 pin input buffer is disabled. Input signal is fixed to the high level. 1: P13 pin input buffer is valid. The pin state reflects the peripheral modules.

- **Port Function Control Register (PFCRC) Address: H'FFFBCC**

Bit	Bit Name	Setting	R/W	Description
3	ITS3	1	R/W	$\overline{\text{IRQ3}}$ Pin Select 0: Selects $\overline{\text{IRQ3}}$-A input on pin P13 1: Selects $\overline{\text{IRQ3}}$-B input on pin P53

- **IRQ Sense Control Register L (ISCRL) Address: H'FFFD6A**

Bit	Bit Name	Setting	R/W	Description
7	IRQ3SR	0	R/W	IRQ3 Sense Control Rise
6	IRQ3SF	1	R/W	IRQ3 Sense Control Fall 01: Interrupt requests are sensed on falling edges of $\overline{\text{IRQ3}}$ input

- **Serial Mode Register_5 (SMR_5) Address: H'FFF600**

Bit	Bit Name	Setting	R/W	Description
7	C/$\overline{A}$	0	R/W	Communication Mode 0: Asynchronous mode 1: Clock synchronous mode
6	CHR	0	R/W	Character Length 0: Selects 8 bits as the data length. 1: Selects 7 bits as the data length.
5	PE	0	R/W	Parity Enable 0: No parity 1: With parity
3	STOP	0	R/W	Stop Bit Length Selects the length of the stop bit during transmission. 0: 1 stop bit 1: 2 stop bits During reception, only the first bit of the stop bits is checked, and when the second bit is 0, it is regarded as the start bit of the next transmit frame.

- **Serial Control Register_5 (SCR_5) Address: H'FFFF602**

Bit	Bit Name	Setting	R/W	Description
7	TIE	0	R/W	Transmit Interrupt Enable 0: Disables TXI interrupts 1: Enables TXI interrupts
6	RIE	0	R/W	Receive Interrupt Enable 0: Disables RXI, ERI interrupts 1: Enables RXI, ERI interrupts
5	TE	0	R/W	Transmit Enable 0: Disables transmit operation 1: Enables transmit operation
4	RE	0	R/W	Receive Enable 0: Disables receive operation 1: Enables receive operation
2	TEIE	0	R/W	Transmit End Interrupt Enable 0: TEI interrupts disabled 1: TEI interrupts enabled
1	CKE1	1	R/W	Clock Enable 1, 0
0	CKE0	X	R/W	Select the clock source. 00: Internal baud rate generator 1X: TMR clock input or average transfer rate generator

Legend
X: Don't care.

- **Serial Status Register_5 (SSR_5) Address: H'FFF604**

Bit	Bit Name	Setting	R/W	Description
7	TDRE	Undefined	R/(W)*	Transmit Data Register Empty Indicates whether TDR contains data for transmission [Setting conditions] • Clearing of the TE bit in SCR (to 0) • Transfer of data from TDR to TSR [Clearing conditions] • Writing a 0 to TDRE after having read TDRE = 1 • Generation of a TXI interrupt request allowing DMAC to write data to TDR
6	RDRF	0	R/(W)*	Receive Data Register Full Indicates whether RDR holds received data [Setting condition] • The normal end of serial reception and the transfer of received data from RSR to RDR [Clearing conditions] • Writing of 0 to RDRF after having read RDRF = 1 • Generation of an RXI interrupt request allowing DMAC or DTC to read data from RDR The RDRF flag is not affected and retains its previous value when the RE bit in SCR is cleared to 0. Note that when the next serial reception is completed while the RDRF flag is being set to 1, an overrun error occurs and the received data are lost.
5	ORER	0	R/(W)*	Overrun Error [Setting condition] • Occurrence of an overrun error during reception [Clearing condition] • Writing of 0 to ORER after having read ORER = 1
4	FER	0	R/(W)*	Framing Error [Setting condition] • Occurrence of a framing error during reception. [Clearing condition] • Writing of 0 to FER after having read FER = 1.
3	PER	0	R/(W)*	Parity Error [Setting condition] • Occurrence of a parity error during reception. [Clearing condition] • Writing of 0 to PER after having read PER = 1.
2	TEND	Undefined	R	Transmit End • Clearing of the TE bit in SCR to 0 • TDRE = 1 on transmission of the last bit of a character [Clearing conditions] • Writing of 0 to TDRE after having read TDRE = 1 • Generation of a TXI interrupt request allowing DMAC to write data to TDR

Note: * Only 0 can be written here, to clear the flag.

- **Smart Card Mode Register_3 (SCMR_3) Address: H'FFF606**

Bit	Bit Name	Setting	R/W	Description
0	SMIF	0	R/W	Smart Card Interface Mode Selection 0: Operation is in the normal asynchronous or clock synchronous mode 1: Operation is in the smart card interface mode

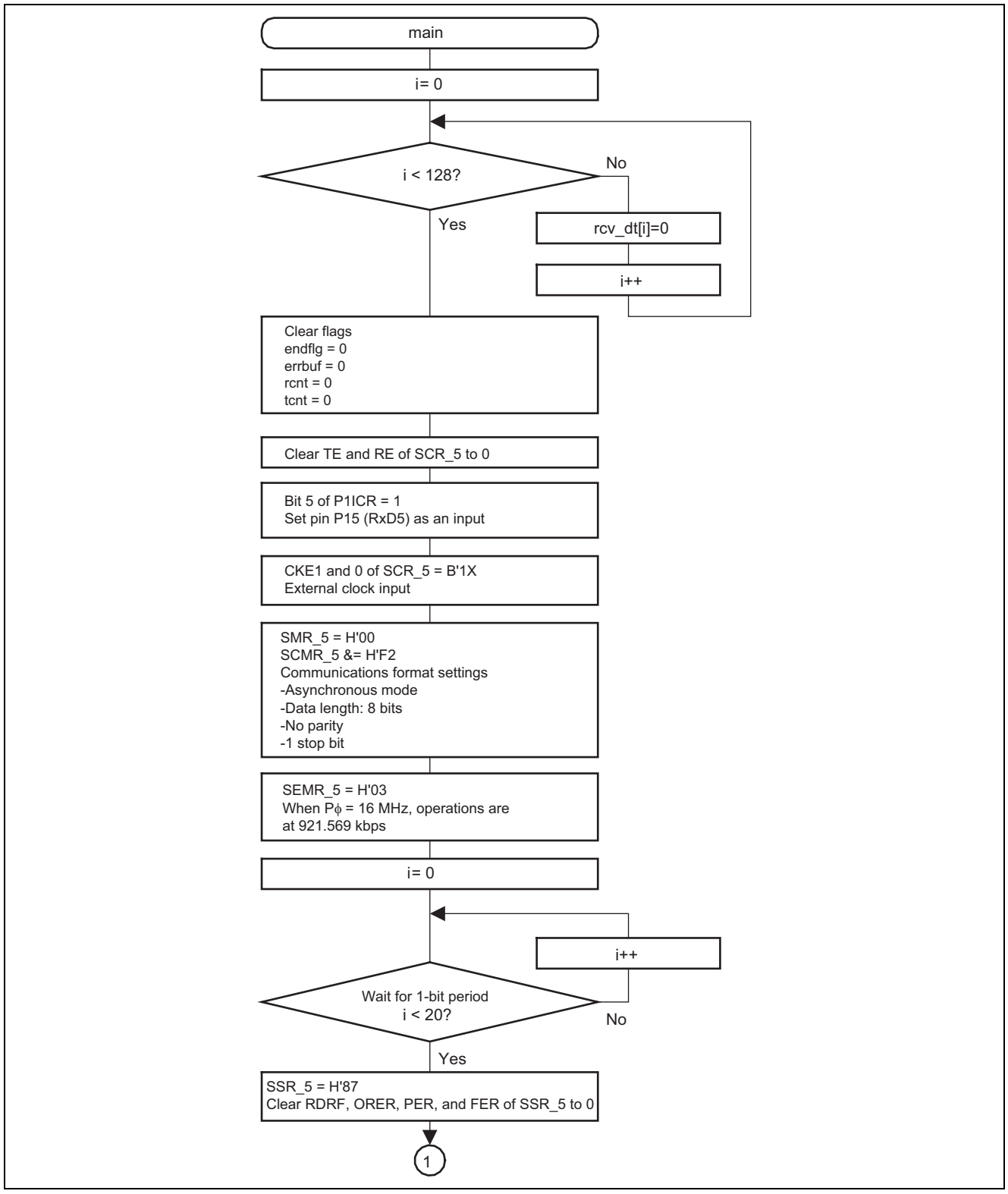
- **Serial Expansion Mode Register_3 (SEMR_3) Address: H'FFF608**

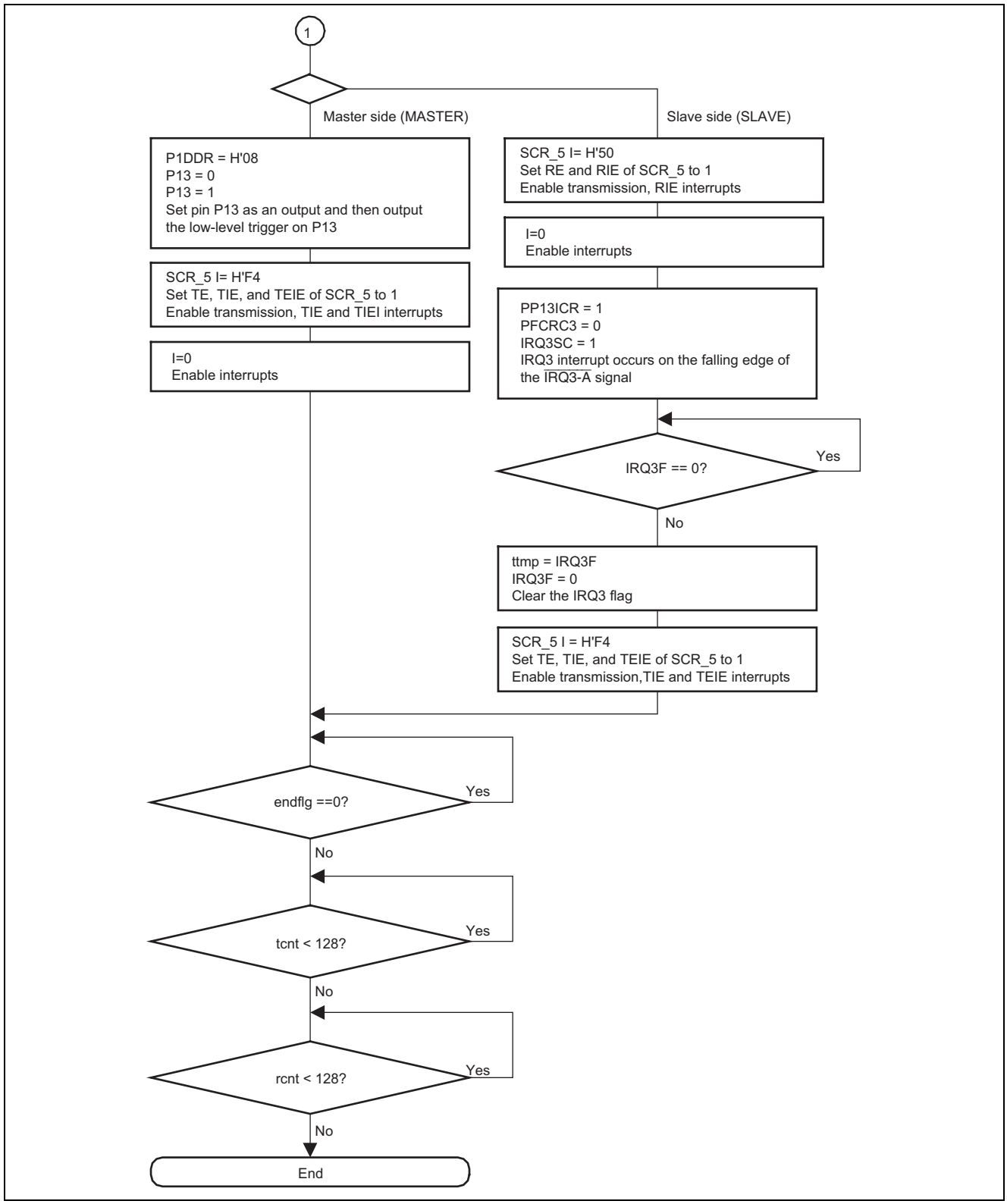
Bit	Bit Name	Setting	R/W	Description
4	ABCS	0	R/W	Asynchronous Mode Basic Clock Select (valid only in the asynchronous mode) Selects the base clock for generating 1-bit periods (the transfer rate). 0: The transfer rate is 1/16 of the frequency of the base clock. 1: The transfer rate is 1/8 of the frequency for average-rate transfer.
3	ACS3	0	R/W	Asynchronous Clock Source Select Selects the clock source in the asynchronous mode. See table 12. 0011: Selects the average transfer rate of 921.569 kbps specifically for Pϕ = 16 MHz. Note 1: When the average transfer rate is selected, the base clock is automatically set regardless of the ABCS bit in the SEMR_5 register (asynchronous base clock selection). Note 2: The setting has the desired effect only when bits ACS3 to ACS0 are in the asynchronous mode (C/$\overline{A}$ bit of SMR register is 0), and the external clock input is selected (CKE1 bit of SCR register is 1).
2	ACS2	0	R/W	
1	ACS1	1	R/W	
0	ACS0	1	R/W	

Table 12 Selection of the Asynchronous Clock Source

ACS3 to 0	Transfer Rate	Pϕ (MHz)	Functions
0000	(Set by the ABCS bit)	-	The average rate transfer generator is not used.
0001	1/16th of the base clock frequency for average-rate transfer	10.667	Average transfer rate 115.152 kbps
0010	1/8th of the base clock frequency for average-rate transfer	10.667	Average transfer rate 460.606 kbps
0011	1/8th of the base clock frequency for average-rate transfer	16	Average transfer rate 921.569 kbps
		8	Average transfer rate 460.784 kbps
0100	(Set by the ABCS bits)	-	Selects TMR-clock input: compare-match output of TMR provides the base clock for transfer
0101	1/16th of the base clock frequency for average-rate transfer	16	Average transfer rate 115.196 kbps
0110	1/16th of the base clock frequency for average-rate transfer	16	Average transfer rate 460.784 kbps
0111	1/8th of the base clock frequency for average-rate transfer	24	Average transfer rate 720 kbps
1000	1/16th of the base clock frequency for average-rate transfer	24	Average transfer rate 115.132 kbps
1001	1/16th of the base clock frequency for average-rate transfer	24	Average transfer rate 460.526 kbps
		12	Average transfer rate 230.263 kbps
1010	1/8th of the base clock frequency for average-rate transfer	24	Average transfer rate 720 kbps
1011	1/8th of the base clock frequency for average-rate transfer	24	Average transfer rate 921.053 kbps
		12	Average transfer rate 460.526 kbps
1100	1/16th of the base clock frequency for average-rate transfer	32	Average transfer rate 720 kbps

5. Flowchart


main
i= 0
i < 128?
No
Yes
rcv_dt[i]=0
i++
Clear flags
endflg = 0
errbuf = 0
rcnt = 0
tcnt = 0
Clear TE and RE of SCR_5 to 0
Bit 5 of P1ICR = 1
Set pin P15 (RxD5) as an input
CKE1 and 0 of SCR_5 = B'1X
External clock input
SMR_5 = H'00
SCMR_5 &= H'F2
Communications format settings
-Asynchronous mode
-Data length: 8 bits
-No parity
-1 stop bit
SEMR_5 = H'03
When Pϕ = 16 MHz, operations are
at 921.569 kbps
i= 0
i++
Wait for 1-bit period
i < 20?
No
Yes
SSR_5 = H'87
Clear RDRF, ORER, PER, and FER of SSR_5 to 0
1


1
Master side (MASTER)
Slave side (SLAVE)
P1DDR = H'08
P13 = 0
P13 = 1
Set pin P13 as an output and then output the low-level trigger on P13
SCR_5 I= H'F4
Set TE, TIE, and TEIE of SCR_5 to 1
Enable transmission, TIE and TIEI interrupts
I=0
Enable interrupts
SCR_5 I= H'50
Set RE and RIE of SCR_5 to 1
Enable transmission, RIE interrupts
I=0
Enable interrupts
PP13ICR = 1
PFCRC3 = 0
IRQ3SC = 1
IRQ3 interrupt occurs on the falling edge of the IRQ3-A signal
IRQ3F == 0?
Yes
No
ttmp = IRQ3F
IRQ3F = 0
Clear the IRQ3 flag
SCR_5 I = H'F4
Set TE, TIE, and TEIE of SCR_5 to 1
Enable transmission,TIE and TEIE interrupts
endflg ==0?
Yes
No
tcnt < 128?
Yes
No
rcnt < 128?
Yes
No
End

5.6.3 rxi5_int Function

1. Overview
   Handler for the receive data full interrupt. Receives one byte.
2. Arguments
   None
3. Return value
   None
4. Description of internal register usage
   Usage of internal registers in this task is described below. The given settings are those used in the task and differ from the initial settings.

- **Serial Control Register_5 (SCR_5) Address: H'FFF602**

Bit	Bit Name	Setting	R/W	Description
6	RIE	0	R/W	Receive Interrupt Enable 0: Disables RXI, ERI interrupts 1: Enables RXI, ERI interrupts
4	RE	0	R/W	Receive Enable 0: Disables reception 1: Enable reception

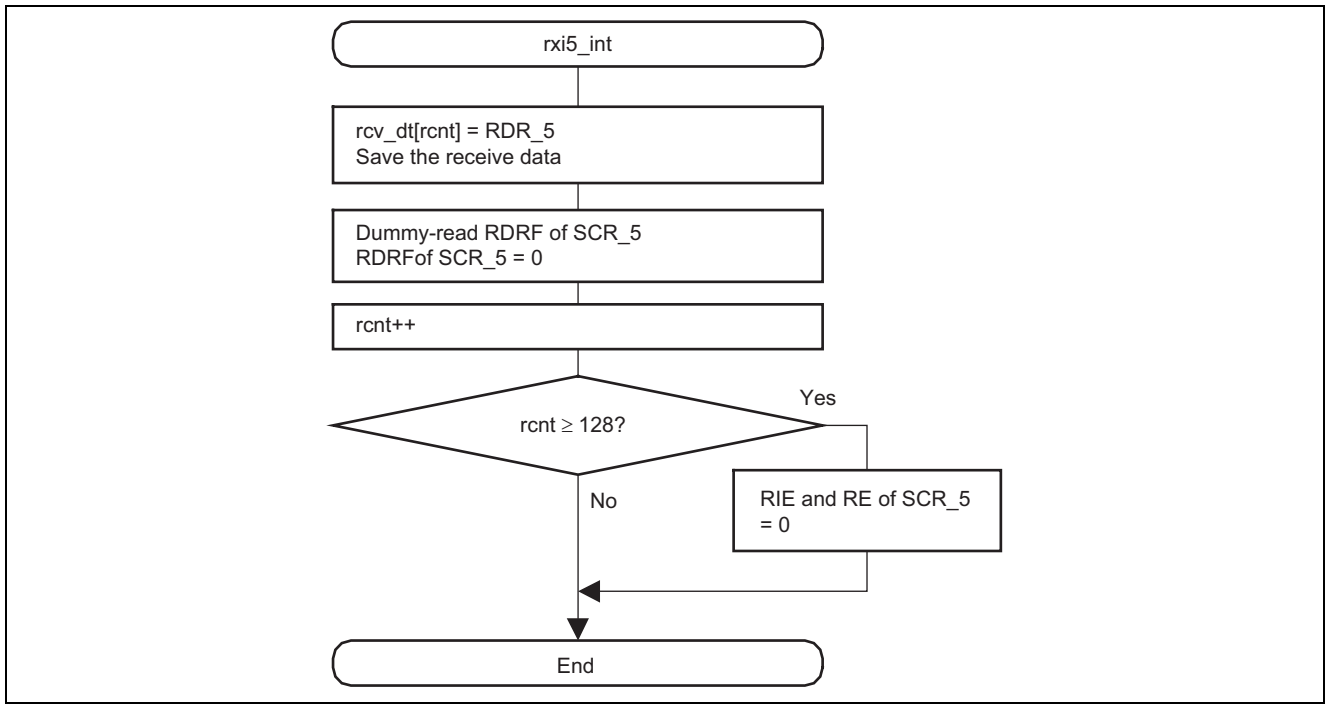
- **Serial Status Register_5 (SSR_5) Address: H'FFF604**

Bit	Bit Name	Setting	R/W	Description
6	RDRF	Undefined	R/(W)*	Receive Data Register Full Indicates whether RDR holds received data [Setting condition] • The normal end of serial reception and the transfer of received data from RSR to RDR [Clearing conditions] • Writing of 0 to RDRF after having read RDRF = 1 • Generation of an RXI interrupt request allowing DMAC or DTC to read data from RDR The RDRF flag is not affected and retains its previous value when the RE bit in SCR is cleared to 0. Note that when the next serial reception is completed while the RDRF flag is being set to 1, an overrun error occurs and the received data are lost.

Note: * Only 0 can be written here, to clear the flag.

- **Receive Data Register_5 (RDR_5) Address: H'FFF605**
  Function: A read-only 8-bit register for storing received data.
  Setting: Undefined.

5. Flowchart


rxi5_int
rcv_dt[rcnt] = RDR_5
Save the receive data
Dummy-read RDRF of SCR_5
RDRFof SCR_5 = 0
rcnt++
rcnt ≥ 128?
Yes
No
RIE and RE of SCR_5
= 0
End

5.6.4 txi5_int Function

1. Overview
   Handler for the transmit data empty interrupt. Transfers one byte for transmission.
2. Arguments
   None
3. Return value
   None
4. Description of internal register usage
   Usage of internal registers in this task is described below. The given settings are those used in the task and differ from the initial settings.

- **Serial Control Register_5 (SCR_5) Address: H'FFF602**

Bit	Bit Name	Setting	R/W	Description
7	TIE	0	R/W	Transmit Interrupt Enable 0: Disables TXI interrupt requests 1: Enables TXI interrupt requests

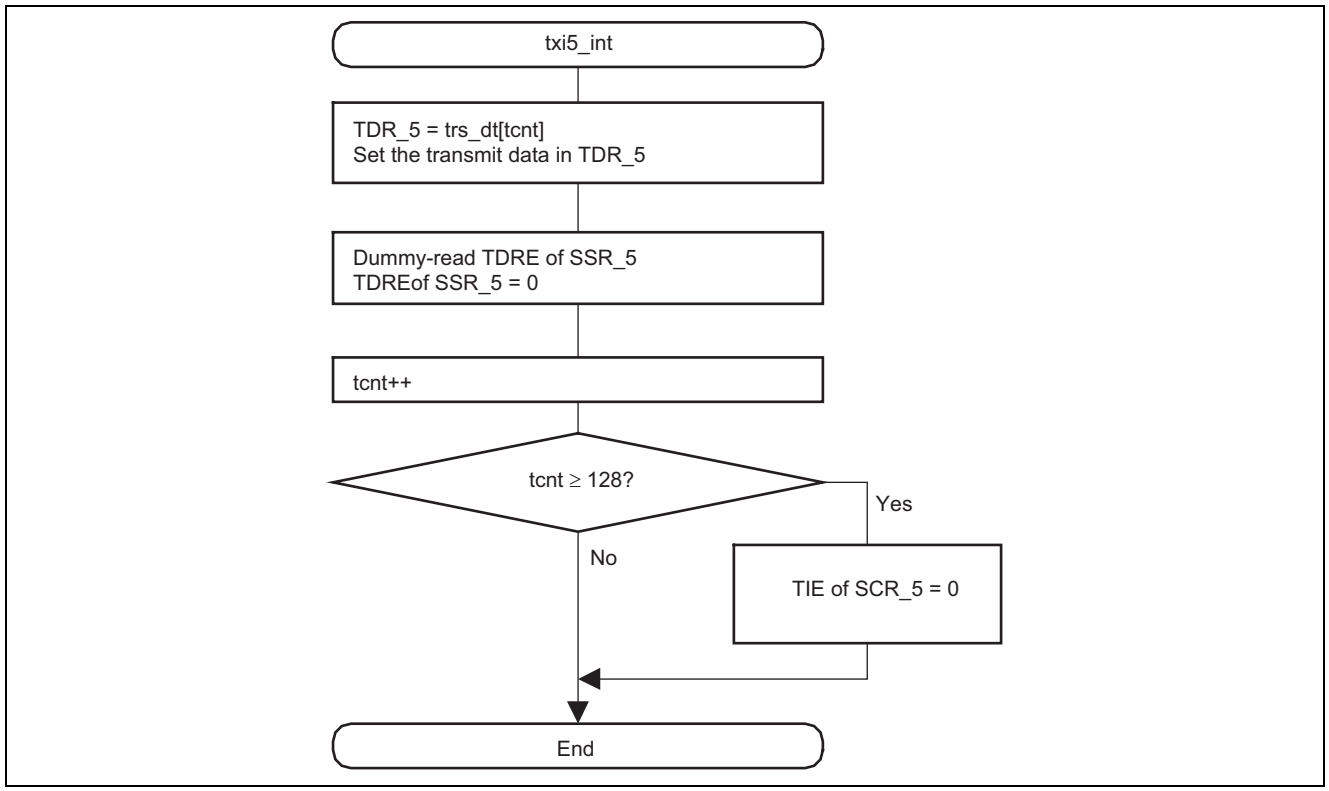
- **Transmit Data Register_5 (TDR_5) Address: H'FFF603**
  Function: A readable/writable 8-bit register that holds data for transmission.
  Setting: trs[tcnt]

- **Serial Status Register_5 (SSR_5) Address: H'FFF604**

Bit	Bit Name	Setting	R/W	Description
7	TDRE	0	R/(W)*	Transmit Data Register Empty Indicates whether TDR contains data for transmission [Setting conditions] • Clearing of the TE bit in SCR (to 0) • Transfer of data from TDR to TSR [Clearing conditions] • Writing a 0 to TDRE after having read TDRE = 1 • Generation of a TXI interrupt request allowing DMAC to write data to TDR

Note: * Only 0 can be written here, to clear the flag.

5. Flowchart


txi5_int
TDR_5 = trs_dt[tcnt]
Set the transmit data in TDR_5
Dummy-read TDRE of SSR_5
TDREof SSR_5 = 0
tcnt++
tcnt ≥ 128?
Yes
No
TIE of SCR_5 = 0
End

5.6.5 eri5_int Function

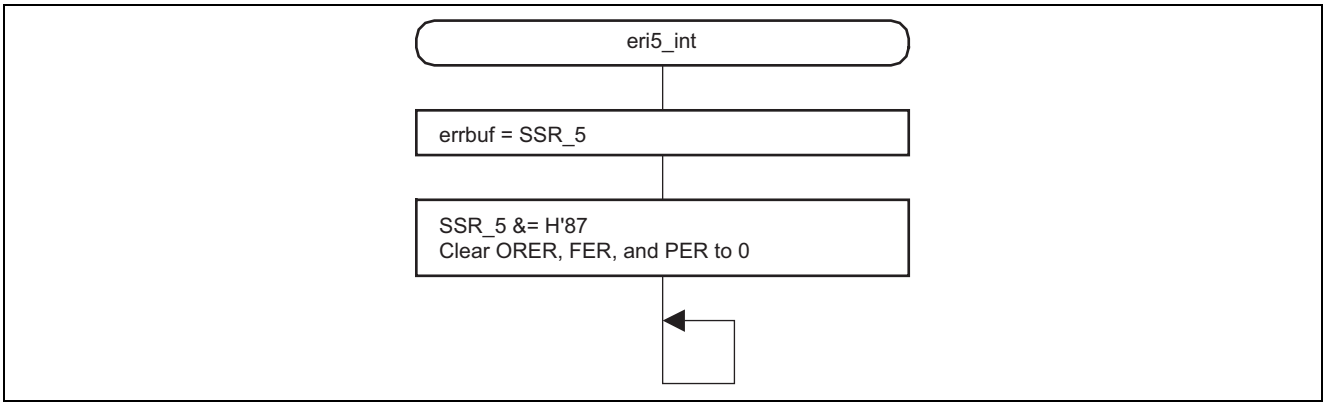
1. Overview
   Handler for the receive error interrupts. Transfers one byte to memory.
2. Arguments
   None
3. Return value
   None
4. Description of internal register usage
   Usage of internal registers in this task is described below. The given settings are those used in the task and differ from the initial settings.

- **Serial Status Register_5 (SSR_5) Address: H'FFF604**

Bit	Bit Name	Setting	R/W	Description
5	ORER	0	R/(W)*	Overrun Error [Setting condition] • Occurrence of an overrun error during reception [Clearing condition] • Writing of 0 to ORER after having read ORER = 1
4	FER	0	R/(W)*	Framing Error [Setting condition] • Occurrence of a framing error during reception [Clearing condition] • Writing of 0 to FER after having read FER = 1
3	PER	0	R/(W)*	Parity Error [Setting condition] • Occurrence of a parity error during reception [Clearing condition] • Writing of 0 to ORER after having read ORER = 1

Note: * Only 0 can be written here, to clear the flag.

5. Flowchart



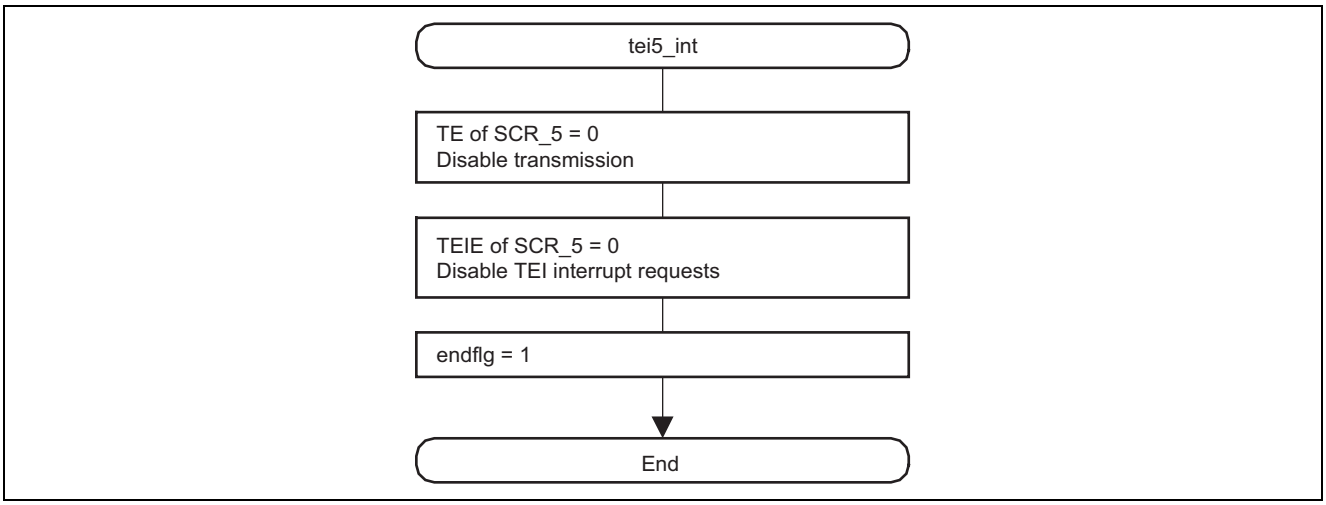
5.6.6 tei5_int Function

1. Overview
   Handler for the transmit end interrupt function. Transfers one byte to memory as a flag.
2. Arguments
   None
3. Return value
   None
4. Description of internal register usage
   Usage of internal registers in this task is described below. The given settings are those used in the task and differ from the initial settings.

- **Serial Control Register_5 (SCR_5) Address: H'FFF602**

Bit	Bit Name	Setting	R/W	Description
5	TE	0	R/W	Transmit Enable 0: Disables transmission 1: Enables transmission
2	TEIE	0	R/W	Transmit End Interrupt Enable 0: Disables TEI interrupt requests 1: Enables TEI interrupt requests

5. Flowchart



Revision Record

Rev.	Date	Description	
		Page	Summary
1.00	Mar.10.06	—	First edition issued

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