

## Renesas RA Family

# Usage of Schmitt Trigger Input Pins on RA4M3

## Introduction

This document answers common questions and points out subtleties in the usage of the Schmitt Trigger Input Pins on the RA4M3 that might be missed unless the hardware manual was extensively reviewed. This document is not intended to be a replacement for the hardware manual. It is intended to supplement the manual by highlighting some key items that most engineers will need to start their own design. It also discusses some design decisions from an application point of view.

## Target Device

RA4M3

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## 1. Usage of Schmitt Trigger Input Pins

GPIO used as normal Input has no Schmitt Trigger as described in the hardware manual. However, it can be used as Input Pins with a Schmitt Trigger with the following restriction. Kindly ensure that you thoroughly evaluate your own environment before use.

**Bit 16, PMR = 1 must be set in the Port mn Pin Function Select Register.**

The following Input Pins have Schmitt Trigger Input capability. This Schmitt Trigger Input capability is usable by the following considerations:

1. The peripheral functions must be selected (PMR = 1) for the individual Input Pins where a Schmitt trigger input is required, but the corresponding peripheral functions cannot be used once Schmitt Trigger Input function is selected, and the pin should be read as a general purpose I/O pin.
2. With PMR = 1 current consumption may increase compared to using PMR = 0.

### 1.1 Settings for pin function control

Table 19.5b Register settings for input/output pin function (PORT0)

PSEL[4:0] settings	Function	pin											
		P000	P001	P002	P003	P004	P005	P006	P007	P008	P009	P014	P015
00000b	(Initial)	-	-	-	-	-	-	-	-	-	-	-	-
ASEL bit	Analog	-	-	-	-	-	-	-	-	-	-	-	-
ISEL bit	Interrupt	✓	✓	✓	-	✓	-	-	-	✓	✓	-	✓

✓ : Available

- : Setting prohibited

Table 19.6b Register settings for input/output pin function (PORT1)

PSEL[4:0] settings	Function	pin															
		P100	P101	P102	P103	P104	P105	P106	P107	P108	P109	P110	P111	P112	P113	P114	P115
00000b	(Initial)	-															
00001b	AGT	✓	-	✓	✓	✓	✓	✓	✓	-	✓	-	✓	✓	✓	✓	-
00010b	GPT	✓	-	✓	✓	✓	✓	-	-	-	✓	-	-	-	-	-	-
00011b	GPT	✓	-	✓	✓	✓	✓	-	-	-	✓	-	✓	✓	✓	✓	-
00100b	SCI	✓	-	✓	-	-	-	-	-	-	-	-	✓	✓	✓	-	-
00101b	SCI	✓	-	-	-	-	-	-	-	-	✓	-	✓	✓	-	-	-
00110b	SPI	-	-	-	-	-	-	-	-	-	✓	-	✓	-	-	-	-
01001b	CLKOUT/RTC	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
01010b	CAC/ADC12	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
10000b	CAN	-	-	✓	-	-	-	-	-	-	-	-	-	-	-	-	-
10001b	QSPI	✓	-	✓	✓	✓	-	-	-	-	-	-	-	-	-	-	-
10010b	SSIE	-	-	-	-	-	-	-	-	-	-	-	-	✓	✓	✓	-
ASEL bit	Analog	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
ISEL bit	Interrupt	✓	✓	-	-	✓	✓	-	-	-	-	-	✓	-	-	-	-

✓ : Available

- : Setting prohibited

Table 19.7b Register settings for input/output pin function (PORT2)

PSEL[4:0] settings	Function	Pin															
		P200 <sup>*4</sup>	P201	P202	P203	P204	P205	P206	P207	P208	P209	P210	P211	P212	P213	P214	
00000b	(Initial)	-															
00001b	AGT	-	-	✓	✓	✓	✓	-	-	-	✓	✓	✓	-	-	✓	
00010b	GPT	-	-	-	-	✓	✓	✓	-	✓	✓	✓	✓	-	-	✓	
00011b	GPT	-	-	✓	✓	✓	✓	-	-	-	-	-	-	-	-	-	
00100b	SCI	-	-	✓	-	✓	✓	✓	✓	-	-	-	-	-	-	-	
00101b	SCI	-	-	✓	✓	✓	-	✓	-	-	-	-	-	-	-	-	
00110b	SPI	-	-	✓	✓	✓	-	-	-	-	-	-	-	-	-	-	
00111b	IIC	-	-	-	-	-	✓	✓	-	-	-	-	-	-	-	-	
01001b	CLKOUT/RTC	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	
01010b	CAC/ADC12	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	
01100b	CTSU	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	
10000b	CAN	-	-	✓	-	-	-	-	-	-	-	-	-	-	-	-	
10001b	QSPI	-	-	-	-	-	-	-	✓	✓	✓	✓	✓	-	-	✓	
10010b	SSIE	-	-	-	-	✓	✓	✓	-	-	-	-	-	-	-	-	
10011b	USBFS	-	-	-	-	✓	✓	-	-	-	-	-	-	-	-	-	
10101b	SDHI	-	-	✓	✓	✓	✓	✓	-	✓	✓	✓	✓	-	-	-	
11010b	Trace (Debug)	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	
ASEL bit	Analog	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	
ISEL bit	Interrupt	-	-	✓	✓	-	✓	✓	-	-	-	-	-	✓	✓	-	

Note 4. When using NMI pin interrupt, Port related registers setting are not required.

✓ : Available

- : Setting prohibited

Table 19.8b Register settings for input/output pin function (PORT3)

PSEL[4:0] settings	Function	Pin													
		P300	P301	P302	P303	P304	P305	P306	P307	P308	P309	P310	P311	P312	P313
00000b	(Initial)	-													
00001b	AGT	-	✓	-	-	✓	-	-	-	-	-	-	✓	✓	-
00010b	GPT	-	✓	✓	-	✓	-	-	-	-	-	-	-	-	-
00011b	GPT	-	✓	✓	✓	✓	-	-	-	-	-	-	-	-	-
00100b	SCI	-	✓	✓	-	-	-	-	-	-	-	-	-	-	-
00101b	SCI	-	-	-	-	-	-	-	-	-	-	-	✓	-	-
00110b	SPI	-	-	-	-	-	-	-	-	-	-	-	-	-	-
10001b	QSPI	-	-	-	-	-	-	-	-	-	-	-	-	-	-
10101b	SDHI	-	-	-	-	-	-	-	-	-	-	-	-	-	✓
ASEL bit	Analog	-	-	-	-	-	-	-	-	-	-	-	-	-	-
ISEL bit	Interrupt	-	✓	✓	-	✓	-	-	-	-	-	-	-	-	-

✓ : Available

- : Setting prohibited

Table 19.9b Register settings for input/output pin function (PORT4)

PSEL[4:0] settings	Function	pin															
		P400	P401	P402	P403	P404	P405	P406	P407	P408	P409	P410	P411	P412	P413	P414	P415
00000b	(Initial)	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
00001b	AGT	✓	-	-	-	-	-	✓	✓	✓	✓	✓	✓	✓	✓	✓	-
00010b	GPT	-	✓	-	-	-	-	-	-	✓	✓	✓	✓	✓	✓	-	-
00011b	GPT	✓	✓	-	✓	✓	✓	✓	✓	✓	-	-	-	-	-	✓	-
00100b	SCI	✓	-	-	-	-	-	-	-	✓	✓	✓	✓	✓	-	-	-
00101b	SCI	-	-	-	-	-	-	-	-	✓	✓	✓	-	-	-	-	-
00110b	SPI	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
00111b	IIC	-	-	-	-	-	-	-	✓	✓	-	-	-	-	-	-	-
01001b	CLKOUT/RTC	-	-	-	-	-	-	-	✓	-	-	-	-	-	-	-	-
01010b	CAC/ADC12	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
01100b	CTSU	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
10000b	CAN	-	-	✓	-	-	-	-	-	-	-	-	-	-	-	-	-
10010b	SSIE	✓	-	✓	✓	✓	✓	✓	-	-	-	-	-	-	-	-	-
10011b	USBFS	-	-	-	-	-	-	-	✓	✓	-	-	-	-	-	-	-
10101b	SDHI	-	-	-	-	-	-	-	-	-	-	✓	✓	✓	-	✓	-
Don't-care	AGT,RTC	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
ASEL bit	Analog	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
ISEL bit	Interrupt	✓	✓	✓	✓	✓	-	-	-	✓	✓	✓	✓	-	-	✓	-

✓ : Available

- : Setting prohibited

Table 19.10b Register settings for input/output pin function (PORT5)

PSEL[4:0] settings	Function	pin									
		P500	P501	P502	P503	P504	P505	P506	P507	P511	P512
00000b	(Initial)	-	-	-	-	-	-	-	-	-	-
00001b	AGT	-	-	✓	✓	✓	✓	-	-	-	-
00010b	GPT	-	-	✓	✓	✓	-	-	-	-	-
00011b	GPT	-	-	-	-	-	-	-	-	-	-
00100b	SCI	-	-	-	-	-	-	-	-	-	-
00111b	IIC	-	-	-	-	-	-	-	-	-	-
01010b	CAC/ADC12	-	-	-	-	-	-	-	-	-	-
10000b	CAN	-	-	-	-	-	-	-	-	-	-
10001b	QSPI	-	-	✓	✓	✓	✓	-	-	-	-
10011b	USBFS	-	-	✓	-	✓	-	-	-	-	-
ASEL bit	Analog	-	-	-	-	-	-	-	-	-	-
ISEL bit	Interrupt	-	-	✓	-	-	✓	✓	-	-	-

✓ : Available

- : Setting prohibited

Table 19.11b Register settings for input/output pin function (PORT6)

PSEL[4:0] settings	Function	Pin													
		P600	P601	P602	P603	P604	P605	P608	P609	P610	P611	P612	P613	P614	
00000b	(Initial)	-													
00001b	AGT	✓	-	-	✓	✓	✓	-	✓	✓	✓	-	✓	✓	
00011b	GPT	✓	-	-	✓	-	-	✓	✓	✓	-	-	-	-	
00101b	SCI	✓	-	-	-	-	-	-	-	-	-	-	-	-	
01001b	CLKOUT/RTC	-	-	-	-	-	-	-	-	-	-	-	-	-	
01010b	CAC/ADC12	-	-	-	-	-	-	-	-	-	-	-	-	-	
10000b	CAN	-	-	-	-	-	-	-	-	✓	-	-	-	-	
ASEL bit	Analog	-	-	-	-	-	-	-	-	-	-	-	-	-	
ISEL bit	Interrupt	-	-	-	-	-	-	-	-	-	-	-	-	-	

✓ : Available

- : Setting prohibited

Table 19.12b Register settings for input/output pin function (PORT7)

PSEL[4:0] settings	Function	Pin											
		P700	P701	P702	P703	P704	P705	P708	P709	P710	P711	P712	P713
00000b	(Initial)	-	-	-	-	-	-	-	-	-	-	-	-
00001b	AGT	✓	✓	✓	✓	✓	✓	-	-	-	✓	✓	✓
00011b	GPT	✓	✓	✓	✓	-	-	-	-	-	-	✓	✓
00101b	SCI	-	-	-	-	-	-	✓	✓	✓	-	-	-
00110b	SPI	✓	-	✓	-	-	-	-	-	-	-	-	-
01010b	CAC/ADC12	-	-	-	-	-	-	-	-	-	-	-	-
01100b	CTSU	-	-	-	-	-	-	-	-	-	-	-	-
10000b	CAN	-	-	-	-	-	✓	-	-	-	-	-	-
10010b	SSIE	-	-	-	-	-	-	-	-	-	-	-	-
ASEL bit	Analog	-	-	-	-	-	-	-	-	-	-	-	-
ISEL bit	Interrupt	-	-	-	-	-	-	✓	✓	-	-	-	-

✓ : Available

- : Setting prohibited

Table 19.13b Register settings for input/output pin function (PORT8)

PSEL[4:0] settings	Function	Pin	
		P800	P801
00000b	(Initial)	-	-
00001b	AGT	-	-
00101b	SCI,SCI-E	-	-
ASEL bit	Analog	-	-
ISEL bit	Interrupt	-	-

✓ : Available

- : Setting prohibited

## 1.2 Steps for setting and using Schmitt Trigger inputs

1. Make sure not to use any peripheral functionality on the desired Schmitt Trigger input pin.
2. Clear PWPR\_BOWI to enable write to PWPR\_PFSWE.
3. Set PWPR\_PFSWE to enable Pmm-PFS.
4. Set PmmPFS.PSEL[4:0] for the peripheral that you select to assign.
5. Set PmmPFS.PMR = 1 (to set peripheral mode).
6. Clear PWPR\_PFSWE to prohibit writing to PmmPFS.
7. Set PWPR\_BOW1 to prohibit writing to PWPR\_PFSWE.
8. Then, you can read the input port with Schmitt Trigger characteristics.

\*Note: With PMR = 1 current consumption may increase compared to using PMR = 0.

### Software Code Example - Setting Port P100 (AGT selected) to Schmitt Trigger Inputs

Table 19.6b Register settings for input/output pin function (PORT1)

PSEL[4:0] settings	Function	pin															
		P100	P101	P102	P103	P104	P105	P106	P107	P108	P109	P110	P111	P112	P113	P114	P115
00000b	(Initial)	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
00001b	AGT	✓	-	✓	✓	✓	✓	✓	✓	-	✓	-	✓	✓	✓	✓	-
00010b	GPT	✓	-	✓	✓	✓	✓	-	-	-	✓	-	-	-	-	-	-
00011b	GPT	✓	-	✓	✓	✓	✓	-	-	-	✓	-	✓	✓	✓	✓	-
00100b	SCI	✓	-	✓	-	-	-	-	-	-	-	-	✓	✓	✓	-	-

The code example configures P100 pin and selects the AGT, enabling the Schmitt Trigger functionality:

```
R_IOPORT_PinCfg(&g_ioport_ctrl, BSP_IO_PORT_01_PIN_02,
((uint32_t)IOPORT_CFG_PORT_DIRECTION_INPUT) |
((uint32_t)IOPORT_CFG_PERIPHERAL_PIN | (uint32_t)IOPORT_PERIPHERAL_AGT));
//set to input
// & set PMR to Schmitt Trigger input
// & select AGT
```

### Software-Code Example - Setting Port P000 IRQ for Schmitt Trigger Inputs

Table 19.5b Register settings for input/output pin function (PORT0)

PSEL[4:0] settings	Function	pin													
		P000	P001	P002	P003	P004	P005	P006	P007	P008	P009	P014	P015		
00000b	(Initial)	-	-	-	-	-	-	-	-	-	-	-	-	-	-
ASEL bit	Analog	-	-	-	-	-	-	-	-	-	-	-	-	-	-
ISEL bit	Interrupt	✓	✓	✓	-	✓	-	-	-	✓	✓	-	✓		

✓ : Available

- : Setting prohibited

Alternatively: if a pin has an IRQ capability, the Schmitt Trigger functionality will be also available once enabling the IRQ, like shown in the following code example:

```
R_IOPORT_PinCfg(&g_ioport_ctrl, BSP_IO_PORT_00_PIN_00,
(uint32_t)(IOPORT_CFG_IRQ_ENABLE));
```



## 2. Website and Support

Visit the following URLs to learn about key elements of the RA family, download components and related documentation, and get support:

RA Product Information	<a href="https://renesas.com/ra">renesas.com/ra</a>
RA Product Support Forum	<a href="https://renesas.com/ra/forum">renesas.com/ra/forum</a>
RA Flexible Software Package	<a href="https://renesas.com/FSP">renesas.com/FSP</a>
Renesas Support	<a href="https://renesas.com/support">renesas.com/support</a>

**Revision History**

Rev.	Date	Description	
		Page	Summary
1.00	Jan.19.24	—	Initial release

# General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

## 1. Precaution against Electrostatic Discharge (ESD)

A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity.

Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

## 2. Processing at power-on

The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

## 3. Input of signal during power-off state

Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

## 4. Handling of unused pins

Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

## 5. Clock signals

After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

## 6. Voltage application waveform at input pin

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between  $V_{IL}$  (Max.) and  $V_{IH}$  (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between  $V_{IL}$  (Max.) and  $V_{IH}$  (Min.).

## 7. Prohibition of access to reserved addresses

Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

## 8. Differences between products

Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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