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Preliminary Application Note

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μPD98412

(NEASCOT-X15™)

ATM SWITCH DEMO-BOARD

Document No. S14766EJ1V0ANJ1 (1st edition)
Date Published December 2000 NS CP(K)

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Printed in Japan

Phase-out/Discontinued

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Phase-out/Discontinued

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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Phase-out/Discontinued

PREFACE

Readers

This manual is intended for user engineers who wish to understand the functions of the μPD98412 and design application systems using it.

Purpose

This manual explains the functions of ATM switch demo-board in the following organization.

Organization

This manual consists of the following chapters.

- μPD98412 (X15) OUTLINE
- μPD98405 (S20) OUTLINE
- μPD98404 (P30) OUTLINE
- μPD98411 (P40) OUTLINE
- μPD98408 (T20) OUTLINE
- SAMPLE APPLICATION CONFIGURATION HARDWARE
- INSTALLATION
- FILE CONFIGURAION
- COMMAND
- SAMPLE APPLICATION CONFIGURATION SOFTWARE (X15EVA.dat)

How to Read This Manual

It is assumed that the readers of this manual have a general knowledge of electricity, logic circuits, and microcomputers.
The devices of NEC's NEASCOT series™ have each nickname.

- μPD98412 : X15
- μPD98405 : S20
- μPD98404 : P30
- μPD98411 : P40
- μPD98408 :T20

Conventions

Data significance	:	Left: high-order digit, right: low-order digit
Active low	:	XXX_B (_B following pin or signal name)
Memory map address	:	Top: high-order, bottom: low-order
Note	:	Explanation of part of text marked **Note**
Caution	:	Important information
Remark	:	Supplementary information
Numeric notation	:	Binary ... XXXX or XXXXb
		Decimal ... XXXX
		Hexadecimal ... 0xXXXX or XXXXh

Phase-out/Discontinued

Related documentation

Some of the related documents are preliminary editions but are not so specified below.

- μPD98412
  - Data sheet : S14237E
  - User's manual : S14169E

- μPD98405
  - Data sheet : S12689E
  - User's manual : S12250E

- μPD98404
  - Data sheet : S11822E
  - User's manual : S11821E

- μPD98411
  - Data sheet : S12953E
  - User's manual : S12736E

- μPD98408
  - Data sheet : S12313E
  - User's manual : S11409E

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CHAPTER1 μPD98412 (X15) OUTLINE

The μPD98412 (NEASCOT-X15) is an LSI integrating ATM switch functions on a single chip. It has UTOPIA Level2 interfaces and can switch 30 × 30 circuits by connecting multiple PHY devices. The μPD98412 employs a shared buffer non-blocking type switch and realizes a switch capacity of 1.5G bps by using an externally connected SRAM for buffering cells.

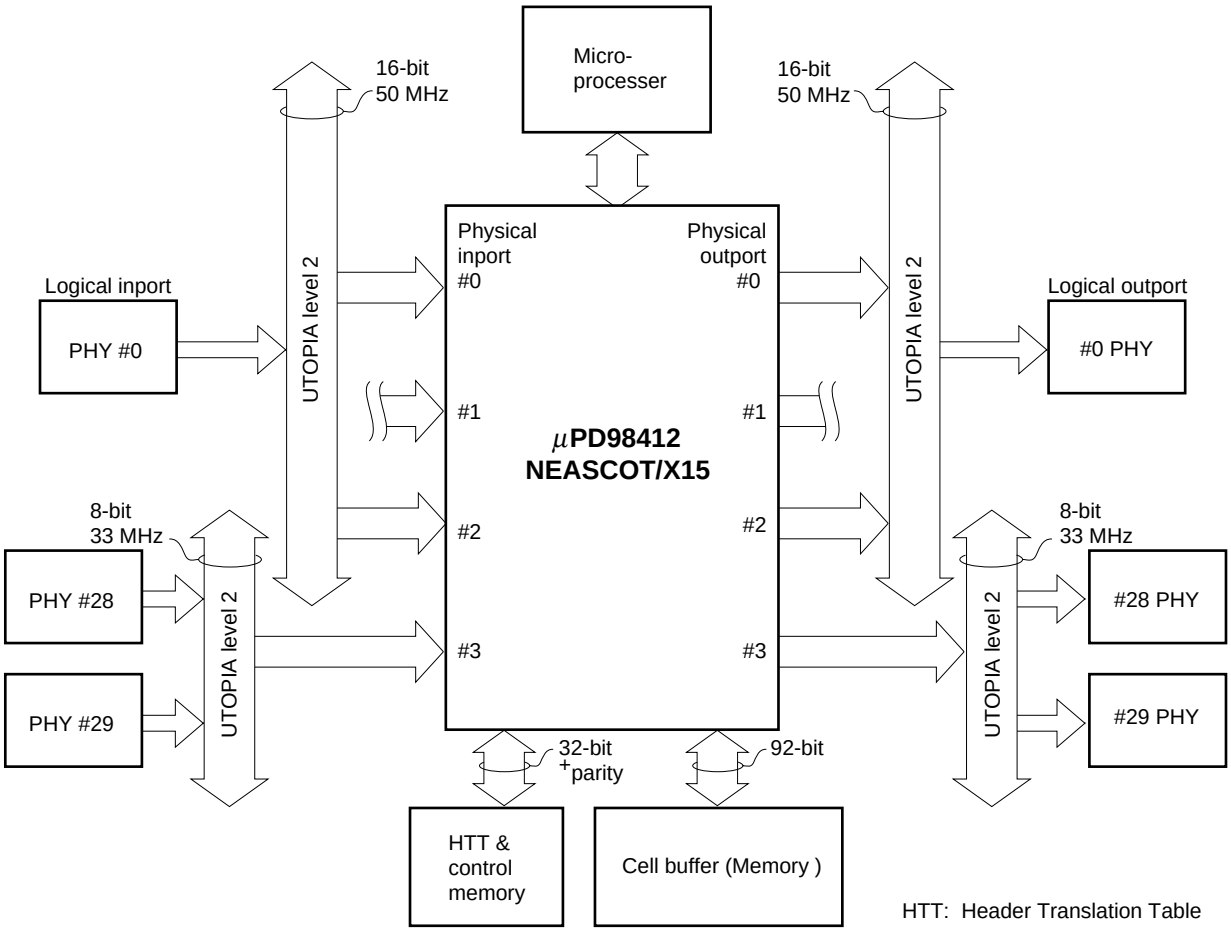
1.1 Features

- Conforms to ATM FORUM UNI Version 3.1 & Traffic Management 4.0
- Realizes all switch functions with a single chip
- Non-blocking type with switch capacity of 1.5 Gbps
- UTOPIA Level2 interface allowing you to select bit widths
  (4 ports × 8 bits, 2 ports × 8 bits + 1 port × 16 bits, 2 ports × 16 bits)
- Various polling modes for UTOPIA Level2 interface
- Can switch 30 logical ports
- Multi-speed (622 Mbps, 155 Mbps, 52 Mbps, 25 Mbps, etc.)
- Microprocessor connecting port can be set for signaling processing and OAM cell processing
- Supports 16K/32K/64K uni-cast VP/VC and 1K/2K/4K multi-cast VP/VC
- Shared buffer architecture using standard SRAM
- Cell buffer capacity: 12.8K/25.6K/51.2K cells
- Supports four QOS classes (CBR, VBR, ABR, UBR)
- ABR traffic control (binary mode)
- Supports EPD (Early Packet Discard) and PPD (Partial Packet Discard)
- +3.3-V single power source (directly connectable with +5-V TTL level signals)
- Test function: Supports JTAG (IEEE 1149.1)
- 576-pin tape BGA (40 × 40 mm)

Phase-out/Discontinued

1.2 Example of System Configuration (Application)

The μPD98412 can be used to realize an ATM layer cell switching function by connecting it to a microprocessor, SRAM for use as a cell buffer, and a header translation table (HTT)/SRAM for storing control information as shown below.



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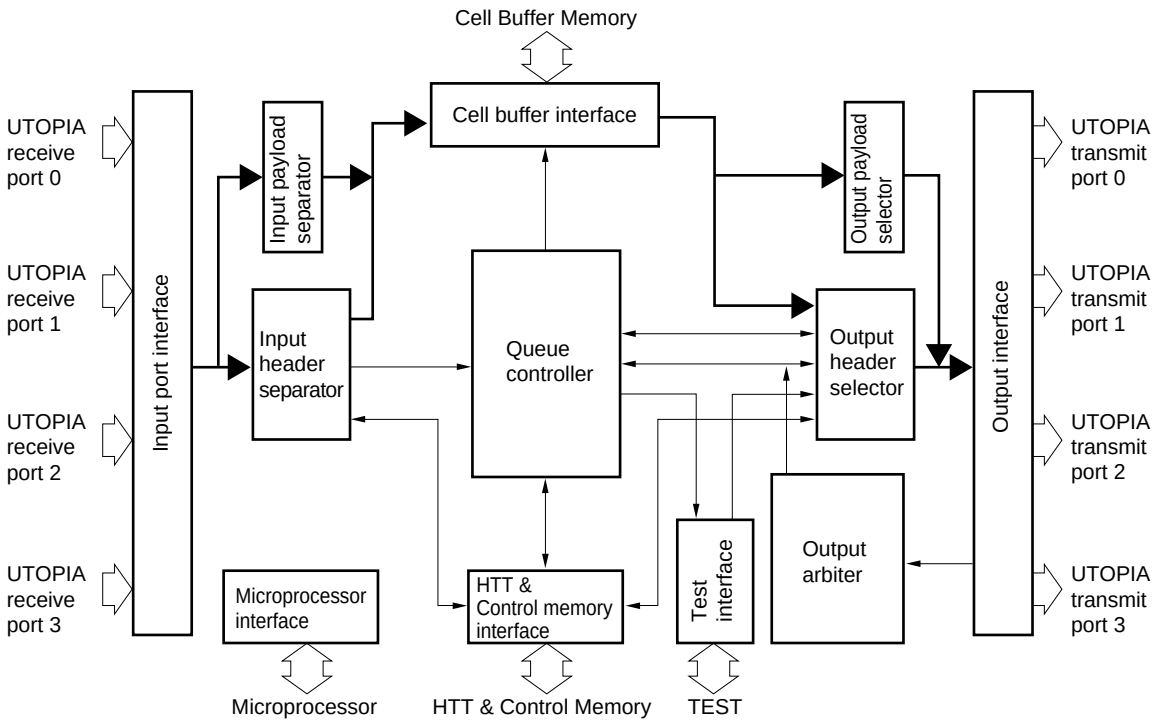
1.3 Block Diagram



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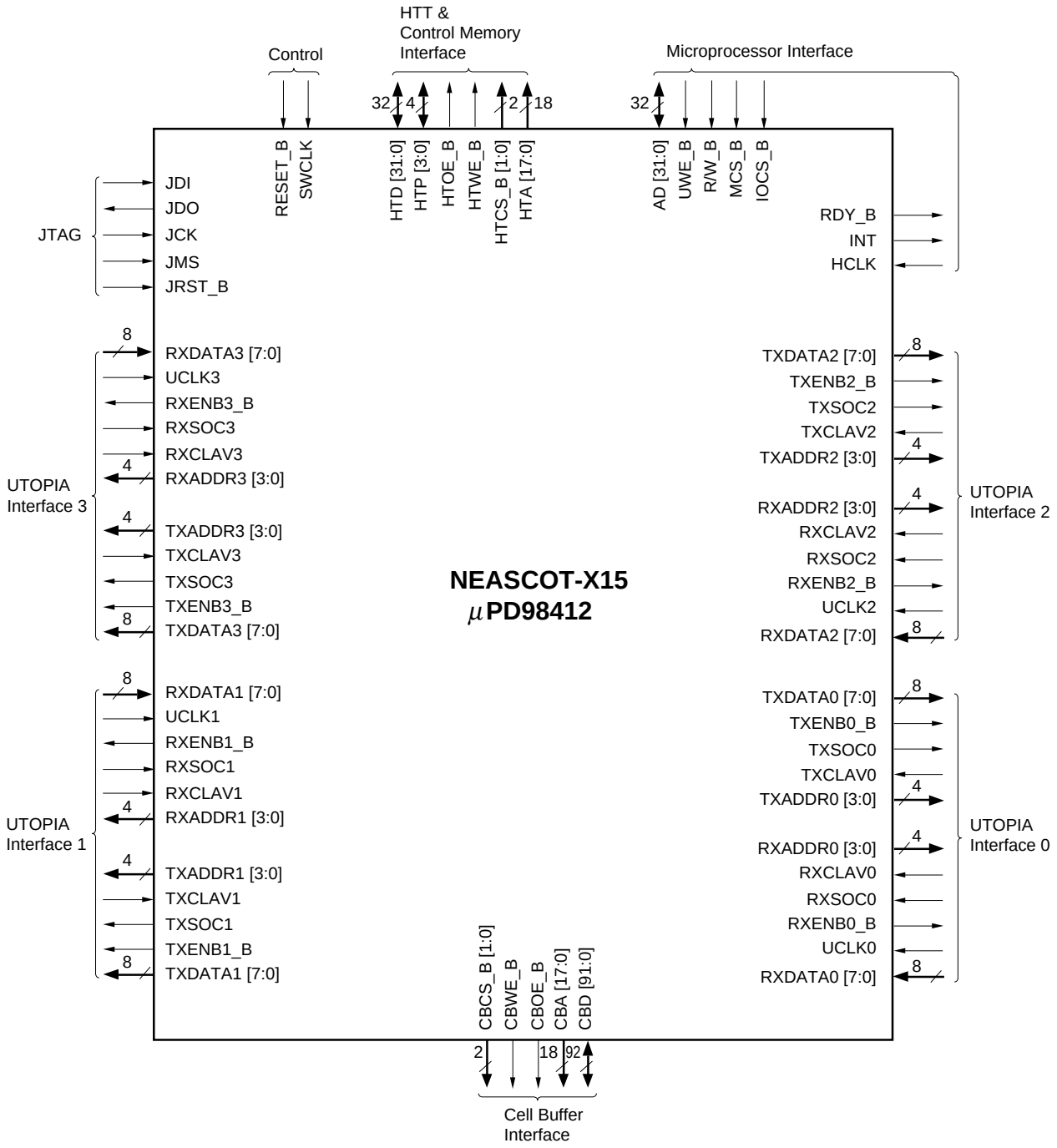
1.4 Pin Configuration

(1) 8-bit 12-PHY polling mode/15-PHY polling mode



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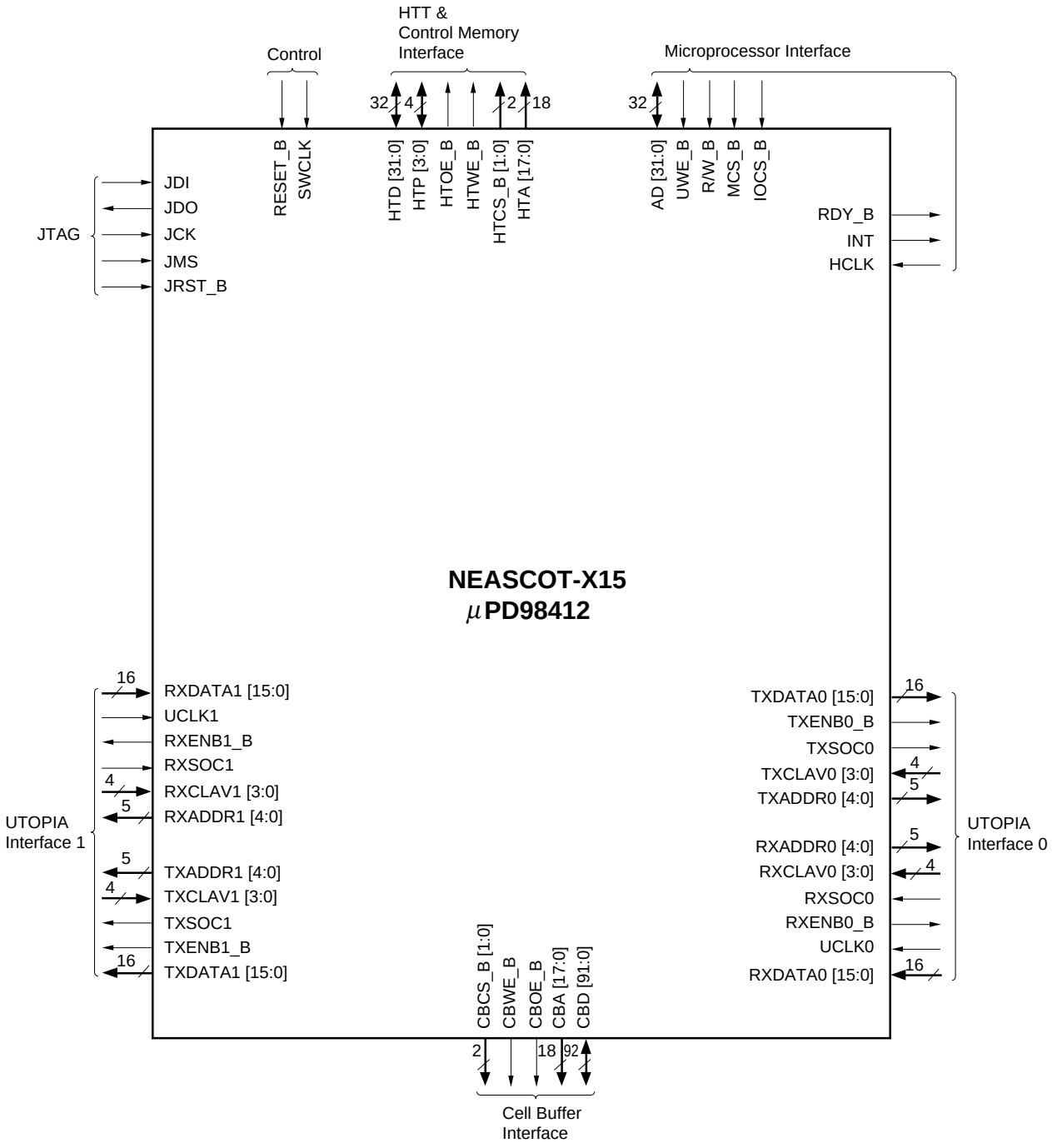
(2) 16-bit multiplexed status polling mode



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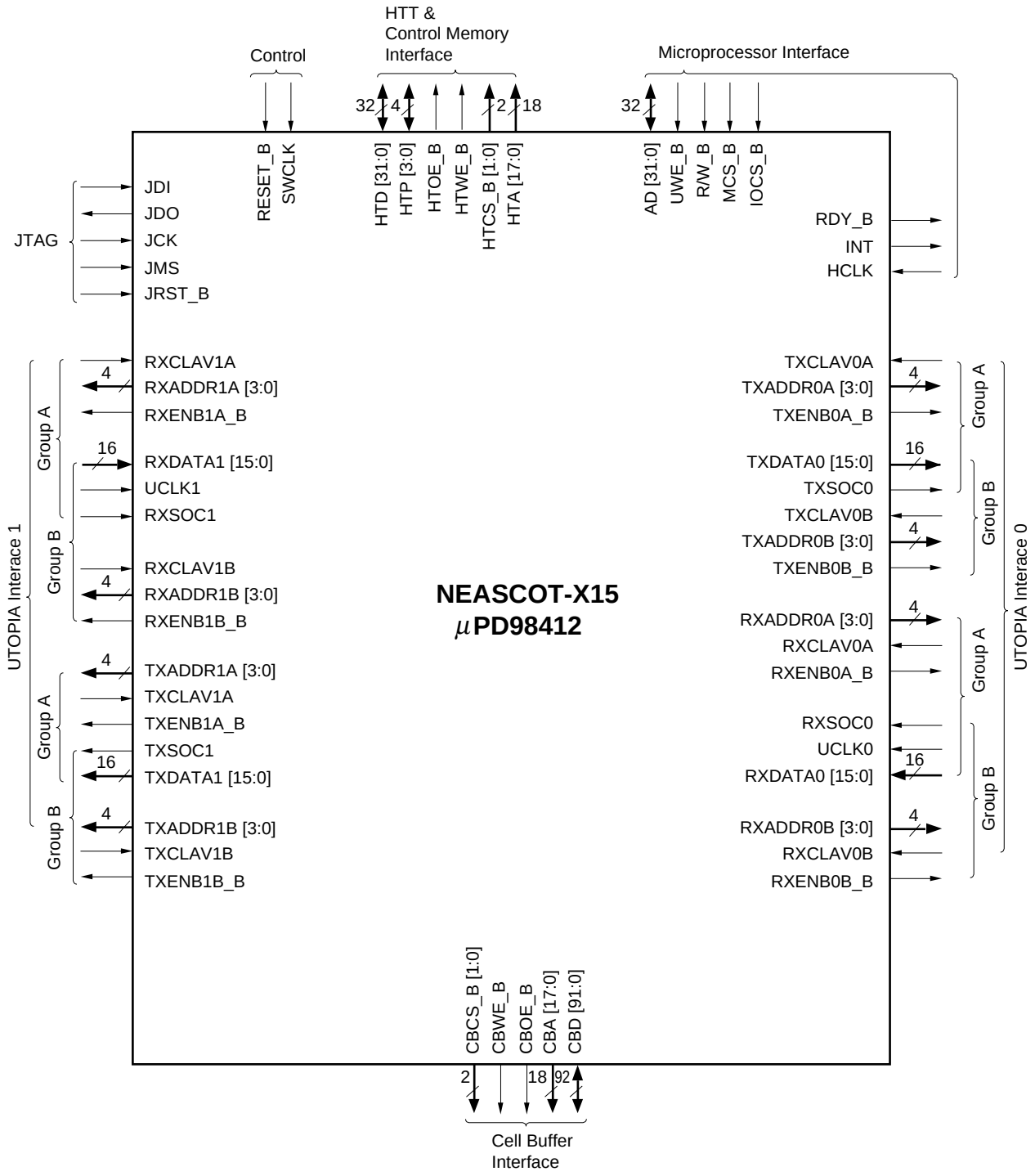
(3) 16-bit 2-group weighted polling mode



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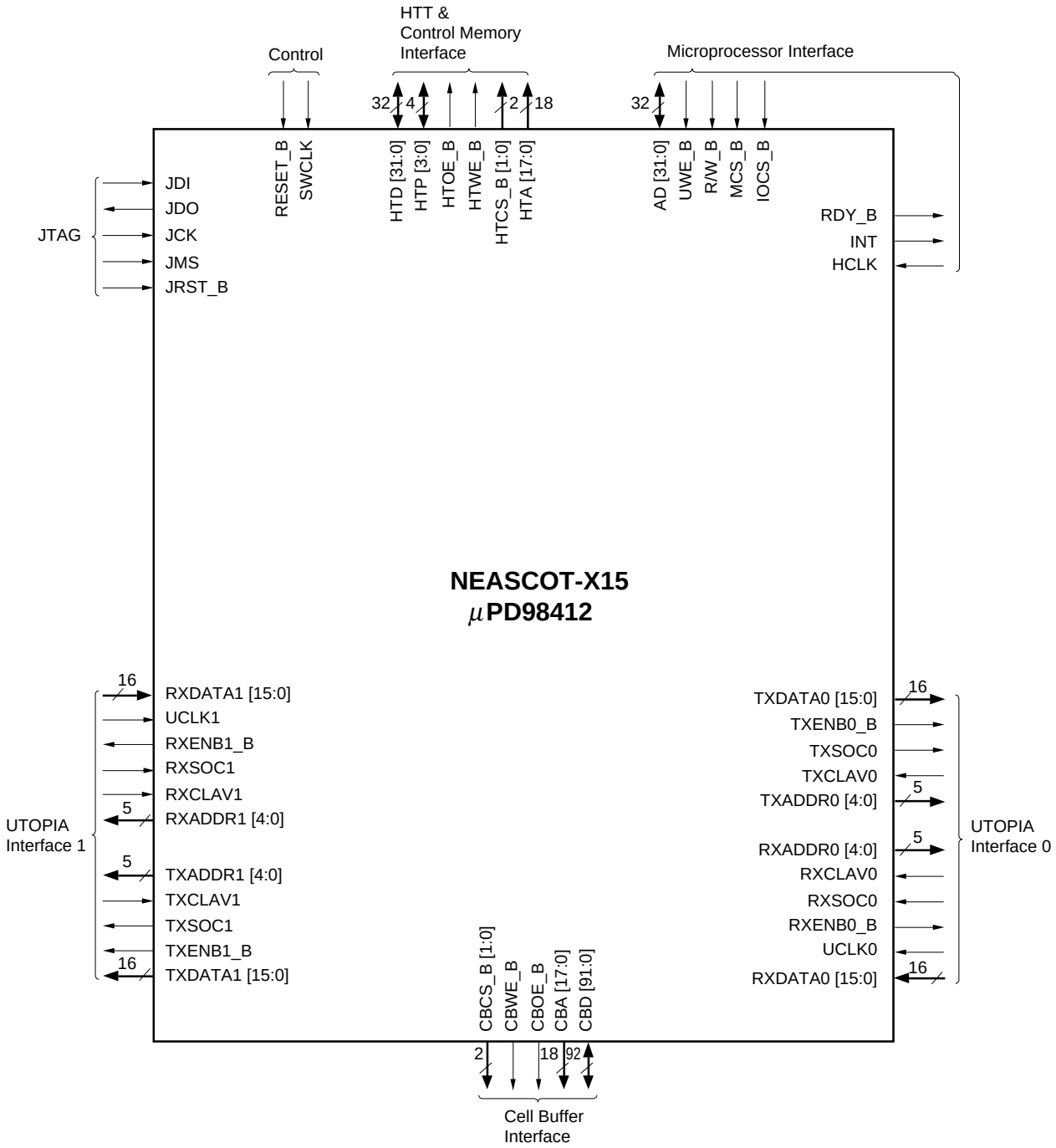
(4) 16-bit 1-group weighted polling mode



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CHAPTER 2 μPD98405 (S20) OUTLINE

The μPD98405 (NEASCOT-S20™) is a high performance ATM segmentation and reassembly chip (SAR chip). It features a PCI bus interface, a SONET/SDH 155-Mbps framer, clock recovery, and supports the ABR function in hardware. The chip conforms to the ATM Forum recommendations and implements the required AAL-5 SAR sublayer, ATM layer, and TC sublayer functions.

2.1 Features

- Conforms to the ATM Forum recommendations.
- The PCI bus and general-purpose bus are supported as host bus interfaces.
  - Built-in PCI bus interface (5/3.3 V, 32/64 bits, 33 MHz): Conforms to the PCI Specification Revision 2.1
  - General-purpose bus interface (5/3.3 V, 32 bits, 33 MHz)
- Implements the required AAL-5 SAR sublayer, ATM layer, and TC sublayer functions.
- Support of AAL-5 processing in hardware
- Software support of non-AAL-5 traffic
- Implements a SONET STS-3c/SDH STM-1 155-Mbps framer function.
- Implements clock recovery/clock synthesizer functions.
- Supports up to 32K virtual channels (VCs).
- 16 VBR traffic shapers for transmission scheduling
- Hardware support of CBR/VBR/ABR/UBR service
- Supports multi-cell burst transfer for transmission and reception.
- Implements an MIB counter.
- Supports the LAN emulation function.
- Receive FIFO which can contain up to 96 cells
- UTOPIA Level-1 interface for an external PHY layer device
- 0.35-μm CMOS technology and 5/3.3-V power supply
  - Bus interface 5 V: 5/3.3-V power supply
  - Bus interface 3.3 V: Single 3.3-V power supply
- 304-pin plastic QFP(0.5 mm, fine pitch) (40 x 40 mm)

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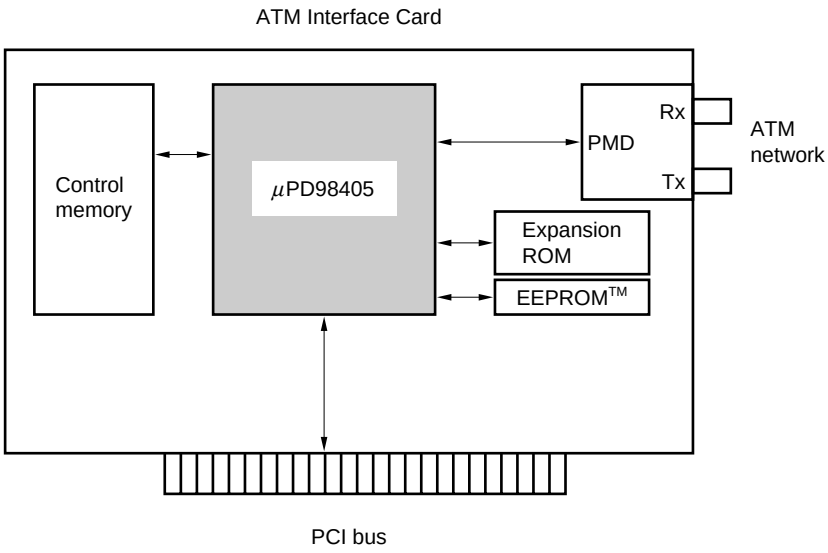
2.2 Application Example



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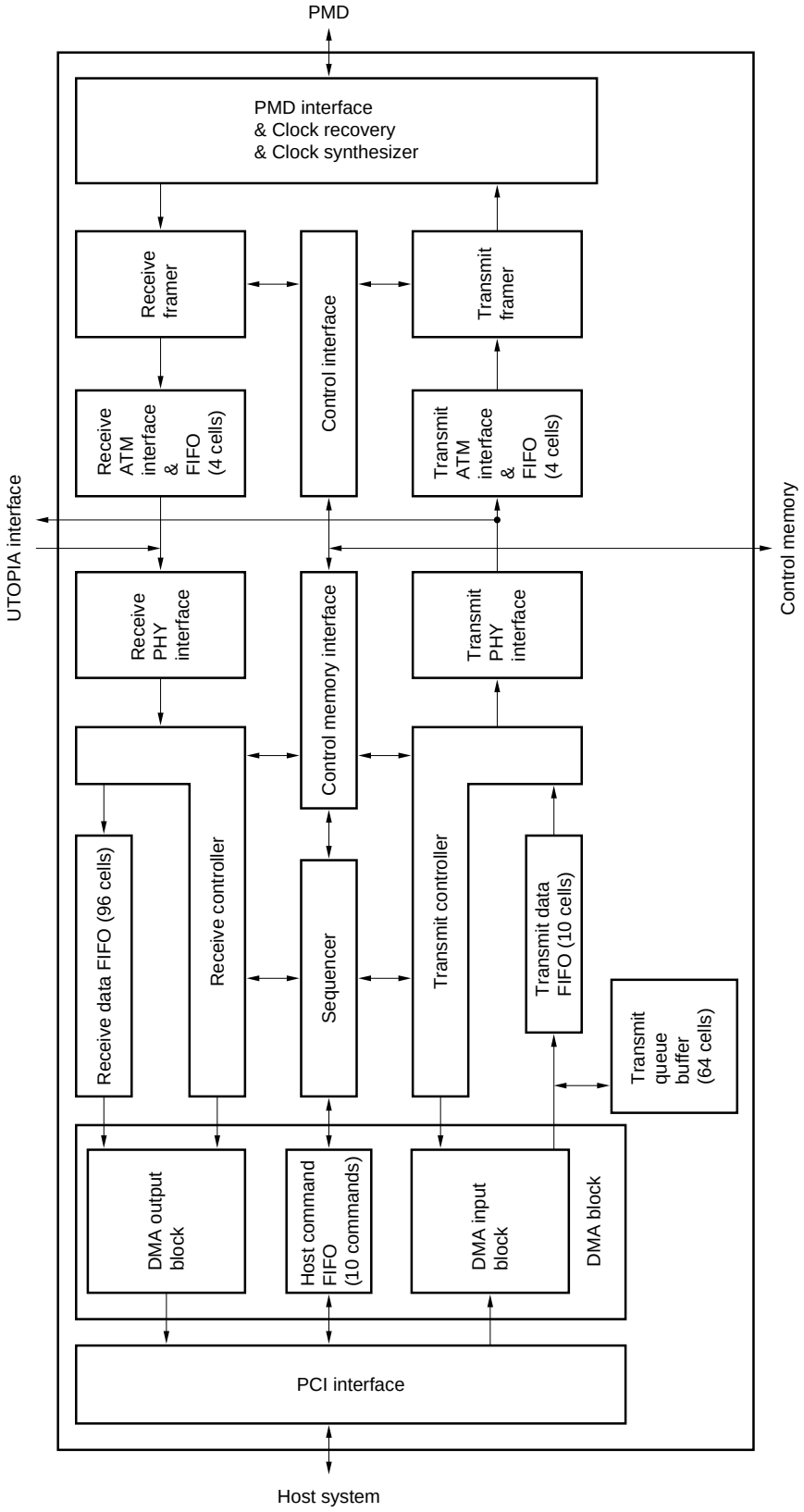
2.3 Block Diagram



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Phase-out/Discontinued

CHAPTER 3 μPD98404 (P30) OUTLINE

The μPD98404 (NEASCOT-P30™) is an LSI for ATM applications, which can be used in ATM adapter boards for connecting PCs or workstations to an ATM network and can also be used in ATM hubs and ATM switches. This LSI provides the TC sub-layer functions in the SONET/SDH-base physical layer within the ATM protocol defined by the ATM Forum's UNI3.1 recommendations.

This product's main functions include transmission functions such as mapping of ATM cells sent from the ATM layer to the payload field in a 155-Mbps SONET STS-3c/SDH STM-1 frame and transmission to PMD (Physical Media Dependent) sub-layer in the physical layer. Its reception functions include separation of the overhead from the ATM cells in data streams received from PMD sub-layer and transmission of the ATM cells to the ATM layer. In addition, this LSI includes a clock recovery function that extracts a reception sync clock from bit streams in received data and a clock synthesis function that generates a clock for transmissions.

3.1 Features

- On-chip clock recovery/clock synthesis functions
- Provides TC sub-layer function for the ATM protocol's physical layer
- Supported frame formats include 155-Mbps SONET STS-3c/SDH STM-1
- Conforms to UTOPIA interface Level 2 V1.0 (af-phy-0039.000 June 1995)
- Supports three UTOPIA interfaces:
  - Single PHY octet-level handshaking
  - Single PHY cell-level handshaking
  - Multi PHY mode
- Selectable to drop/bypass unassigned cells
- On-chip internal loopback functions for PMD layer loopback and ATM layer loopback
- Supports two PMD interfaces: serial and parallel
  - 155.52 Mbps serial interface
  - 19.44 MHz parallel interface
- Provides registers for writing/reading overhead information

  SOH (section overhead) :J0 byte, Z0 (first and second) bytes, F1 byte
  LOH (line overhead) :K1 byte, K2 byte
  POH (path overhead) :F2 byte, C2 byte, H4 byte
- Provides pseudo error frame transmit function for various errors
- Supports JTAG boundary scan test function
- CMOS process
- +3.3 V single power supply
- 144-pin plastic QFP (20 × 20 mm fine pitch package)

Phase-out/Discontinued

- Provides abundant OAM (Operation and Maintenance) functions

Transmit side

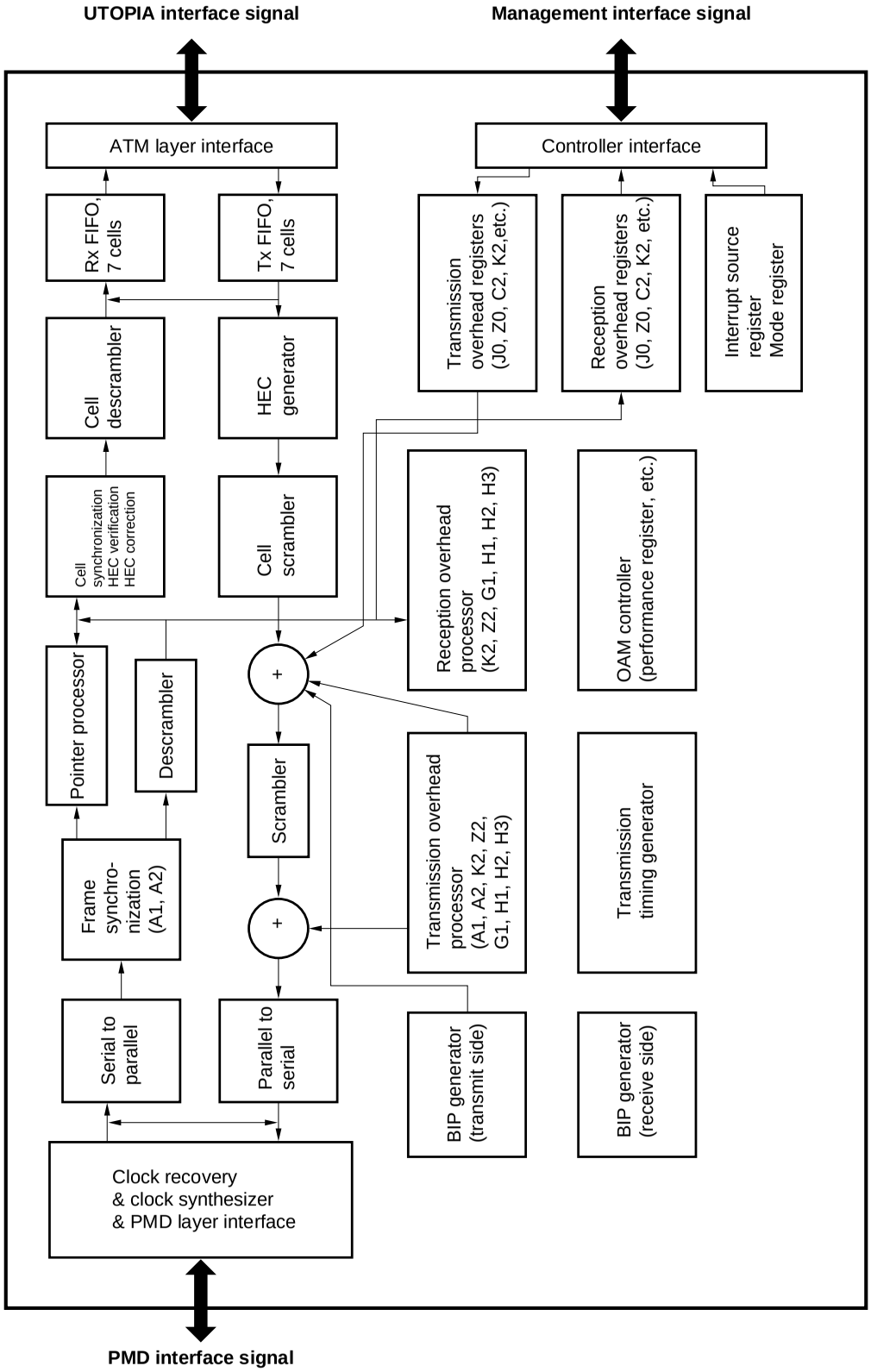
- Transmission of various alarm data
  - * Source-triggered transmission
    Line RDI (FERF), Path RDI (FERF)
    Line REI, Path REI
  - * Command-specified transmission
    Line AIS, Path AIS
    Line REI, Path REI
- Pseudo error generation frame transmission functions
  LOS generated frame
  OOF, LOF generated frame
  LOP generated frame
  OCD, LCD generated frame
  B1 error generated frame
  B2 error generated frame
  B3 error generated frame
  Line REI generation frame
  Path REI generation frame

Receive side

- Detection of alarm and fault signals
  LOS (Loss Of Signal)
  OOF (Out Of Frame)
  LOF (Loss Of Frame)
  LOP (Loss Of Pointer)
  OCD (Out Of Cell delineation)
  LOC (Loss Of Cell delineation)
  Line RDI (FERF), Path RDI (FERF)
  Line AIS, Path AIS
- Detection and display of quality loss sources
  B1 error, B2 error, B3 error,
  Line REI, Path-REI
- On-chip error counters
  B1 byte error counter (16-bit)
  B2 byte error counter (20-bit)
  B3 byte error counter (16-bit)
  Line REI error counter (20-bit)
  Path REI error counter (16-bit)
  Rx Frequency justification processing counter (12-bit)
  HEC error drop cell counter (20-bit)
  FIFO overflow drop cell counter (20-bit)
  Idle cell counter (20-bit)
  Valid cell counter (20-bit)

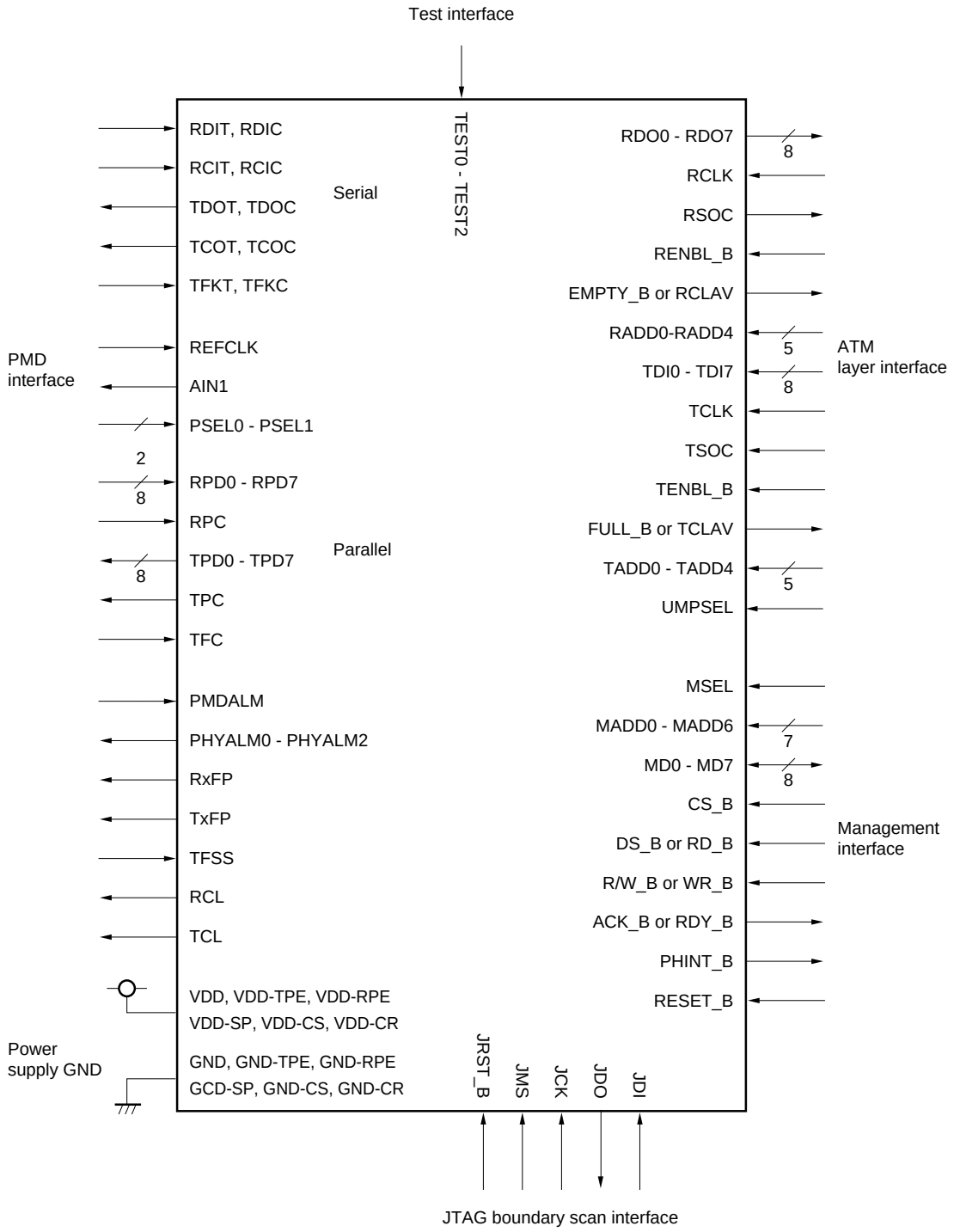
Phase-out/Discontinued

3.2 Block Diagram



Phase-out/Discontinued

3.3 Pin Configuration



Phase-out/Discontinued

CHAPTER 4 μPD98411 (P40) OUTLINE

The μPD98411 (NEASCOT-P40™) is one of ATM LSIs and provides the functions of the TC sublayer of the SONET/SDH-base physical layer of the ATM protocol specified by the ATM Forum. Its main functions include a transmission function for mapping an ATM cell passed from a high-end ATM switch device or SAR device to the payload of a 155-Mbps SONET STS-3c/SDH STM-1 frame and transmitting the cell to a transceiver at the line side, and a reception function for separating the overhead and ATM cell from the data string received from a receiver and transmitting the ATM cell to the ATM switch device or SAR device. The μPD98411 combines these transmission/reception functions into a port function that is realized as a single four-port LSI chip. This LSI is ideally suited for use in the ATM hubs, ATM switches, and other equipment used to configure an ATM network.

In addition, the μPD98411 also has a clock recovery function for each port to extract clock for reception of receive data from the bit stream, and a clock synthesis function to generate a clock for transmission.

4.1 Features

- Incorporates an ATM user network interface TC sublayer function for four channels.
- Conforms to ATM FORUM UNI v3.1.
- Incorporates four clock recovery PLLs and one clock synthesizer PLL.
- ATM layer interface conforms to ATM FORUM UTOPIA Level 2 v1.0.
  Can be selected from the multi-PHY interface (up to 800 Mbps) in several different modes.

Single 16-bit	1TCLAV/1RCLAV (Cell Available) signal mode
Single 8-bit	Direct Status Indication mode
Dual 8-bit	Multiplexed Status Polling mode

- A CPU interface can be set to either of two modes.

RD-WR-RDY style (Intel-compatible mode)
DS- R/W-ACK style (Motorola-compatible mode)

- The line-side PMD interface accepts a P-ECL level input.
- Supports a loopback function.
- Supports a pseudo error generation frame transmission function.
- Incorporates one general input port per channel and three output ports (each able to drive an LED) per channel.
- Supports JTAG boundary scan test (IEEE 1149.1).

Phase-out/Discontinued

- Incorporates a wide range of operation, administration, and maintenance (OAM) functions.

  - **Transmission**

Alarm Transmission	Line Quality Monitoring
APS	Insertion of B1-byte computation
Line AIS/Path AIS	Insertion of B2-byte computation
Line RDI/Path RDI	Insertion of B3-byte computation
	Automatic transmission of a line REI
	Automatic transmission of a path REI

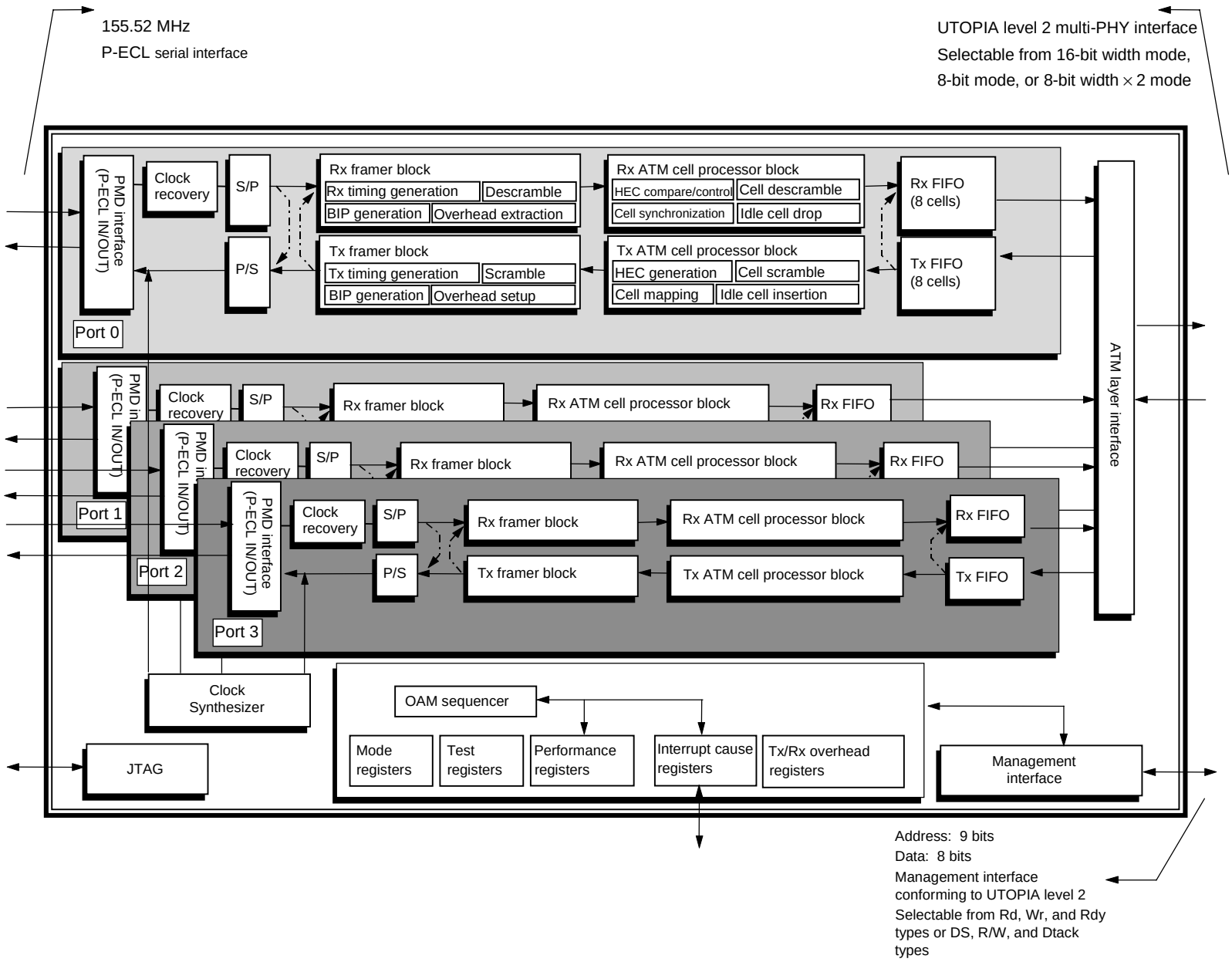
  - **Reception**

Alarm and Failure Detection	Notification of Degraded Line Quality	Line Quality Monitor Counter (24-Bit)
External input signal change	B1 error	B1 error counter
LOS	B2 error	B2 error counter
OOF	B3 error	B3 error counter
LOF	Line REI	Line REI counter
LOP	Path REI	Path REI counter
OCD	Frequency justification	Frequency justification counter
LCD	FIFO overflow	HEC processing dropped cell counter
Line AIS/path AIS		FIFO overflow dropped cell counter
Line RDI/path RDI		Received idle cell counter
APS		Valid cell counter

- 0.35-μm CMOS process
- Low power consumption; +3.3 V single-voltage power supply
- 240-pin QFP package (0.5-mm fine pitch, 32 × 32 mm)

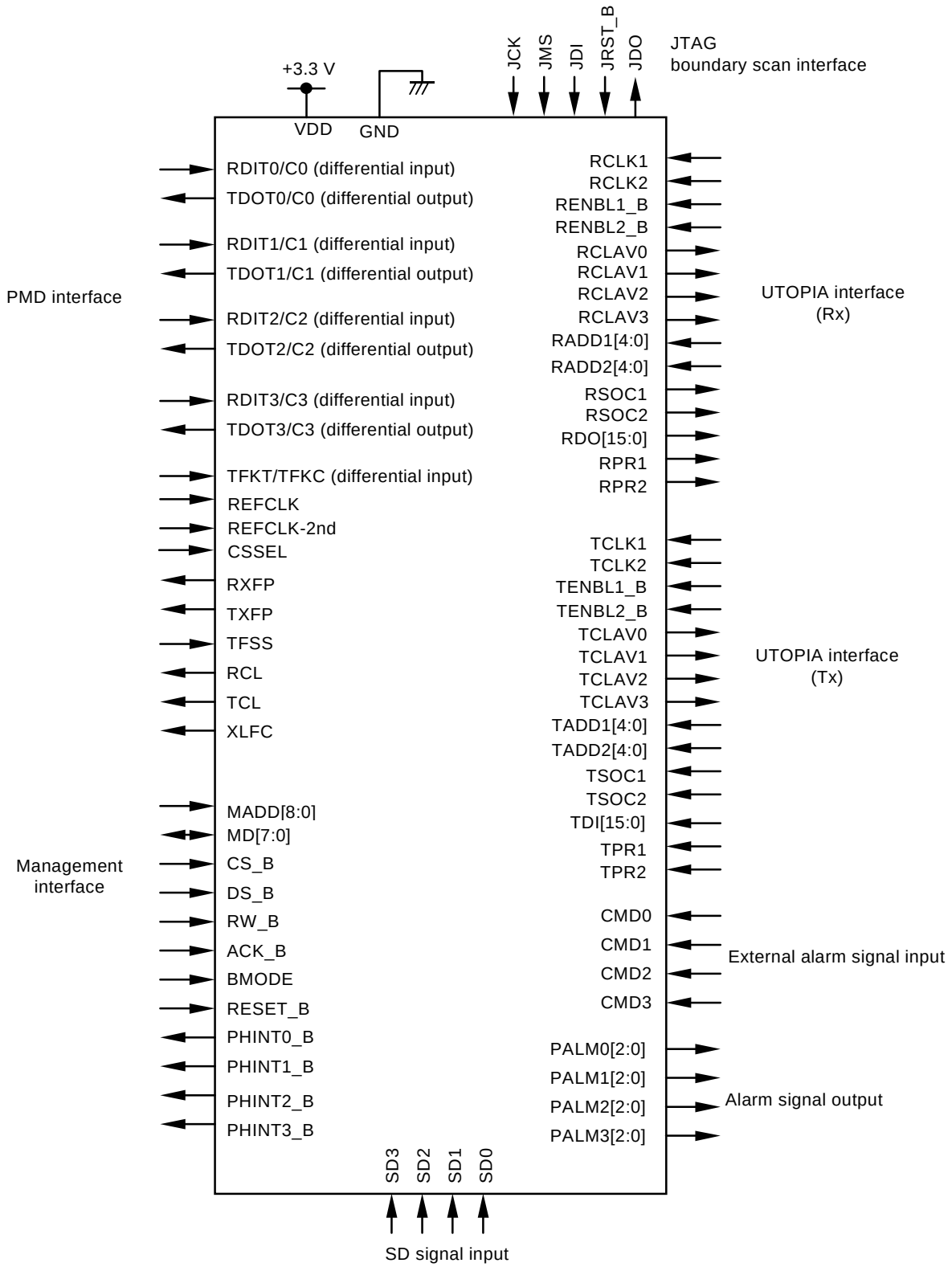
Phase-out/Discontinued

4.2 Block Diagram



Phase-out/Discontinued

4.3 Pin Configuration



Phase-out/Discontinued

CHAPTER 5 μPD98408 (T20) OUTLINE

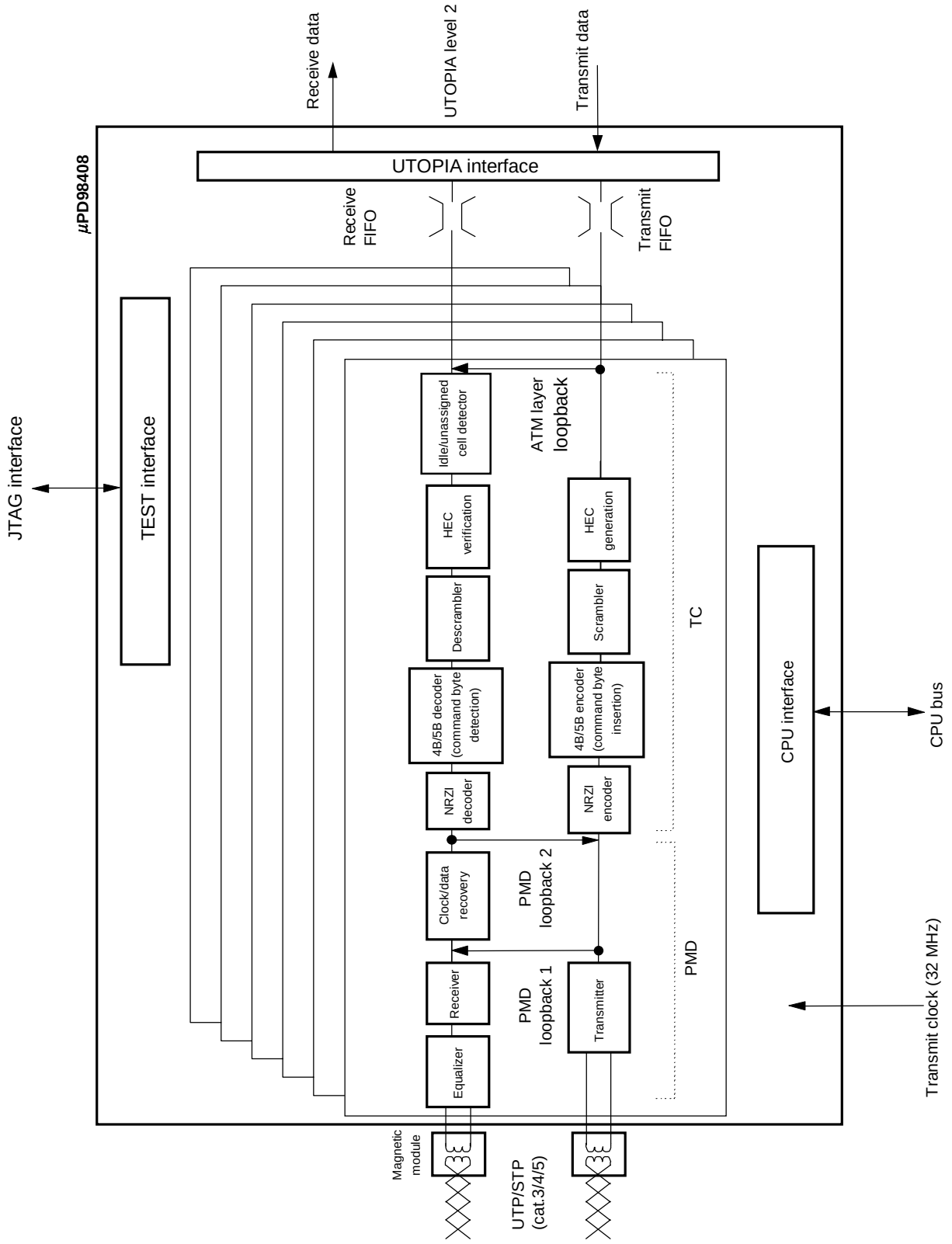
The μPD98408 is an ATM physical layer LSI IC that complies with ATM25 (25.6 Mbps) and which supports TC sublayer and PMD sublayer functions. Interfacing with the ATM layer and AAL layer LSI is implemented at UTOPIA Level 2.

5.1 Features

- Provides a 25.6-Mbps ATM PHY (PMD & TC) function for six circuits
- Conforms to the ATM Forum PHY interface specifications (af-phy-0040.000 November 1995).
- UTOPIA Level 2 V1.0 (af-phy-0039.000 June 1995: max. 8 bits/40 MHz) interface
- Three-cell built-in transmit/receive FIFOs for each circuit
- PMD sublayer functions:
  (a) Built-in clock recovery.
  (b) Built-in equalizer.
- TC sublayer functions:
  (a) NRZI encoder/decoder.
  (b) Command byte insertion/detection.
  (c) 4B/5B encoder/decoder.
  (d) Cell scrambler/descrambler.
  (e) HEC generation/verification.
- CPU interface: Intel or Motorola can be selected.
- Supports STP and UTP (Categories 3, 4, 5).
- Loopback function: Loopback in the PMD and ATM layers.
- Operation And Maintenance (OAM) functions: Input failure detection, HEC error detection and 4B/5B code error detection.
- Test function: Supports JTAG.
- Power supply voltage: 3.3 V ± 5 %.
- 208-pin plastic QFP (fine pitch) (28 × 28 mm)

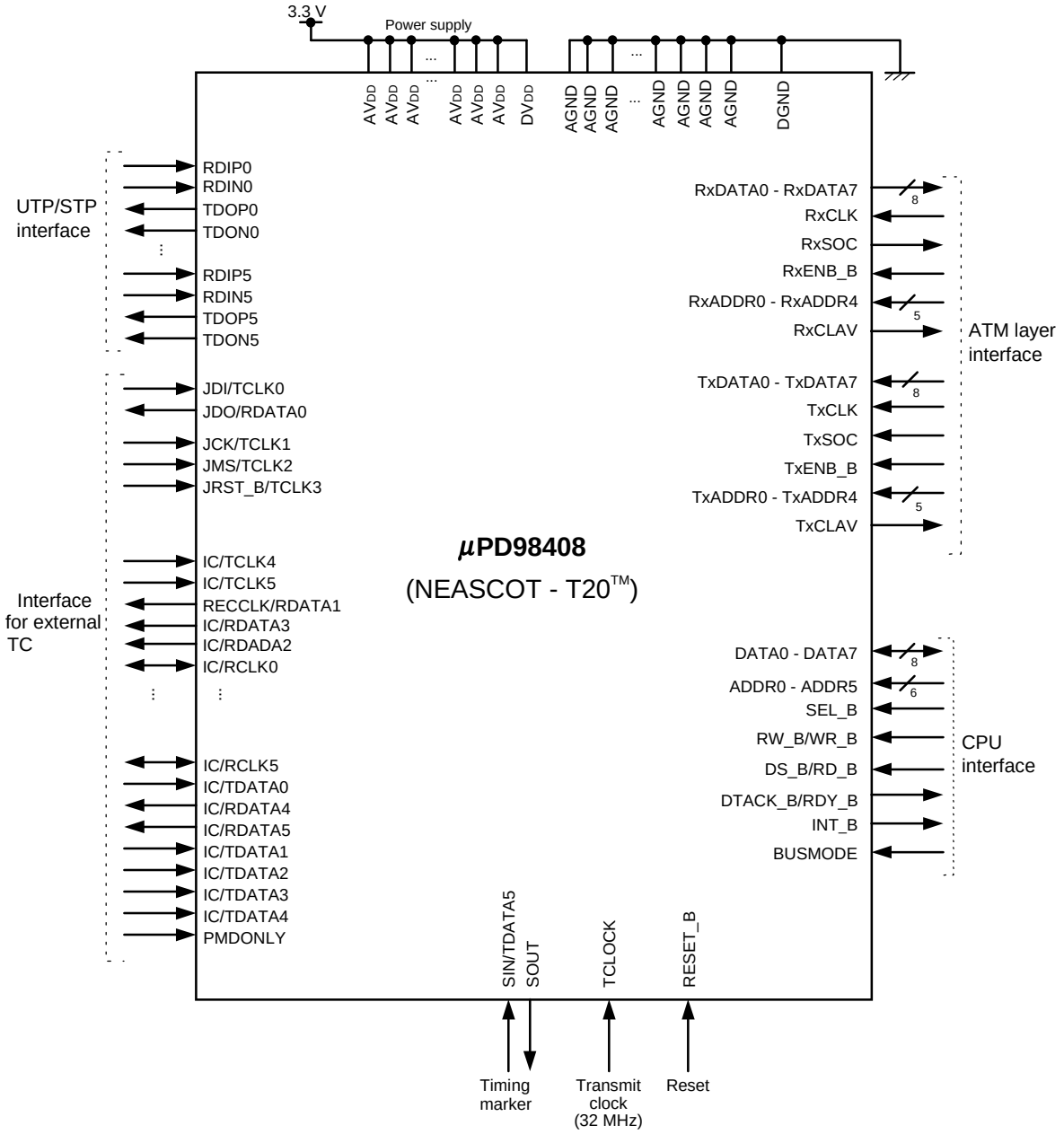
Phase-out/Discontinued

5.2 Block Diagram



Phase-out/Discontinued

5.3 Pin Configuration



Phase-out/Discontinued

[MEMO]

Phase-out/Discontinued

CHAPTER 6 SAMPLE APPLICATION CONFIGURATION HARDWARE

This demo-board was designed as an example application, showing how to use NEC's ATM devices to build a simple ATM switch.

Additionally it gives the possibility to get easily familiar with the existing ATM devices like X15, S20, T20, P30 and P40.

- **Outline**

This demo card is a small ATM switch card that uses as a main device the 1.5 Gbps ATM switch LSI X15 (μPD98412). It consists of a X15 ATM switch demo-board, which contains the PCI-bridge and the switching LSI as well as a cell generator.

Through UTOPIA-connectors additional PHY modules can be plugged-in.

These cards give the opportunity to use it by simply plug into the PCI slot of a PC and it can work as simple ATM switch for many multimedia applications.

- **Features**

X15 ATM switch demo-board: μPD98412 (X15) with the maximum memory capability (51.2K cell)
μPD98405 (S20) as PCI-bridge, management control and ATM cell generator device μPD98404 (P30) as a cell generator PHY (no external ATM equipment needed, e.g. second ATM NIC)
4 UTOPIA Level-2 (8-bit) connectors for PHY module extension

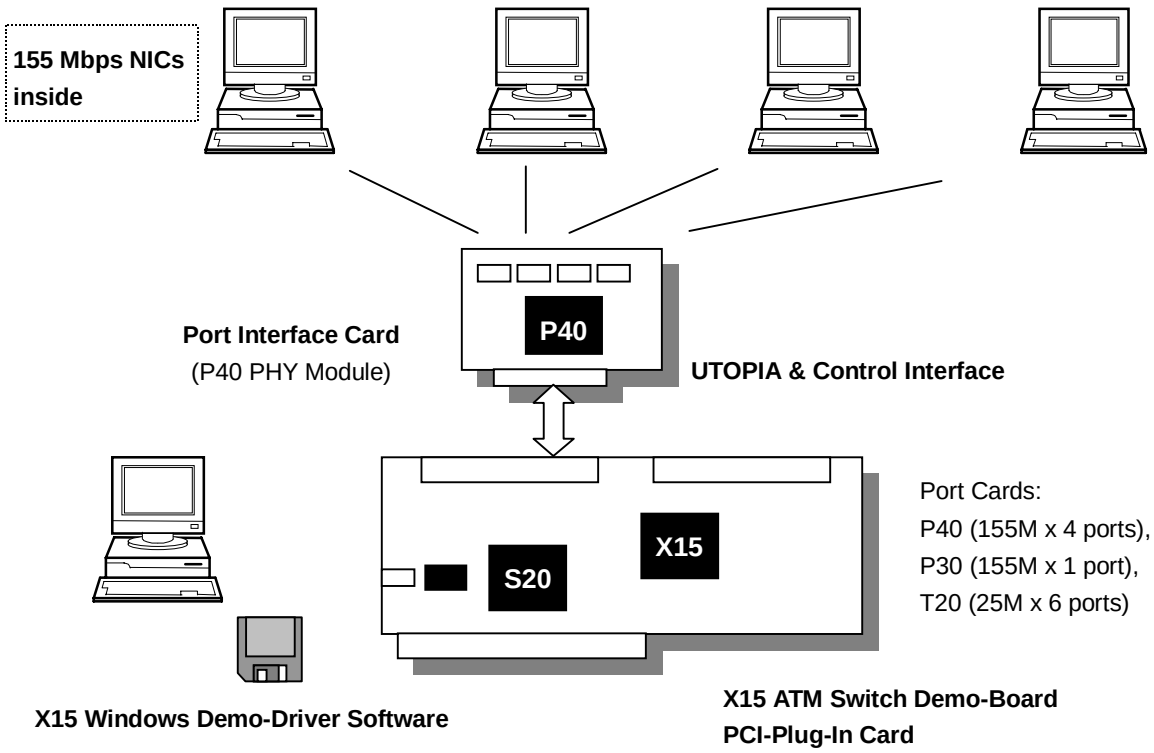
PHY module1: μPD98411 (P40) with four 155M optical transceivers
2: μPD98404 (P30) with one 155M optical transceiver
3: μPD98408 (T20) with six 25M electrical transceivers

Phase-out/Discontinued

6.1 Working System Configuration

(1) Example1 (Network solution)

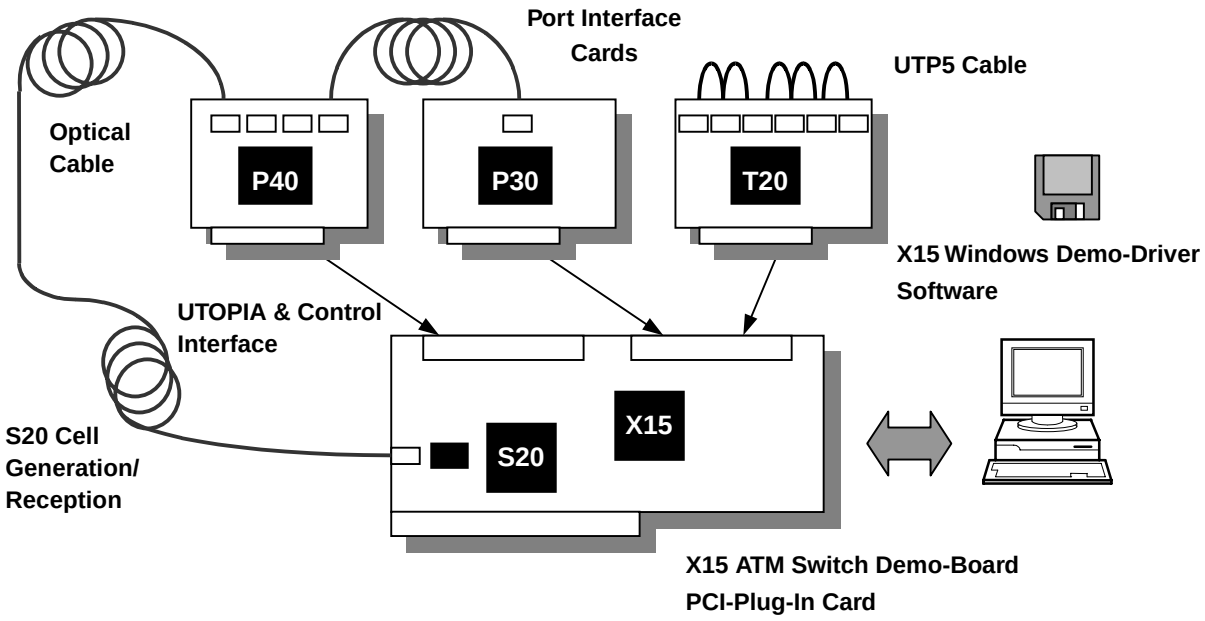
X15 ATM Switch Demo-Board
P40 PHY Module
PC with PCI Interface
X15 Windows™ Demo-Driver Software
PCs with OC-3 ATM NICs Interfacing to the P40 Card
MMF (Multi-Mode optical Fiber)



Phase-out/Discontinued

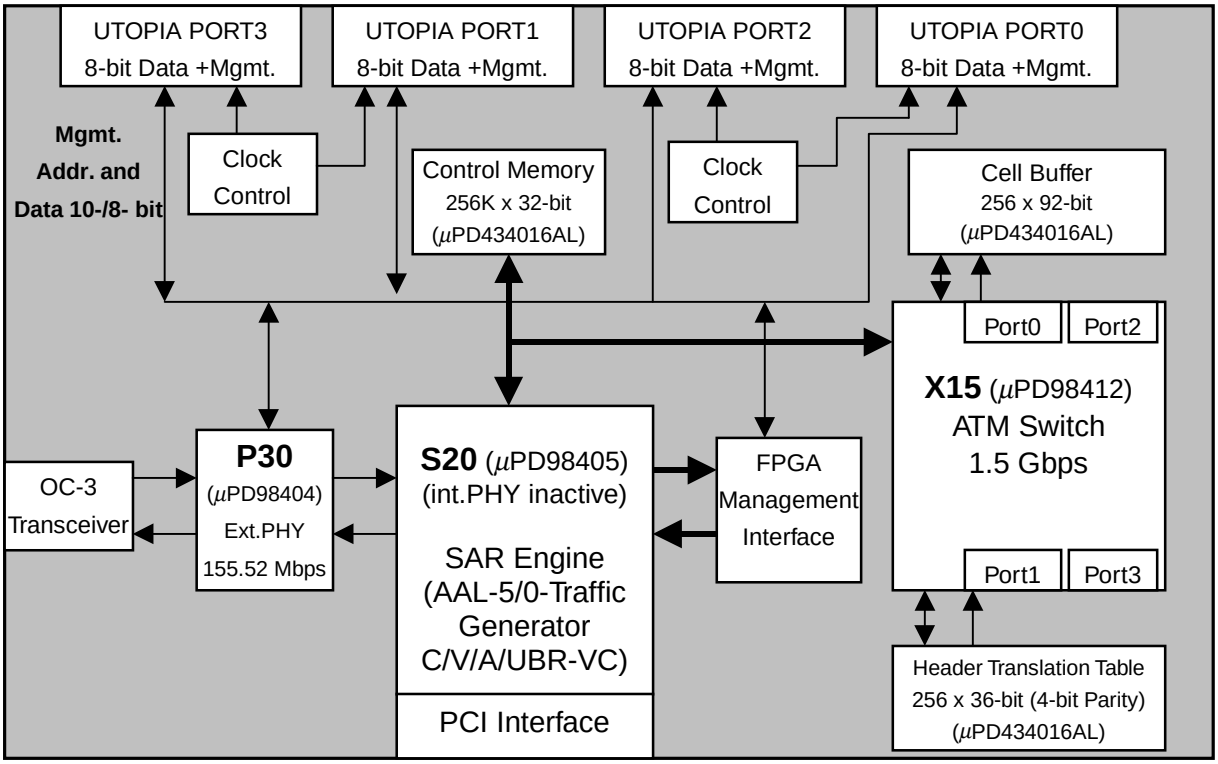
(2) Example2 (Standalone solution with S20 traffic generation)

X15 ATM Switch Demo-Board
P40 PHY Module
P30 PHY Module
T20 PHY Module
PC with PCI Interface
X15 Windows Demo-Driver Software
MMF (Multi-Mode optical Fiber)
UTP (Unshelled Twist Pair cable)



Phase-out/Discontinued

6.2 Block Diagram



PCI Local Bus: Based on PCI REV2.1, 64- or 32-bit/33 MHz

PCI bridge inside μPD98405 (S20)

FPGA Management Interface to access the internal registers

μPD98412 (X15): 1.5 Gbps ATM switch

Cell Buffer (6 SRAM ICs with 4M-bit each): Fast SRAM to buffer the cells

HTT and Control Buffer (3 SRAM ICs with 4-Mbit each): Fast SRAM for Header Translation Table and Queue Control

Four 8-bit UTOPIA Level-2 connectors: Two can be combined to build a 16-bit UTOPIA interface, which is needed for the P40 Board

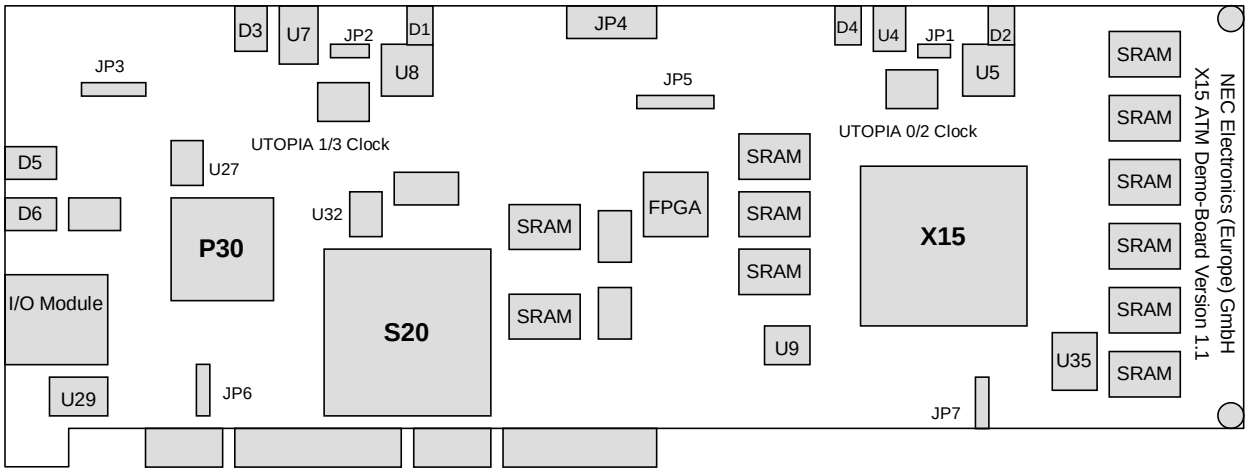
μPD98405 (S20): Used as PCI bridge, Traffic Generator and Management Control

μPD98404 (P30): Used as a Traffic Generator PHY

Clock control: Provides the UTOPIA clocks for the PHY modules

Phase-out/Discontinued

6.3 X15 ATM Switch Demo-Board Appearance (Top)



JP1: Three pins (1,2,3) Shunt 1,2:common clock U4 for UT0 + UT2, Shunt 2,3: separate clock U4 for UT0, U5 for UT2

JP2: Tree pins (1,2,3) Shunt 1,2:common clock U7 for UT1 + UT3, Shunt 2,3: separate clock U7 for UT1, U8 for UT3

JP3: 5 jumper to use PCI voltage source for PHY modules **(Caution DO NOT USE JP4 IF JP3 SHUNTS ARE CONNECTED!)**

JP4: Power connector for PHY modules **(Caution DO NOT USE JP4 IF JP3 SHUNTS ARE CONNECTED!)**

JP5: For programming the FPGA

JP6: Leave open!

JP7: Leave open!

D1 : UTOPIA 1 Receive/Transmit (TXENB1_B and RXENB1_B)

D2 : UTOPIA 0 Receive/Transmit (TXENB0_B and RXENB0_B)

D3 : UTOPIA 3 Receive/Transmit (TXENB3_B and RXENB3_B)

D4 : UTOPIA 2 Receive/Transmit (TXENB2_B and RXENB2_B)

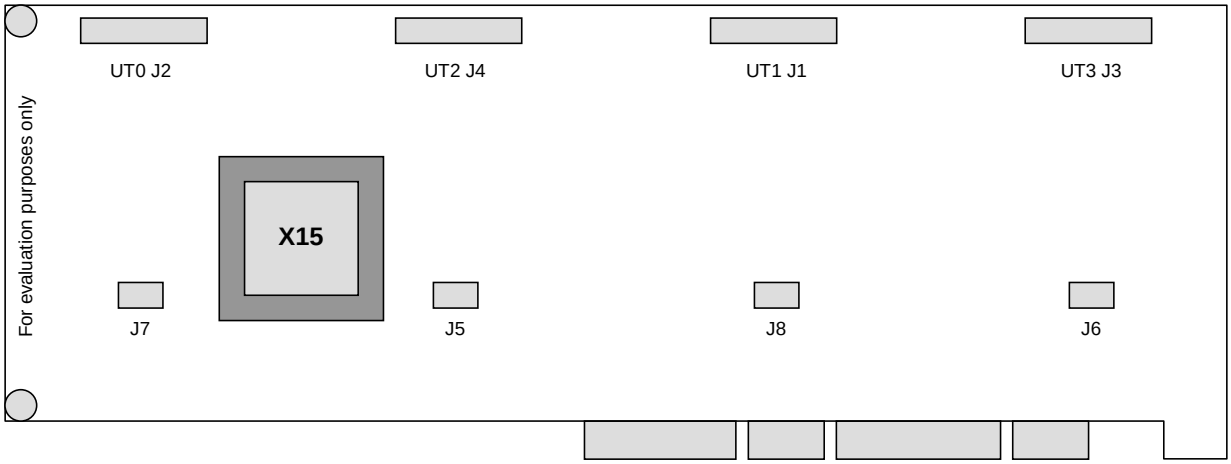
D5 : PHY-Alarm (P30: PHYARM0)

D6 : Synchronization (Optical Module Synchronization)

U7, U8, U4, U5: UTOPIA oscillators

Phase-out/Discontinued

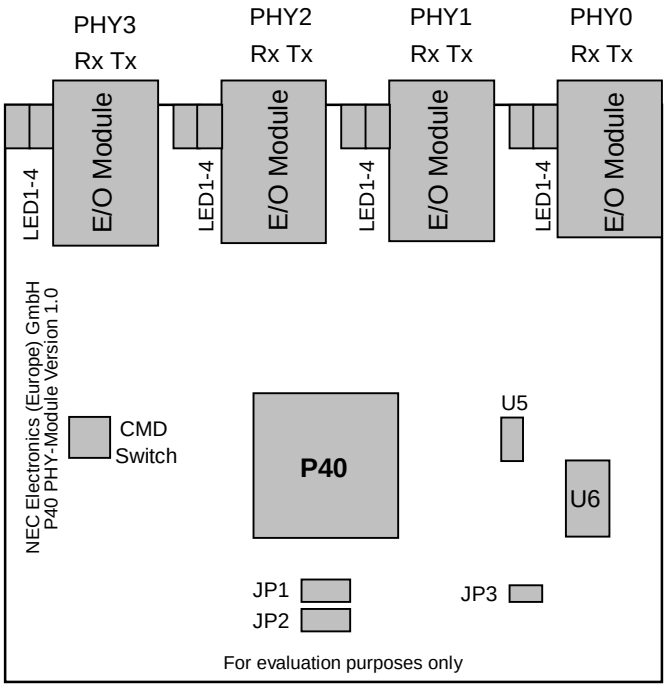
6.4 X15 ATM Switch Demo-Board Appearance (Bottom)



J1 - J8 to connect with PHY Modules

Phase-out/Discontinued

6.5 P40 PHY Module Appearance



JP1: Three pins (1,2,3) (Connect 1,2 = address polling), (Connect 2,3 = multiplexed status polling)

JP2: Three pins (1,2,3) (Connect 1,2 = address polling), (Connect 2,3 = multiplexed status polling)

JP1 and JP2 must be connected identically (e.g. left aligned 1-2 or right aligned 2-3)

JP3: Open

U5 : P40 Transmit PLL-clock (19,44 MHz)

U6 : Voltage Regulator

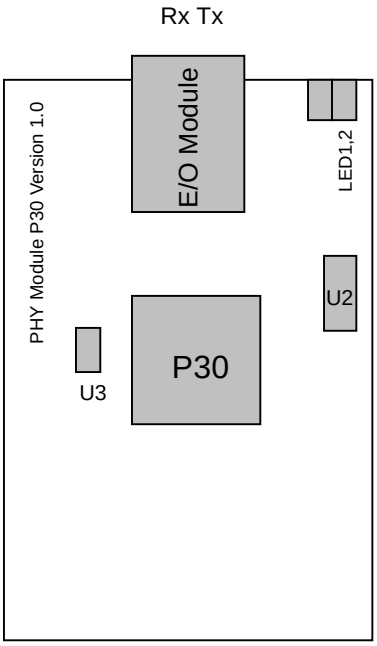
CMD Switch: Switch open -> P40 CMDx = 1, Switch closed -> P40 CMDx = 0

LED1-4: Green :P40 synchronized

Red :P40 PARM pins 1-3

Phase-out/Discontinued

6.6 P30 PHY Module Appearance



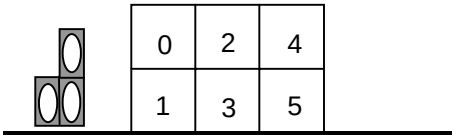
U2: Voltage Regulator

U3: Transmit PLL-clock (19.44 MHz)

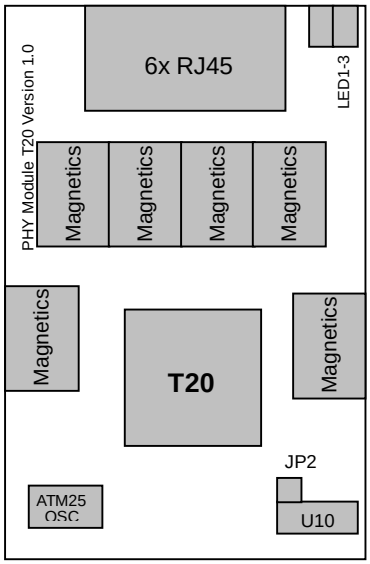
LED1,2: Green : Synchronization
(Optical Module Synchronization)
Red : PHY-Alarm (P30: PHYARM0)

Phase-out/Discontinued

6.7 T20 PHY Module Appearance



RJ45 Connector Number



JP2: open

U10: Voltage Regulator

LED1-3: Green: Transmit/Receive UTOPIA (T20: TXENB_B and RXENB_B)

Red : Interrupt (T20: INT_B)

Phase-out/Discontinued

[MEMO]

Phase-out/Discontinued

CHAPTER 7 INSTALLATION

7.1 Hardware Installation

Shut off the PC and unplug power cord. Connect X15 ATM switch demo-board and the relevant PHY modules. Check jumper settings due to CHAPTER 6.

There are several connections possible. Each UTOPIA interface of the X15 ATM switch demo-board can be connected to one PHY module or 2 UTOPIA interfaces have to be used together to plug-in the P40 PHY module.

Caution Use only PORTS 0 and 2 or 1 and 3 together. Never insert the P40 PHY module into the middle of X15 ATM switch demo-board (Ports 2 and 1).

Example: X15 ATM switch demo-board, two T20 PHY Module, and two P30 PHY module.

Caution The external hardware connection must be reflected inside the correspindent X15EVA.ENV file of your software package.

In the former example (two T20, two P30) the X15EVA.ENV must include.

```
# UTOPIA_num, target
Phy0 P30
Phy1 P30
Phy2 T20
Phy3 T20
```

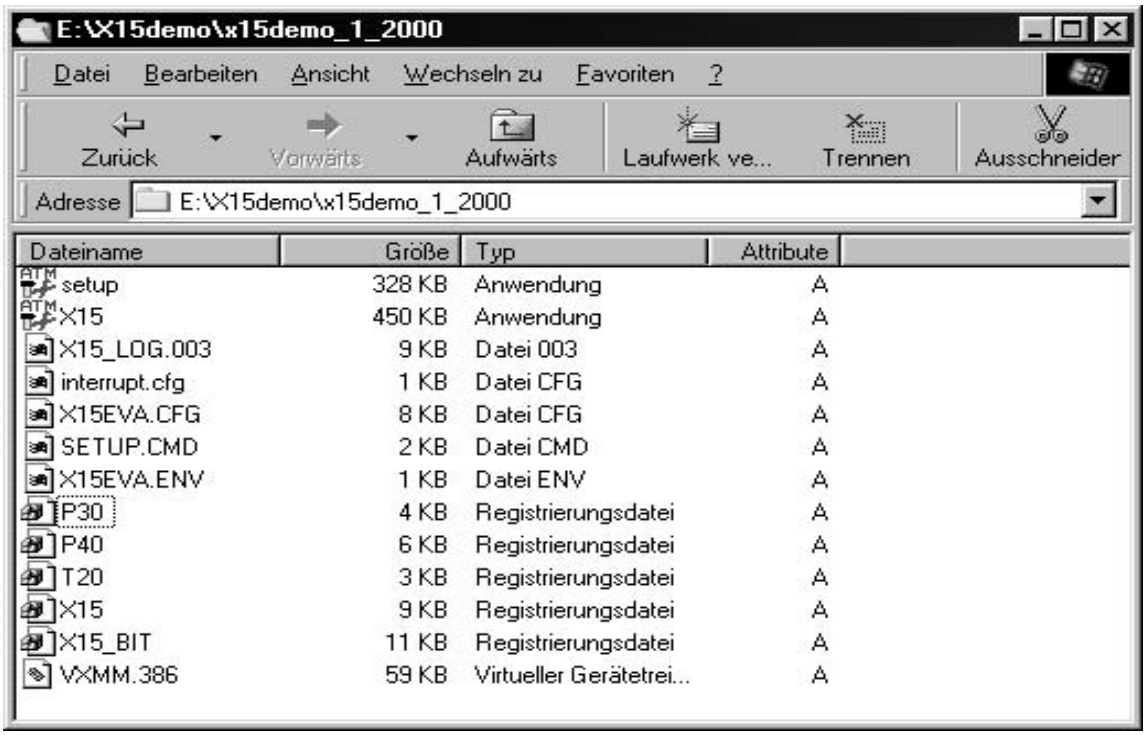
An additional example is the connection of two P40 PHY module with 16 bit interfaces. Now one has to combine two 8-bit UTOPIA interfaces to one 16-bit interface. **UTOPIA 0 and UTOPIA 2 must be addressed as Phy2 and UTOPIA 1 and UTOPIA 3 as Phy3.**

```
# UTOPIA_num, target
Phy2 P40
Phy3 P40
```

Phase-out/Discontinued

7.2 Software Installation

The picture below shows the files, needed to get the X15 ATM switch demo-board running.



Each file has a special meaning and is described as follows:

SETUP: An . EXE file. Initializes the hardware within the OS. Uses “VXMM.386” system file for interrupt control, host system memory assignment and access to the X15 ATM switch demo-board hardware. **This program has to run first for initialization.**

X15: A . EXE file. Main program to start X15 ATM switch demo-board.

X15_log.003: A log file. Every command is recorded here.

Interrupt.CFG: Enables interrupt ability on P40 devices.

X15EVA.CFG: Includes the initialization of the whole X15 ATM switch demo-board.

SETUP.CMD: A command file mainly used to open the traffic generation of S20. User normally do not touch this file.

X15EVA.ENV: Specifies the available ATM devices with their register configuration. Additionally this file must include the real hardware situation of the connected PHY modules to the X15 ATM switch demo-board (**See also 7.1 Hardware Installation**.)

P30: A .reg file. Describes the register names of P30. Due to this file you can chose registers by their names

P40: A .reg file. Describes the register names of P40.

T20: A .reg file. Describes the register names of T20.

X15, X15_BIT: A.reg files. Describe the register and bit names of X15.

VXMM.386: System file for the hardware

Caution The software package must be stored within a path-name that is up to 8 characters long (MS-DOS™ Convention).

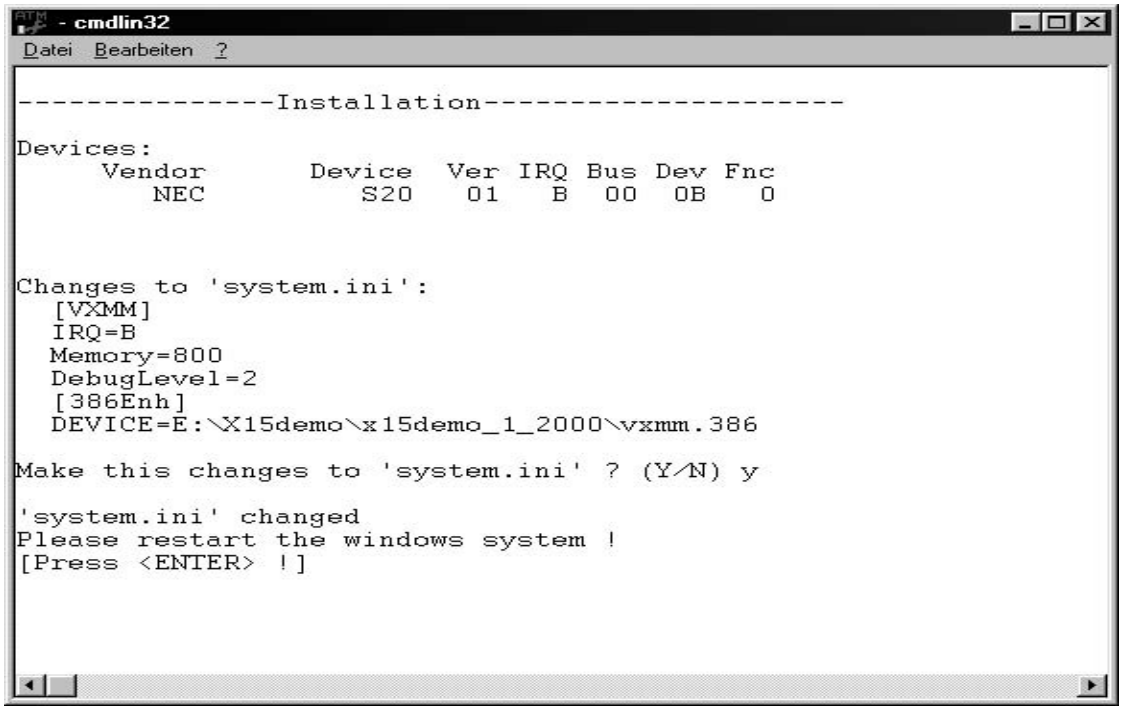
Phase-out/Discontinued

After copying the software and installation of the hardware the PC has to be restarted.
Now the following windows of the Hardware Assistant will appear:
The Hardware Assistant window shows:

1. Looking for a device driver within a certain path. Click -> Next
2. Click to: List of driver in certain paths. Click -> Next
3. A list of drivers pops up. Choose: OTHER COMPONENTS. Click -> Next
4. Shows Model: Not supported device. Click -> Next
5. A warning pops up. Ignore the warning. Click -> YES
6. Asks now to install the driver. Click -> Next
7. Responds to the installation with a big yellow “?” Click -> Finish

Now the OS should work as usual.

After that the VXMM.386 has to be installed. Change to the X15 demo path and run SETUP.
The window below pops up. Answer the question to change system.ini with “Y”. Press “ENTER” and restart the system.



Now the X15 demo hardware and software should be installed correctly.
To check this item, change to the X15 demo directory and run “X15.EXE”.

Phase-out/Discontinued

Now this window should pop up:

```
- cmdlin32
Datei  Bearbeiten  ?
*********************************************
*            COMMAND INTERPRETER            *
* (c) 1995-1999 TU Chemnitz, DaKo, Heynig   *
*********************************************
Register command group 'DIALOG'.
Register command group 'PCI'.
Register command group 'DRIVER'.
Register command group 'X15'.
Register command group 'X15add'.
0 X15 > find 0 /o
S20 device 7 is open. Device 7 selected. Open X15.
Reset P0 P1 P2 P3 X15
Plugin NEC Software...
*********************************************
*    Monitoring Software for NEASCOT-X15    *
*  Copyright (c) 1998-1999  NEC Corporation *
*********************************************
1 X15 > driver.copen 0 50 $x15dev
1 X15 = driver.copen 0 50 H:7
Channel 71 at device 7 is open.
2 X15 > driver.receive 1
Display received packets is ON.
3 X15 > driver.send $channel 100 5
3 X15 = driver.send H:71 100 5
Send 5 x 100 bytes on channel 71
Time: 8 ms
Packet received @ channel 71 (han=00000007, ptr=8002301C, size=100)
'!"#$%&'()*+,-./0123456789:;<=>?@ABCDEFGHIJKLMNOPQRSTUVWXYZ[\'
Packet received @ channel 71 (han=00000007, ptr=8002441C, size=100)
'"#$%&'()*+,-./0123456789:;<=>?@ABCDEFGHIJKLMNOPQRSTUVWXYZ[\]'
Packet received @ channel 71 (han=00000007, ptr=8002581C, size=100)
'#$%&'()*+,-./0123456789:;<=>?@ABCDEFGHIJKLMNOPQRSTUVWXYZ[\]^'
Packet received @ channel 71 (han=00000007, ptr=80026C1C, size=100)
'$%&'()*+,-./0123456789:;<=>?@ABCDEFGHIJKLMNOPQRSTUVWXYZ[\]^_'
Packet received @ channel 71 (han=00000007, ptr=8002841C, size=100)
'%&'()*+,-./0123456789:;<=>?@ABCDEFGHIJKLMNOPQRSTUVWXYZ[\]^_`'
Rate: 0.504 Mbit/s
4 X15 > _
```

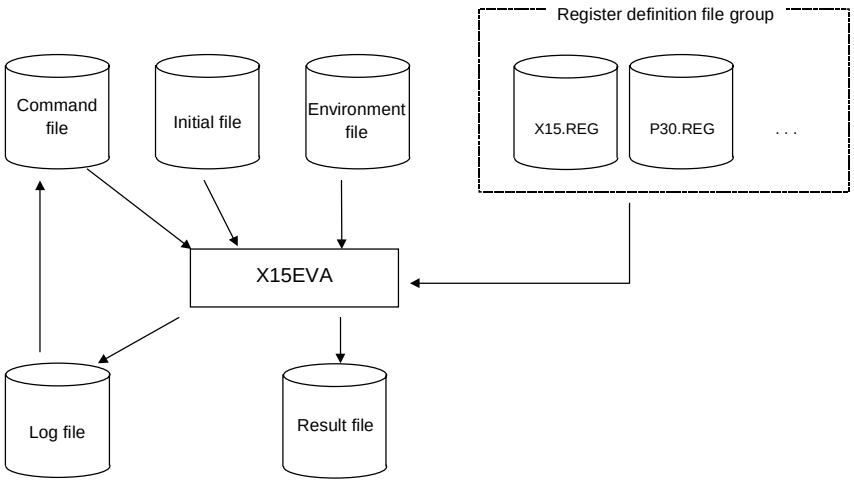
If this window appears the system is working properly.

Phase-out/Discontinued

CHAPTER 8 FILE CONFIGURATION

8.1 File Configuration

The file configuration of this program is shown below.



File name	I/O	Explanation
Command file	I	File from which commands are input
Log file	O	File to which command input history is stored in interactive mode
Environment file (X15EVA.ENV)	I	File used to specify register definition file name. Also, specifies the types of PHY that are connected to each UTOPIA port of μPD98412.
Result file	O	File to which the results of command execution are output.
Register definition file group	I	File used to define the names of those registers used by each LSI.
Initial file	I	File to specify commands that are executed when this monitor is activated.

Remark In this version, the environment file (X15EVA.ENV) must exist in current directory.

Phase-out/Discontinued

8.2 Environment File

This section describes the format of the environment file (**X15EVA.ENV**).

Command specification

Commands to specify register definition file name

Format: c*hip_name access_size file_name*

Function: Specify a default access size and a name of register definition file for each *chip_name*.

- *chip_name*

  Following values can be specified.

  X15, **T20**, **P15**, **P30**, **X10** (for compatibility with the X10EVA)

- *access_size*

  Default access size when accessing each chip. When using commands without **-1**,**-2** or **-4** option, this value is used.

- *file_name*

  Specify the name of file to define registers name of each *chip_name*.

Commands to specify bit field definition file

Format: **X15_BIT** *file_name*

Function: Specify the file name to define bit field names.

Commands to specify PHY type

Format: *phy_no chip_name*

Function: Specify the PHY module's type that is connected to each UTOPIA port.

- *phy_no*

  Specify value according to the following format.

  Phy*x.y* ...x: UTOPIA interface number (0 - 3)

  y: PHY device number (0 - 1).

- *chip_name*

  Specify the PHY module type which is connected to each *phy_no*. Following values can be specified.

  T20 ... T20 PHY module

  P15 ... P15 PHY module

  P30 ... P30 PHY module

Phase-out/Discontinued

Commands to specify the default base address

Format : **PBASE_ADR** *base_address*

Function: Specify the default base address for **PINIT** command. When **PINIT** command is input without base address option, base address specified here is assumed by default.

Commands to specify the initial configuration file

Format : **INIFILE** *file_name*

Function: Specify the initial configuration setup file name. Commands specified in this file are executed when this monitor program is activated. The format of this file is same as the file that is specified as the **IFILE** command argument.

Examples

The sample environment file is shown below. Lines beginning with '#' are regarded as comment line.

```
#
#  Specify the register definition file
#
X15  4  C:\INST_DIR\X15.REG
T20  1  C:\INST_DIR\T20.REG
P15  1  C:\INST_DIR\P15.REG
P30  1  C:\INST_DIR\P30.REG
#
#  Specify initial configuration setup file
#
INIFILE  C:\INST_DIR\X15EVA.CFG
#
#  Specify the bit field definition file
#
X15_BIT C:\INST_DIR\X15_BIT.REG
#
#  Define PORT assign
#
Phy00  T20
Phy10  P15
Phy20  P30
Phy21  P30
Phy30  T20
#
#  Define base address for PINIT command
#
PBASE_ADR  0xe000000
```

Phase-out/Discontinued

[MEMO]

Phase-out/Discontinued

CHAPTER 9 COMMAND

9.1 Overview

9.1.1 Activation

Either of the following commands is entered from the DOS prompt, in the format described below.

(1) X15EVA

After activation of the program, the command input prompt is displayed (interactive mode). As they are input, commands are automatically saved into a log file so that, when processing is subsequently repeated, the file can be used as a command file.

* The log file is named X15_LOG.xxx (where xxx = 000 - 999). The program obtains the value of xxx by incrementing the largest value it finds in the current directory.

(2) X15EVA command

The command specified as an argument is executed, after which the program terminates (command line mode). In this case, no prompt is displayed and commands are not written to a log file as they are input.

9.1.2 Termination

In interactive mode, the program can be terminated by entering "**Q(UIT)**", either from the command input prompt or from within the command file.

In command line mode, the program is terminated automatically after executing the specified command, whichever the **QUIT** command is specified or not in command file.

Phase-out/Discontinued

9.2 Commands

9.2.1 Overview

The commands that can be specified with this program are listed below.

Function		Command name
File I/O commands		
	1. Specify a output result file name	OFILE
	2. Input commands from the specified file	IFILE
Read group commands		
	1. Memory dump	DUMP
	2. Register/memory read	READ
	3. Value comparison	COMP
Write commands		
	1. Register/memory write	WRITE
	2. Memory batched write (fill)	FILL
Others		
	1. Reset	RESET
	2. Terminate	Q, QUIT
	3. Help	?, HELP
	4. PCI initialization	PINIT
	5. PCI status acquisition	PSTAT
	6. Display all PCI configuration registers	PCONF
	7. Execute following commands while the specified condition is true	WHILE
	8. Display information to indicate while the device caused interrupt or not..	INTCHK
	9. Open channel of S20	COPEN
	10. Close channel of S20	CCLOSE
	11. Send data through S20	SEND

9.2.2 Command Priority

Basically, specification of the register **READ** command is assumed by default. That is to say, when commands are input, they are retrieved in the order shown below.

(1) The system determines whether an input command matches those shown in the list in Section 2.1
When a match is found, the command is executed. When the input command does not match any of those in the list, processing proceeds to step 2)

(2) The system determines whether the input command matches the register name of μPD98412.
When a match is found, **READ** command is performed and the contents of the register are displayed.

Phase-out/Discontinued

9.3 Command Declaration

Command arguments as shown Chapter 4 are declared as shown below.

Note that this program does not differentiate between uppercase and lowercase for input commands and command arguments.

9.3.1 Basic Rule of Declaration

In this manual, a command name is described using uppercase bold characters and command options are described using lowercase.

Note that command options are described using following notations.

Declaration	Description
[xxx]	xxx is the option that can be omitted
< xxx | yyy >	Either xxx or yyy must be specified

9.3.2 Address Declaration

[*Target*:]< *address* | *register-name* | *system variable-name* >

- *Target*

  The target to be accessed is specified. Any of the following can be specified. X15, specified previously, is assumed as the default.

  X15 ... Specifies R/W to/from the I/O register of μPD98412.
  Px.y ... Specifies R/W to/from the I/O register for PHY.
  X: UTOPIA interface number (0 - 3)
  y: PHY channel e.g. 0 to 3 for a P40
  HT ... Specifies R/W to/from HTT memory
  CB ... Specifies R/W to/from CB memory
  ALL ... All space in memory map
  SYS ... Specifies system variable name (For detail, see below).
  X10 ... This option is identical with specifying “X15”. (compatibility with the X10EVA)

  Remark About details of memory map, see **9.5.1 Memory Map**.

- *Address*

  the address is specified using any of the following notations.

  1. Hexadecimal
     specified as a number either starting with ‘0x’ or ending with ‘h’.
  2. Decimal
     Specified with 0 - 9.
  3. Binary
     specified as a number either starting with ‘0b’ or ending with ‘b’.

- *register-name*

  The address is set according to the register name. To use this notation, environment files are specified correctly. About environment files, See **8.2 Environment File**.

- *system variable-name*

Phase-out/Discontinued

Following internal variable-name can be specified.

I,J,K … Mainly, these variables are used for a loop counter of WHILE command. For example, when executing commands five times recursively, following notation can be used.

(Example)

```
WHILE SYS:I!=5
    (COMMANDS)
WEND
```

(Example)

- X15:0x0000
  Address 0x0000 of X15
- OQminCRV
  OQminCRV register of X15
- P00:CMR
  CMR register of PHY module (UTOPIA 0, PHY 0)

Phase-out/Discontinued

9.3.3 Address Range Specification

[*Target*:] *address-address*

- *Target*

  Same as in **9.3.2 Address Declaration.**

- *Address-address*

  The address range is specified using the notations described in **9.3.1 Basic Rule of Declaration.**

9.3.4 Value Specification

[=*Value*]

The *value* is specified using any of the following notations. With both hexadecimal and binary notation, "_" can be used as a delimiter.

1. Hexadecimal

   specified as a number either starting with ‘0x’ or ending with ‘h’.

2. Decimal

   Specified with 0 - 9.

3. Binary

   specified as a number either starting with ‘0b’ or ending with ‘b’.

Phase-out/Discontinued

9.4 Command Details

9.4.1 File I/O Commands

(1) OFILE Command

Format : **OFILE** [-n] [*filename*]

Function : The output results for the following commands are output to the file specified with *filename*. Provided the output destination remains unchanged, this command can be used as many times as necessary. Note that even after the specification of this command, results are output to the standard output (display). When the “-n” option is specified, however, results are output to a file only, not to the standard output. Also, omitting the specification of *filename* indicates that file output is to be terminated.

Remark It is not possible to specify this command as an argument of command line mode.

(2) IFILE Command

Format : **IFILE** *filename*

Function : The following commands are input from the file specified with *filename*. If execution of this command is terminated from within a file, the prompt is redisplayed. At this time, comments indicating the start and termination of the **IFILE** command are written into the log file, together with the history of the commands actually executed in the input file.

Remark This command can be nested up to 8 times.

Phase-out/Discontinued

9.4.2 Read Group Commands

(1) DUMP Command

Format : **DUMP** [*target:*] *address-address* [-n] [-b *filename*]

Function : The dump results for the memory areas of the specified target are output. The result is output in the following 16-bytes/line format.

Option:

-b: The results of reading are output, in binary format, to the file specified with this option.

-n: Not output to the standard output.

Example) DUMP **X15**:0x0000-0x001f

```
address    00 01 02 03  04 05 06 07  -  08 09 0a 0b   0c 0d 0e 0f
0x0000     00 00 00 00  00 00 00 00  -  00 00 00 00   00 00 00 00
0x0010     00 ff 00 00 ......
```

(2) READ Command

Format: **READ** [-d][*target:*]< *address* | *register* | *system variable* > [< -1 | -2 | -4 >]

Function: The contents of memory of the specified target, or the values of register, are output. Moreover, if the specified register has names per each bit fields, all bit field names and values are also displayed (see example 2).
Also, the register name can be specified either in regular format or left-truncated (see example 3).

Option:

-d: The results of reading are displayed as a decimal value.

-1: One byte memory access is performed.

-2: Two bytes memory access is performed.

-4: Four bytes memory access is performed.

Remark When access unit (-1,-2,-4) option is omitted, following values are assumed as default. (These default values can be defined in the Environment file.)

- When the address is specified directly.
  X15, HT, CB, ALL ... 4 Byte
  Px.y ... 1 Byte
- When the register name is specified.
  Register size

This restriction is also applied to other commands that can obtain this access unit option.

Example 1) READ X15:0x0000 -4
-> 0x0000 = 0x00000200

Example 2) READ X15:CMD
-> CMD = 0x2007
REV = 0x20
CMD = 0x07

Example 3) READ X15:MQ*
-> MQminCRV = 0x0000
MQminRNV = 0x0000
MQminABR = 0x0000

Phase-out/Discontinued

MQminUBR = 0x0000
MQthCRV = 0x0000
MQthRNV = 0x0000
MQthABR = 0x0000
MQthUBR = 0x0000

(3) COMP Command

Format: **COMP** [*target:*]< *address*|r*egister* >=*value* [< -1|-2|-4>]
or [*target:*] *address* -b *filename*

Function: The value of the specified target is read, then compared with the specified value. When the values match, the message "compare complete" is output.
When the values do not match, the results of reading are displayed.

Options:

-1: One byte access is performed.
-2: Two bytes access is performed.
-4: Four bytes access is performed.
-b *filename*:
When a filename is specified, values are compared with expected values in this file. Address range is due to the specified file byte size. The format of this file must be a binary type format.

Example 1) X15EVA COMP X15:CMD = 0x2000
-> compare complete!!

Example 2) X15EVA COMP X15:0x0000 -b X15.dmp

->	address	source(mem)	dest(comp)
	0x0000	0x00	0x20
	0x000f	0x00	0x07

compare end!

Phase-out/Discontinued

9.4.3 Write Group Commands

(1) WRITE Command

Format: **WRITE** [*target:*]< *address* | *register* | *system variable*><=*value* | *its_name=value*> [<-1|-2|-4>]

Function: The specified value is written either into memory of the specified target, or into the register. Moreover, if the specified register has a different field name in the bit field, specification can also be made with *bits_name*=*value*. In this case, when the entire bit field has not yet been set, only that bit value is set (read modify write).

Options:

-1: One byte memory access is performed.

-2: Two bytes memory access is performed.

-4: Four bytes memory access is performed.

Example 1) WRITE X15:MQminABR=0x0000

-> Value 0x0000 is set in register MQminABR.

Example 2) WRITE X15:HT0.NVPC=7 NVCI=8 BASE=0x0000

-> The settings of those bits for which no new value is specified remain as is.

Remark In some registers (such as STATUS register of μPD98412), to write 1 is performed as clearing of value. In this case, “read-modify-write” procedure is not performed correctly. So it is not possible to specify bit fields name as target address.

(2) FILL Command

Format: **FILL** [*target:*]*address-address* [-v *value]* [-i *increment*][-w *width*]

or [target:]address -b filename

Function: Sets the specified value in memory of the specified target.

Options:

-v: The specified value is set. When no value is specified, 0x00 is assumed. A value in the range of 0x0000 to 0xffff can be specified.

-i: The value specified in “-v” is incremented by the value specified in this option. When this option is omitted, 0x00 is assumed. A value in the range of 0x0000 to 0xffff can be specified. When incremented value exceeds the maximum value (0xffff), the value returns to 0x00.

-w: Address range is partitioned by this specified byte length. 1, 2, and 4 are suitable for this option. The value specified in “–v” is incremented by the value specified in “-i” per this partitioned address. When no value is specified as *width*, the length of *value* is assumed.

-b: The contents of the specified binary file are written into memory, starting from the specified address. The amount of data written into memory is the same as the file size. Note that this option cannot be specified together with any of the other options.

Phase-out/Discontinued

Example 1) FILL X15:0x0000-0x000f,-v0x00,-i0x01,-w2

->

Address	Stored Value
0x0000	0x00
0x0002	0x01
0x0004	0x02
0x0006	0x03
.	.
.	.
.	.

9.4.4 Other Commands

(1) RESET Command

Format: **RESET** [*targets...]*

Function: Issues the RESET command for μPD98412 and PHY.
[targets]: P30 or P40 or T20 pr X15

(2) QUIT Command

Format: < **Q** | **QUIT** >

Function: Terminates processing

(3) HELP Command

Format: < **?** | **HELP** >

Function: Synopses of all command are displayed. Synopses are displayed only on the screen, and not output to the file specified in **OFILE** command.

(4) PINIT Command (For compatibility with X10 software only)

Format: **PINIT** [*base_address*]

Function: Set the base address for mapping memory of X15 ATM switch demo-board to system memory space. When *base_address* is omitted, the default value defined in the Environment file is used.
This command also sets interrupt handler. When a H/W interrupt occurs, this program executes following procedures.

(1) Reads “STATUS” register and saves this value internally. When INTCHK command is specified, this STATUS value is displayed.
(2) Changes “INTMASK” register’s value to stop the device from interrupting.

Remark When this monitor is activated, the PCI bus interface is not initialized automatically. So **PINIT** command must be specified at first.

Phase-out/Discontinued

(5) PSTAT Command

Format: **PSTAT**

Function: The status register of PCI configuration is displayed.
The status is displayed in hexadecimal format as shown below.

0x0000: O.K.
0x00f0: fast back-to-back enable.
0x0100: data parity error detected.
0x0200: DEVSEL# timing.
0x0400: DEVSEL# timing.
0x0800: target abort issued.
0x1000: target abort received.
0x2000: master abort received.
0x4000: system error issued.
0x8000: parity error detected.

(6) PCONF Command

Format: **PCONF**

Function: All configuration registers of PCI are displayed in hexadecimal format.

(7) WHILE command

Format: **WHILE** [target:]< *address* | *register* **| *system variable***> < == | != > *value*
< -1 | -2 | -4 > [-t *time*]
command lines
WEND

Function: Execute command lines specified between WHILE and WEND line while the specified condition is true. When the condition is false, exit while loop and execute next commands.

Options:

==: While the value of specified register is equal to the specified *value*, execute *command lines*.

!=: While the value of specified register is not equal to the specified *value*, execute *command lines*.

-t: Limit time to avoid endless recursion. When spent time exceed this limit time, a message is displayed and execute command lines which are described next to the **WEND** line.
Specifying 0 as this limit time or omitting this option is assumed as endless recursion

Remark This command can be nested up to 8 times.

- This command is only available in a command file. When enter this command from command prompt, a error message is displayed.

Phase-out/Discontinued

(8) INTCHK Command

Format: **INTCHK** [-c]

Function: If interruption occurred, value of “STAUTS” register when interruption occurred is displayed.

-c: Remain STATUS value retained in this program. When this option is omitted, Clear internal information of this program.

Remark This program supports only interrupt from μPD98412, so recommend to set interrupt mask register of PHY device to disable interrupts. When interrupts from other devices occur, interrupt handler executes following procedures.

- Interrupt from PHY devices
  Sends a command to PIC(Programmable Interrupt Controller) of PC for disabling interrupts.
- Interrupt from any other PCI devices that share interrupt line with μPD98412.
  Interrupt handler executes nothing and jumps the other interrupt handler that is registered previously by other device driver.

(9) COPEN Command

Format: **copen** <vpi> <vci> [<device>] [/t /r /0 /a /c /v]

Function: To use S20 as traffic generator. This command specifies ATM traffic for output to the S20/P30 devices on the X15 ATM switch demo-board.

<vpi>: unsigned decimal value of the VPI
<vci>: unsigned decimal value of the VCI
<device>: unsigned hexadecimal value of device number

Remark Normally device number is unknown.

/t:	transmit only
/r:	receive only
/0:	AAL0
/a:	ABR
/c:	CBR
/v:	VBR

(10) CCLOSE Command

Format: **CCLOSE** <channel>

Function: Closes the open channel that was established with COPEN.

<channel>: Channel number of the COPEN command

(11) SEND Command

Format: **SEND** [<channel> [<size> [<number>]]

Function: Send data of a certain channel with the specified size. Number describe how many packets should be sent.

<channel>: unsigned hexadecimal value of the channel
<size>: unsigned decimal value of the frame size
<number>: unsigned decimal value of repeated frames

Phase-out/Discontinued

9.5 Memory Map and Address Description

The S20 on the X15 ATM switch demo-board has an external Framer because only in this configuration the S20 Management-Interface for controlling external PHY-Devices becomes available. This PHY-Management Interface of S20 has a 19-Bit wide Address Range. The Address Range was divided in multiple Areas with the help of an extra PLD device (Lattice ispLSI2128V), in order to accommodate all the following Management Interfaces of the X15 ATM switch demo-board:

- 4 UTOPIA-Management Interface
- X15-Management Interface
- Management Interface of the external P30 PHY-Controller connected to S20

The Address-Mapping is done as shown in the Table bellow:

9.5.1 Memory Map

Address Range	Access	Description
0x000 ... 0x1ff	R/W	UTOPIA Interface 0 Read and Write Access
0x200 ... 0x3ff	R/W	UTOPIA Interface 1 Read and Write Access
0x400 ... 0x5ff	R/W	UTOPIA Interface 2 Read and Write Access
0x600 ... 0x7ff	R/W	UTOPIA Interface 3 Read and Write Access
0x800	R/W	X15 Address for X15 I/O Access and Auto I/O Read
0x802	R/W	X15 Address for X15 MEM Access and Auto MEM Read
0xA00	W	X15 32 Bit Data Access for X15 I/O Write
0xA01	W	X15 16 Bit Data Access for X15 I/O Write
0xA02	W	X15 32 Bit Data Access for X15 MEM Write
0xA03	W	X15 16 Bit Data Access for X15 MEM Write
0xC00 ... 0xC7F	R/W	Ext. PHY P30 Read and Write Access
0xE00	R	Lattice Interrupt Indication Register
0xE00	W	Lattice Interrupt Indication Read Mask Register
0xE01	W	Lattice Reset Register
0xE02	R	Lattice X15 or UTOPIA Read Error Indication Register
0xE02	W	Lattice Management State Machine Reset
0xE03	R	Lattice Revision, Actual Rev. 5

In addition to the X15 ATM switch demo-board's Management Interfaces the Control Registers of the Lattice glue-logic are also mapped within the Address Range. Their function is described in detail in the following paragraphs.

Phase-out/Discontinued

9.5.2 Access to the UTOPIA-Management Interfaces

Access to the Management Interfaces is made (as shown in the Table above) through the PHY-Management Address Range **0x000 ... 0x7ff** of S20. When the Host-system makes an access to this area, the glue-logic implemented in the Lattice relays this access to the selected UTOPIA-Interface.

The Host accesses S20's PHY-Management Address Range through an Indirect_Access_Command to S20. For example, to read the physical Address 0x10 of UTOPIA Interface 2, the Host has to configure the S20's CMR Register as follows:

Bit R/W = **1**	(Read Access)
B3-B0 = **XXXX**	(Byte enable, Don't care)
TGT = **10**	(Target = External PHY Layer Device)
ADDRESS = **0x410**	(UTOPIA 2 Base = 0x400 + Offset 0x10)

Finally, the Host starts access to the selected target as an Indirect_Access_Command to S20. S20 reads from Address 0x410 and stores the value in his CER Register (See S20 User's Manual).

Write access to the UTOPIA-Interfaces is made analogous to Read access through an Indirect_Access_Command to the target "External PHY layer device".

9.5.3 Access to X15-Management Interfaces

X15 has 2 Management Interfaces, the first one for Register Access (I/O) and the second one for accessing the HTT- respectively Cell-Memory. Accessing the X15 internal Registers is done after this schema:

To read an X15-Register the Host must write the 32-Bit Address of the register to be read at the Address 0x800 of the target "External PHY layer device" through an Indirect_Access_Command. This access is recognized by the Lattice glue-logic, which latches the 32-Bit Address value. Afterwards a Lattice internal state machine starts automatically a X15 I/O Read access to the latched Register Address. The 32-Bit value, which is being read out, is also latched. The host must now execute an Indirect_Access_Command to the "External PHY layer device" target's Address 0x800 in order to read this value. Thus the X15-Register value from Latch is read out by S20 and placed in his CER Register, and made accessible for the Host.

A Read Access to the X15 HTT- and Cell-Memory is done analogous to the X15 I/O-Read Access with the only difference that the Indirect_Access_Command has to be made at the Address 0x802.

Write Accesses to X15 can be 16- or 32-Bit wide and differ from each other. A 32-Bit Write Access to a X15 register is made as follows:

First of all, the Host makes a Write access with the ADDRESS of the X15 register as a value with the help of an Indirect_Access_Command to Address 0x800 and saves (as in Read access) the value in the 32-Bit Latch (in Lattice). After that, the Host writes the actual 32-Bit wide register VALUE through an Indirect_Access_Command to Address 0xA00, which operation triggers a state machine in Lattice PLD. The state machine runs a 32-Bit Write access to the register Address, saved in the Latch.

A 16-Bit Write Access to a X15 register is made similar to the 32-Bit Write. But In this case, the Host makes a Write access with the actual 16-Bit wide register VALUE of the X15 register with the help of an Indirect_Access_Command to Address 0xA01.

Writing of 32- or 16-Bit Values to the X15 HTT- and Cell-Memory is just like writing to X15 registers. The Host has to put the memory ADDRESS with an Indirect_Access_Command (Write) to the Address 0x802 into the 32-Bit Latch. Afterwards the desired memory VALUE is stored with another Indirect_Access_Command (Write) to the Address 0xA02 (32-Bit write) or to the Address 0xA03 (16-Bit write). The Write access to the X15 Memory area is done by a state machine in Lattice, as soon as S20 gets the Host's Indirect_Access_Command (Write) to Addresses 0xA02 or 0xA03 respectively.

Phase-out/Discontinued

9.5.4 Access to the Management Interface of the External P30 Attached to S20

The registers of the external P30, connected to S20, can be written or read out through an Indirect_Access_Command in the Address Range 0xC00…0xC7F. For example, the Host must make an Indirect_Access_Command (Read) to Address 0xC10 to read P30's Register 0x10.

9.5.5 Lattice Control Register

The glue-logic, providing the Management Interfaces, implemented in Lattice has several Control registers, described bellow.

- **Lattice Interrupt Indication Register IIR**

  Address: 0xE00

  Access Mode: R

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
-	-	PINT	XINT	MINT3	MINT2	MINT1	MINT0

Field	Function	Value after Reset
PINT	Indicates Interrupt from external P30: 0 – No interrupt from P30 1 – Interrupt request from P30	0
XINT	Indicates Interrupt from X15: 0 – No interrupt from X15 1 – Interrupt request from X15	0
MINT3	Indicates Interrupt from UTOPIA Interface 3: 0 – No interrupt from UTOPIA 3 1 – Interrupt request from UTOPIA 3	0
MINT2	Indicates Interrupt from UTOPIA Interface 2: 0 – No interrupt from UTOPIA 2 1 – Interrupt request from UTOPIA 2	0
MINT1	Indicates Interrupt from UTOPIA Interface 1: 0 – No interrupt from UTOPIA 1 1 – Interrupt request from UTOPIA 1	0
MINT0	Indicates Interrupt from UTOPIA Interface 0: 0 – No interrupt from UTOPIA 0 1 – Interrupt request from UTOPIA 0	0

There are 6 Interrupt sources on the X15 ATM switch demo-board:

- 4 Interrupt lines to the UTOPIA-Management Interfaces
- 1 Interrupt line to X15
- 1 Interrupt line to P30

These Interrupt lines are merged in Lattice to one Interrupt Request and directed to S20 as an External PHY Layer Interrupt. The IIR Register indicates which Interrupt source has set a PHY-Interrupt to S20. This is a read-only register and only Bits, for which the corresponding Mask-Bits in IRMR-register were previously set to "1", can be read out. During register read, all Bits, for which the IRMR-register mask was set, are automatically reset to "0". If the mask in IRMR-register is set for all Bits, before IIR-register is read, then the first read of IIR-register deactivates the PHY-Interrupt signal to S20. Nevertheless, if an Interrupt source is still active, the corresponding Bit in IIR-register is automatically set again to "1"and S20 gets another PHY-Interrupt.

Phase-out/Discontinued

- **Lattice Interrupt Indication Read Mask Register IRMR**

  Address: 0xE00

  Access Mode: W

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
-	-	IRMR5	IRMR4	IRMR3	IRMR2	IRMR1	IRMR0

Field	Function	Value after Reset
IRMR5	Mask Interrupt Indication for IIR.PINT: 0 – masks out a PINT interrupt indication on IIR-Read access, a read access to IIR does not clear a active interrupt indication on Bit PINT in register IIR 1 – enables the interrupt indication read access to IIR Bit PINT, a read access to IIR clears a active interrupt indication on Bit PINT in register IIR	0
IRMR4	Mask Interrupt Indication for IIR.XINT: 0 – masks out a XINT interrupt indication on IIR-Read access, a read access to IIR does not clear a active interrupt indication on Bit XINT in register IIR 1 – enables the interrupt indication read access to IIR Bit XINT, a read access to IIR clears a active interrupt indication on Bit XINT in register IIR	0
IRMR3	Mask Interrupt Indication for IIR. MINT3: 0 – masks out a MINT3 interrupt indication on IIR-Read access, a read access to IIR does not clear a active interrupt indication on Bit MINT3 in register IIR 1 – enables the interrupt indication read access to IIR Bit MINT3, a read access to IIR clears a active interrupt indication on Bit MINT3 in register IIR	0
IRMR2	Mask Interrupt Indication for IIR. MINT2: 0 – masks out a MINT2 interrupt indication on IIR-Read access, a read access to IIR does not clear a active interrupt indication on Bit MINT2 in register IIR 1 – enables the interrupt indication read access to IIR Bit INT2, a read access to IIR clears a active interrupt indication on Bit MINT2 in register IIR	0
IRMR1	Mask Interrupt Indication for IIR. MINT1: 0 – masks out a MINT1 interrupt indication on IIR-Read access, a read access to IIR does not clear a active interrupt indication on Bit MINT1 in register IIR 1 – enables the interrupt indication read access to IIR Bit MINT1, a read access to IIR clears a active interrupt indication on Bit MINT1 in register IIR	0
IRMR0	Mask Interrupt Indication for IIR.MINT0: 0 – masks out a MINT0 interrupt indication on IIR-Read access, a read access to IIR does not clear a active interrupt indication on Bit MINT0 in register IIR 1 – enables the interrupt indication read access to IIR Bit MINT0, a read access to IIR clears a active interrupt indication on Bit MINT0 in register IIR	0

Phase-out/Discontinued

Register IRMR masks Interrupt Indications during reads of IIR-Register. The IRMR register is a write-only type. Setting Bits to “1” allows read and therefore reset of the corresponding Interrupt Indication in IIR. Resetting to “0” prohibits deliberately deletion of the corresponding Interrupt Indication on reading of IIR-register. This mechanism allows Interrupt service routines to detect and reset each specific Interrupt source.

- **Lattice Reset Register RR**

  Address: 0xE01

  Access Mode: W

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
-	-	RR5	RR4	RR3	RR2	RR1	RR0

Field	Function	Value after Reset
RR5	Enable / Disable External PHY Reset Input: 0 – disable external PHY Reset Input 1 – enable external PHY Reset Input	0
RR4	Enable / Disable X15 Reset Input: 0 – disable X15 Reset Input 1 – enable X15 Reset Input	0
RR3	Enable / Disable UTOPIA IF 3 Reset Output: 0 – disable UTOPIA IF 3 Reset Output 1 – enable UTOPIA IF 3 Reset Output	0
RR2	Enable / Disable UTOPIA IF 2 Reset Output: 0 – disable UTOPIA IF 2 Reset Output 1 – enable UTOPIA IF 2 Reset Output	0
RR1	Enable / Disable UTOPIA IF 1 Reset Output: 0 – disable UTOPIA IF 1 Reset Output 1 – enable UTOPIA IF 1 Reset Output	0
RR0	Enable / Disable UTOPIA IF 0 Reset Output: 0 – disable UTOPIA IF 0 Reset Output 1 – enable UTOPIA IF 0 Reset Output	0

The RR Register allows resetting separate Circuits of X15 ATM switch demo-board as desired.

By setting to “1” the corresponding Reset-Line is durably activated. By setting to “0” the corresponding Reset-Line is permanently deactivated.

- **Lattice X15 or UTOPIA Read Error Indication Register**

  Address: 0xE02

  Access Mode: R

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
-	-	-	-	-	X15MRD	X15IORD	RDERR

This register is for test purposes only. On access various Error messages of the in Lattice implemented Read State machine are read out.

Phase-out/Discontinued

- **Lattice Management State Machine Reset**
  Address: 0xE02
  Access Mode: W

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
-	-	-	-	-	-	-	-

This register is for test purposes only. Any write access with arbitrary value resets the State machine implemented in Lattice.

- **Lattice Revision Register**
  Address: 0xE03
  Access Mode: R

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0	0	0	0	0	1	0	1

This register contains the actual Version number of the Lattice's glue-logic and is read-only. The current Lattice-Version is 5.

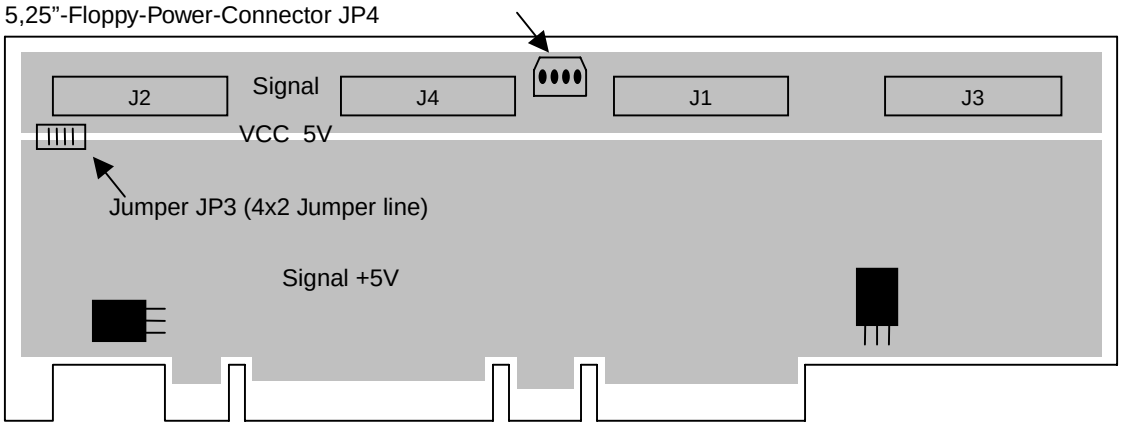
Phase-out/Discontinued

9.6 Jumper Settings

The X15 ATM switch demo-board has 3 Jumper lines for configuring Power supply and 2 Jumpers for selection of UTOPIA Clock Signals.

Jumper line JP3 allows to connect the X15 5V power supply (5V from PCI-Connector) to the 5V power supply of the 4 UTOPIA-Interfaces. When JP3 is closed (set), the UTOPIA-Interfaces get their 5V power supply from the 5V Plane of X15 ATM switch demo-board, which is powered itself by the PCI-Connector. In this case it is **forgotten to plug-in** the external power supply to the 5,25“-Floppy-Power-Connector JP4.

Jumper line JP6 allows the connection of the 3.3V power plane and the X15 ATM switch demo-board VCC-power plane. If the PCI-Hostsystem provides 3.3V on the PCI-Connector (not the case nowadays) then this power is railed to the 3.3V power plane of X15. In such case, shorting (setting) JP6 will allow to supply 3.3V from PCI-Connector directly to the X15 ATM switch demo-board’s VCC plane. This also means, that the linear regulator U29 must not be soldered! If no 3.3V are available on the PCI-Connector, then U29 generates 3.3V power supply for the X15 ATM switch demo-board’s VCC plane from tne 5V PCI-Connectors power. Then it is a must to leave JP6 open!



Jumper line JP7 allows the connection of the VCC plane (3.3V power from U29 or PCI-Connector) and the VCC_X15 power plane of X15 ATM switch demo-board. VCC_X15 powers X15 (U3) and its external memory devices (U12…U20) with 3.3V. Closing JP7 provides 3.3V power from the VCC plane to the VCC_X15 plane. In this case do not solder (place on board) the linear regulator U35.

Otherwise U35 provides 3.3V to the VCC_X15 power plane from the PCI-Connector’s 5V power, Then leave JP7 open!

Phase-out/Discontinued

Jumpers JP1 and JP2 make possible to select the which UTOPIA-Clock signals are used.
In the Table bellow the meaning of the Jumper settings for JP1 and JP2 are shown:

Text	Pin1	Pin2	Pin3	Meaning
Jumper JP1				
Common	closed			Clock signals of UTOPIA-Interfaces 0 and 2 are generated in Oscillator U4.
Separate		closed		Clock signals of UTOPIA-Interfaces 0 are generated in Oscillator U4. Clock signals of UTOPIA-Interfaces 2 are generated in Oscillator U5.
Jumper JP2				
Common	closed			Clock signals of UTOPIA-Interfaces 1 and 3 are generated in Oscillator U7.
Separate		closed		Clock signals of UTOPIA-Interfaces 1 are generated in Oscillator U7. Clock signals of UTOPIA-Interfaces 3 are generated in Oscillator U8.

Phase-out/Discontinued

9.7 Sample Procedure

A sample usage of this monitor is shown below.

(Step1) Edit an input file.

Prepare an input file such as shown below before activating this monitoring software. Here, the name of input file is “sample.dat”. Note that the **PINIT** and **RESET** commands must be specified before accessing μPD98412.

```
ofile sample.out
pinit 0xe000000
reset
write X15:0x040=0x30
read X15:0x040
  .
  .
```

“sample.dat”

(Step2) Activate the monitor

Enter **X15EVA** command from DOS prompt for activating this monitor, and enter **IFILE** command from the prompt of this monitor.

```
C:\> X15EVA
  .  ( Some messages and Copyright are displayed)
  .
command: ifile sample.dat
```

(Step3) Confirm the result

If **OFILE** command is specified in the input file, command results are output to the specified file. In this sample case, “sample.out” is specified, in sample.dat, as output file name.

```
# pinit 0xe000000
# reset
# write X15:0x040=0x30
# read X15:0x040
  0x00000040 = 0x00000030
  .
  .
  .
```

“ sample.out”

Phase-out/Discontinued

[MEMO]

Phase-out/Discontinued

CHAPTER 10 SAMPLE APPLICATION CONFIGURATION SOFTWARE (X15EVA.dat)

```
#
# Initial configuration file for monitoring software of NEASCOT-X15
#
#    X15 Revision    : Rev2.0
#
#
// Setup a daisy-chain for Test of:
// P40 at UTOPIA 1 and 3 (16bit)
// P30 at UTOPIA 0
// T20 at UTOPIA 2
// S20 -> P40 Port 0 -> P40 Port 1 -> P30 -> T20 Port 5 -> T20 Port 6 -> P40 Port 0
// Connect S20 with P40 Port 0, P40 Port 1 with P30, T20 with loop back RJ45 jacks
// VPI: 0 , VCI=50d for all connections
// X15 Logical Port Setup:
// Port0 -> Port1 -> Port7 -> Port5 -> Port6 -> Port0


// Begin with Initialization X15
// reset
// Switch off X15 working
write X15:CMD.CMD=0x0

// Set X15 Mode1 Register: HTT and Cell Buffer Memory Size is 256k, Memory Access goes to HTT
write X15:MODE1=0x0122

// X15 Queue Configurations
write X15:OQminCRV=0x080
write X15:OQminRNV=0x080
write X15:OQminABR=0x080
write X15:OQminUBR=0x080
write X15:TCminCRV=0x100
write X15:TCminRNV=0x100
write X15:TCminABR=0x100
write X15:TCminUBR=0x100
write X15:OQthCBR=0x0100        // OQthRVR, OQthCBR
write X15:OQthRVR=0x0100
write X15:OQthRM=0x0100         // OQthNVR, OQthRM
write X15:OQthNVR=0x0100
write X15:OQthABR=0x0100        // OQthAEP, OQthABR
write X15:OQthAEP=0x0100
write X15:OQthUBR=0x0100        // OQthUEP, OQthUBR
write X15:OQthUEP=0x0100
write X15:OQthCCL=0x0100        // OQthCCL
write X15:OQthRCI=0x0100        // OQthRCL, OQthRCI
```

Phase-out/Discontinued


```
write X15:OQthRCL=0x0100
write X15:OQthACI=0x0100        // OQthACL, OQthACI
write X15:OQthACL=0x0100
write X15:OQthUCI=0x0100        // OQthUCL, OQthUCI
write X15:OQthUCL=0x0100
write X15:UCthCBR=0x0200        // UCthCBR
write X15:UCthRVR=0x0200        // UCthRVR, UCthRM
write X15:UCthRM=0x0200
write X15:UCthNVR=0x0200        // UCthNVR
write X15:UCthABR=0x0200        // UCthABR, UCthAEP
write X15:UCthAEP=0x0200
write X15:UCthUBR=0x0200        // UCthUEP, UCthUBR
write X15:UCthUEP=0x0200
write X15:ALLmin=0x3400         // Allmin

// X15 UTOPIA 16 Bit IF 1 Configuration for P40 on UTOPIA 16 Bit IF 1
write UTPCFG3.EN=0
write UTPCFG1.EN=1,BW=1

// X15 Logical Port 0-3 Configuration for P40 on UTOPIA 16 Bit IF 1
write X15:PT0.SG=0,EN=1,UPN=1,PHY=0
write X15:PT1.SG=0,EN=1,UPN=1,PHY=1
write X15:PT2.SG=0,EN=1,UPN=1,PHY=2
write X15:PT3.SG=0,EN=1,UPN=1,PHY=3

// X15 Logical Port 0,1,2,3,5,6 Configuration for T20 on UTOPIA 8 Bit IF 2
//write X15:PT0.SG=0,EN=1,UPN=2,PHY=0
//write X15:PT1.SG=0,EN=1,UPN=2,PHY=1
//write X15:PT2.SG=0,EN=1,UPN=2,PHY=2
//write X15:PT3.SG=0,EN=1,UPN=2,PHY=3
write X15:PT5.SG=0,EN=1,UPN=2,PHY=4
write X15:PT6.SG=0,EN=1,UPN=2,PHY=5

// X15 Logical Port 7 Configuration for P30 on UTOPIA 8 Bit IF 0
write X15:PT7.SG=1,EN=1,UPN=0,PHY=0

// X15 PHY Module P40 Configuration on UTOPIA 16 Bit IF 1
write P3:MltUT=7
write P3.0:PHYIDR=0x80
write P3.1:PHYIDR=0x81
write P3.2:PHYIDR=0x82
write P3.3:PHYIDR=0x83

// X15 PHY Module T20 Configuration on UTOPIA 8 Bit IF 2
write P2:PHYADD0=0x90  // Set Physical Line0 to Utopia Address 0, set Bit 4 of Address = 1, because Bit 4 is
hard wired to 1
write P2:PHYADD1=0x91  // Set Physical Line1 to Utopia Address 1, set Bit 4 of Address = 1, because Bit 4 is
hard wired to 1
```

Phase-out/Discontinued

write P2:PHYADD2=0x92 **// Set Physical Line1 to Utopia Address 1, set Bit 4 of Address = 1, because Bit 4 is hard wired to 1**
write P2:PHYADD3=0x93 **// Set Physical Line1 to Utopia Address 1, set Bit 4 of Address = 1, because Bit 4 is hard wired to 1**
write P2:PHYADD4=0x94 **// Set Physical Line1 to Utopia Address 1, set Bit 4 of Address = 1, because Bit 4 is hard wired to 1**
write P2:PHYADD5=0x95 **// Set Physical Line1 to Utopia Address 1, set Bit 4 of Address = 1, because Bit 4 is hard wired to 1**

// Set X15 HT Register
write X15:HT0=0x52a00000
write X15:HT1=0x52a00400
write X15:HT2=0x52a00800
write X15:HT3=0x52a00c00
write X15:HT4=0x41800400
write X15:HT5=0x41800500
write X15:HT6=0x41800600
write X15:HT7=0x41800700
write X15:HT8=0x41800800
write X15:HT9=0x41800900
write X15:HT10=0x41800a00
write X15:HT11=0x41800b00
write X15:HT12=0x41800c00
write X15:HT13=0x41800d00
write X15:HT14=0x41800e00
write X15:HT15=0x41800f00
write X15:HT16=0x41801000
write X15:HT17=0x41801100
write X15:HT18=0x41801200
write X15:HT19=0x41801300
write X15:HT20=0x41801400
write X15:HT21=0x41801500
write X15:HT22=0x41801600
write X15:HT23=0x41801700
write X15:HT24=0x41801800
write X15:HT25=0x41801900
write X15:HT26=0x41801a00
write X15:HT27=0x41801b00
write X15:HT28=0x41801c00
write X15:HT29=0x41801d00

// setup a dais-chain for Test of:
// S20 -> P40 Port 0 -> P40 Port 1 -> P30 -> T20 Port 5 -> T20 Port 6 -> P40 Port 0
// Connect S20 with P40 Port 0, P40 Port 1 with P30, T20 with loop back RJ45 jacks
//
// X15 Logical Port Setup:

Phase-out/Discontinued


```
// Port0 -> Port1 -> Port7 -> Port5 -> Port6 -> Port0
//
// Port 0 VPI 00 VCI 50 -> Port 1 VPI 00 VCI 50
write HTT:0x000000C8=0xe0010032
write HTT:0x00000080=0xe0010032
// Port 1 VPI 00 VCI 50 -> Port 7 VPI 00 VCI 50
write HTT:0x000010C8=0xe0070032
write HTT:0x00001080=0xe0070032
// Port 7 VPI 00 VCI 50 -> Port 5 VPI 00 VCI 50
write HTT:0x00001CC8=0xe0050032
write HTT:0x00001C80=0xe0050032
// Port 5 VPI 00 VCI 50 -> Port 6 VPI 00 VCI 50
write HTT:0x000014C8=0xe0060032
write HTT:0x00001480=0xe0060032
// Port 6 VPI 00 VCI 50 -> Port 0 VPI 00 VCI 50
write HTT:0x000018C8=0xe0000032
write HTT:0x00001880=0xe0000032

// Enable X15 Switching
write X15:CMD.CMD=7

// Enable Status logging

write X15:CTENHT=0x9f
write X15:CTENHEC=0x9f
write X15:CTENMEM=0xc0c0
write X15:CTENRCV=0x81

//Enable P30 counters
write P0:PCFR2=0x0
```

Phase-out/Discontinued

APPENDIX APPLICATION CIRCUITS

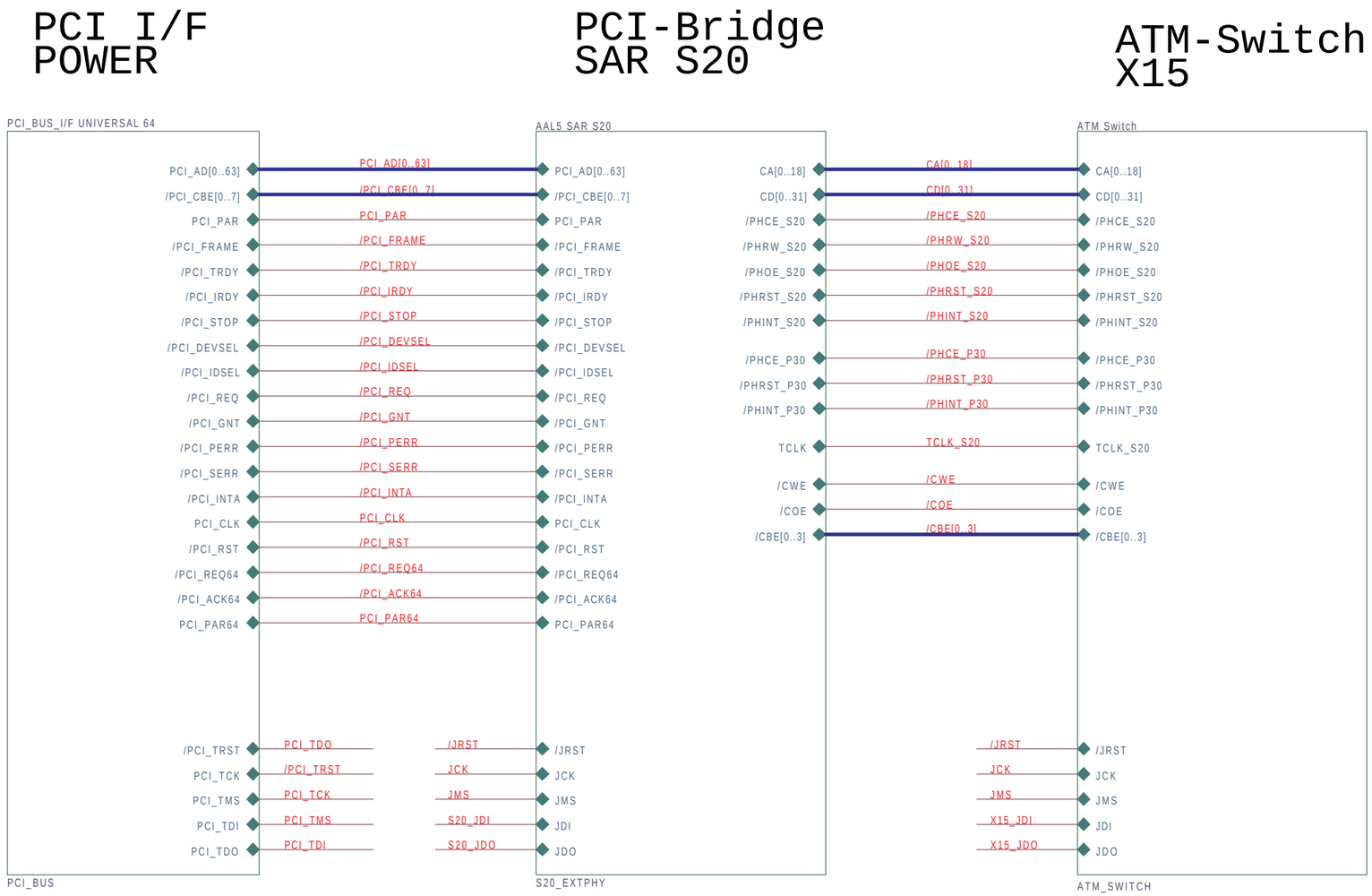
The application circuits used X15, P30, P40, and T20 are shown in this section.

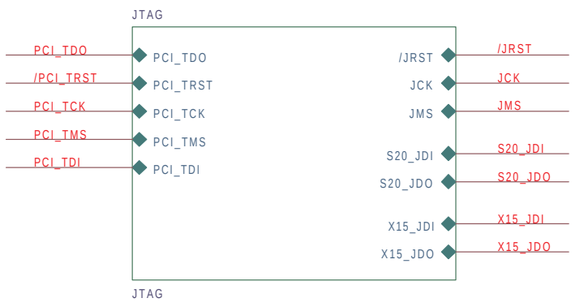
Phase-out/Discontinued

[MEMO]

Phase-out/Discontinued

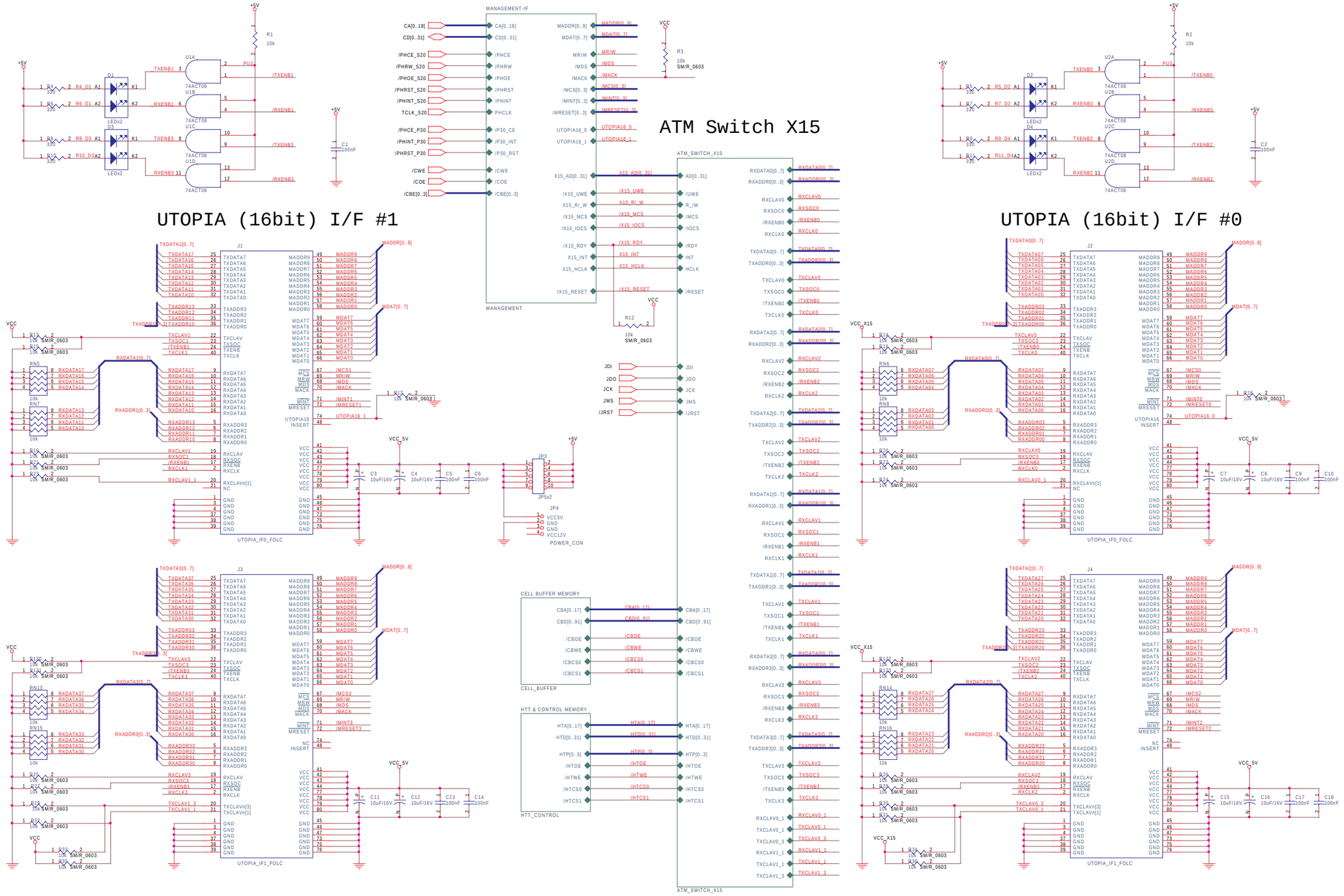
Figure A-1. X15 ATM Demo Board Circuit (TOP Schematic)





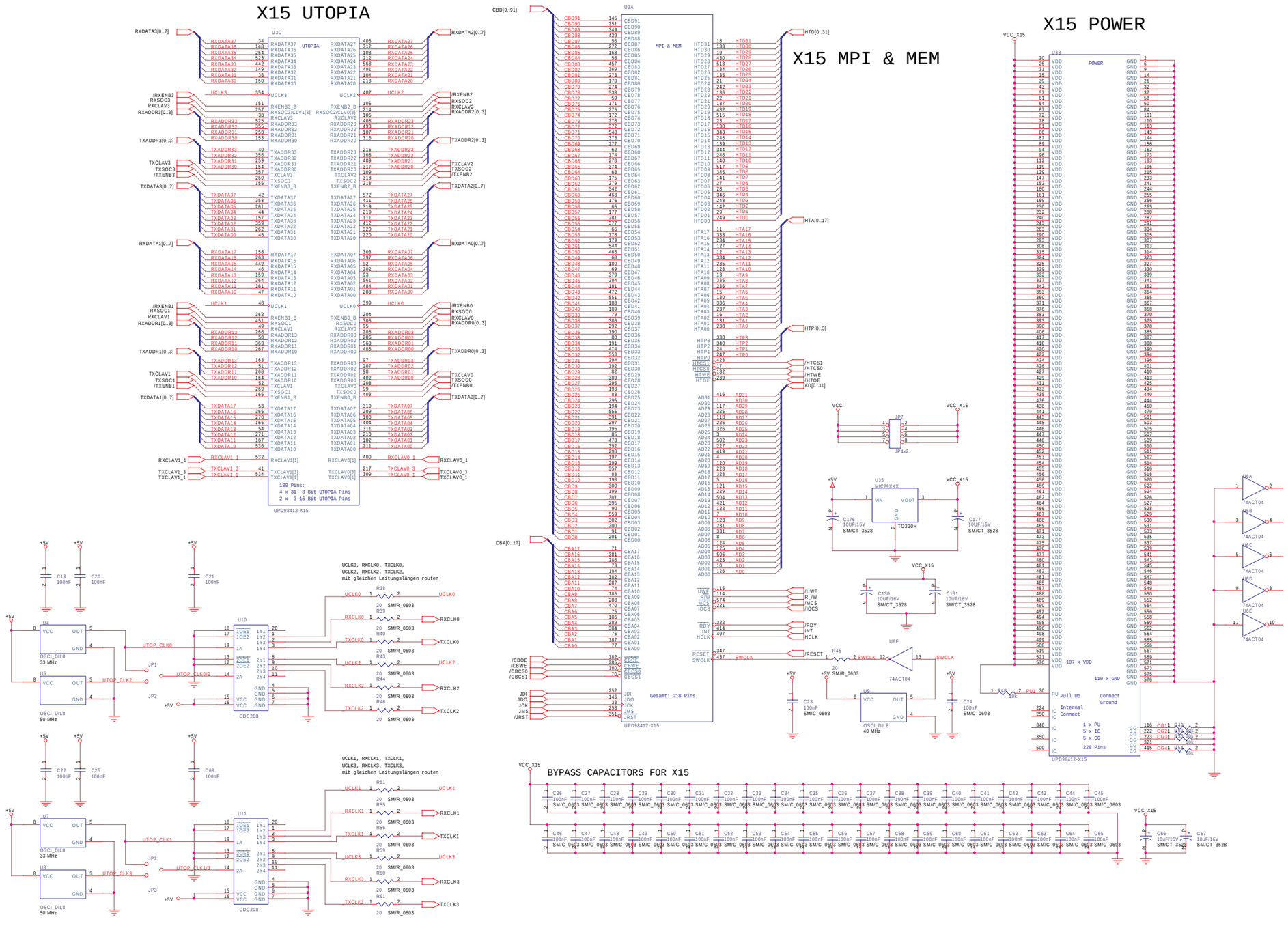
Phase-out/Discontinued

Figure A-2. X15 ATM Demo Board Circuit (ATM Switch) (1)



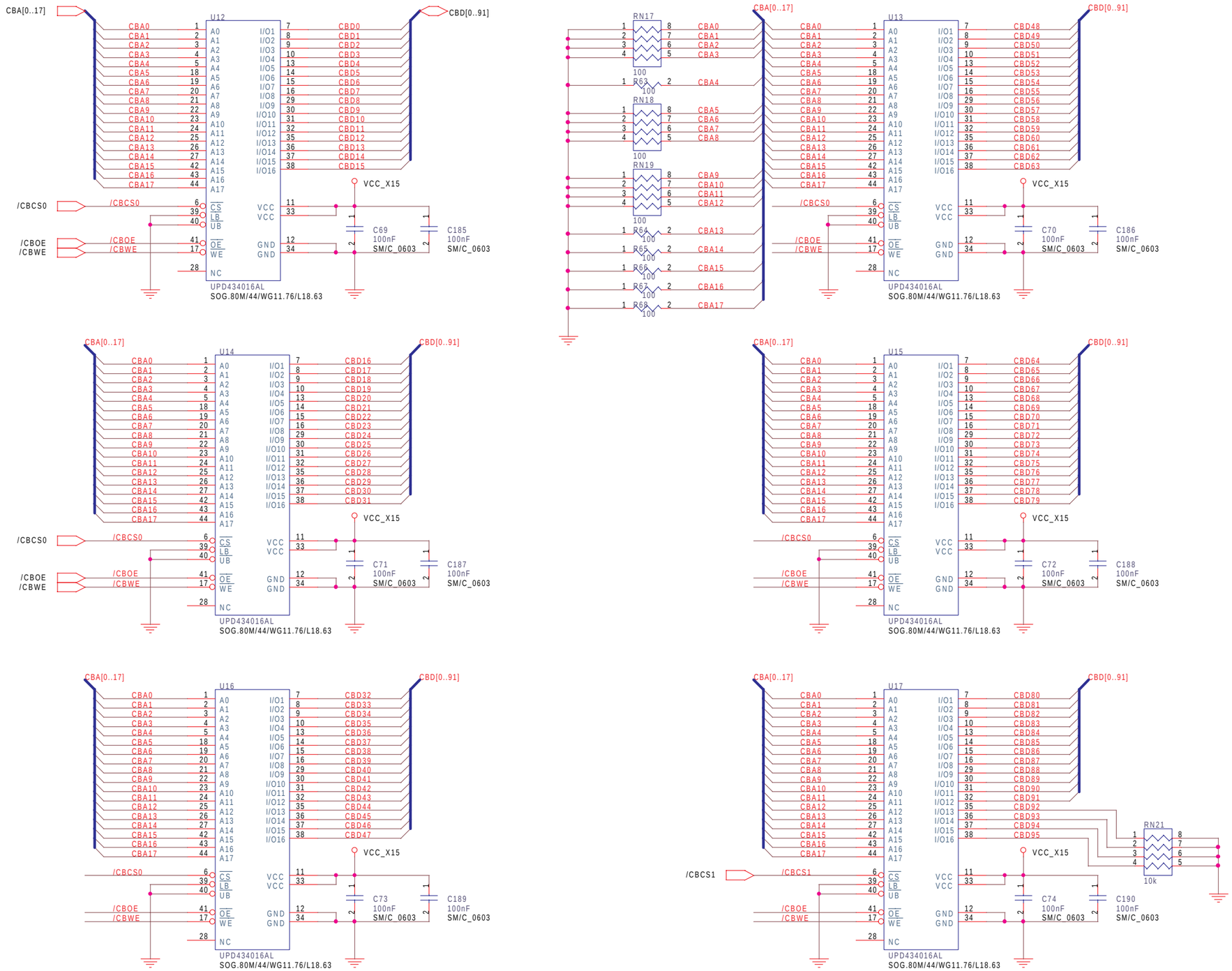
Phase-out/Discontinued

Figure A-3. X15 ATM Demo Board Circuit (ATM Switch) (2)



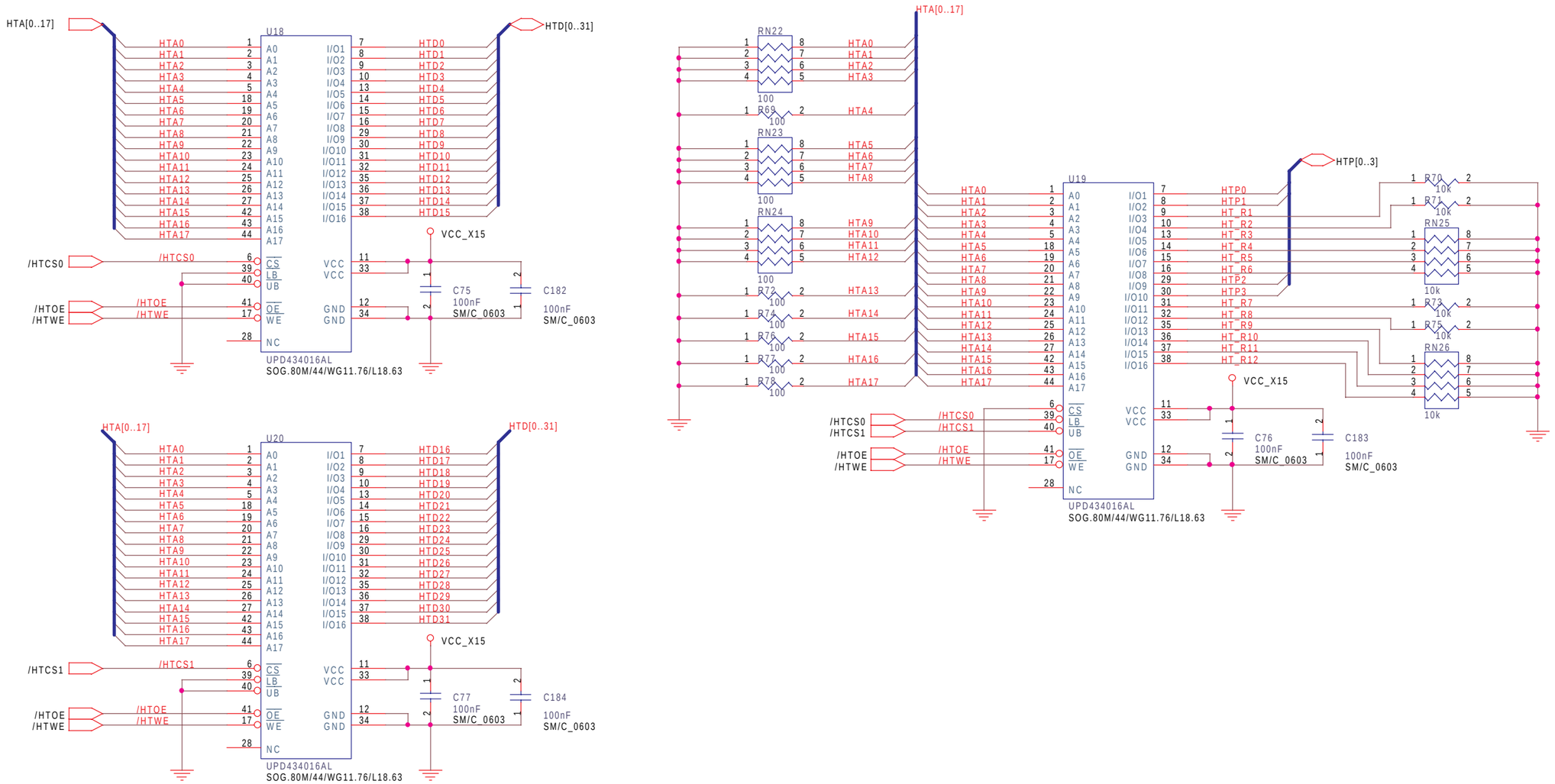
Phase-out/Discontinued

Figure A-4. X15 ATM Demo Board Circuit (Cell Buffer)



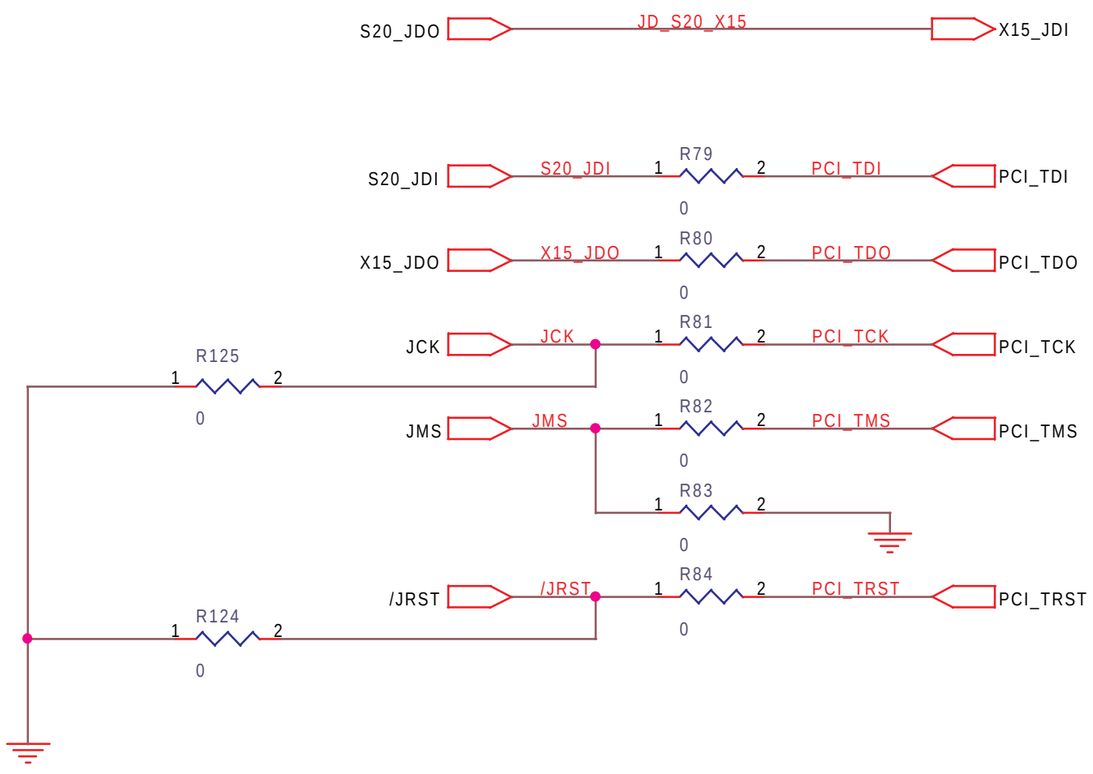
Phase-out/Discontinued

Figure A-5. X15 ATM Demo Board Circuit (HTT Control)



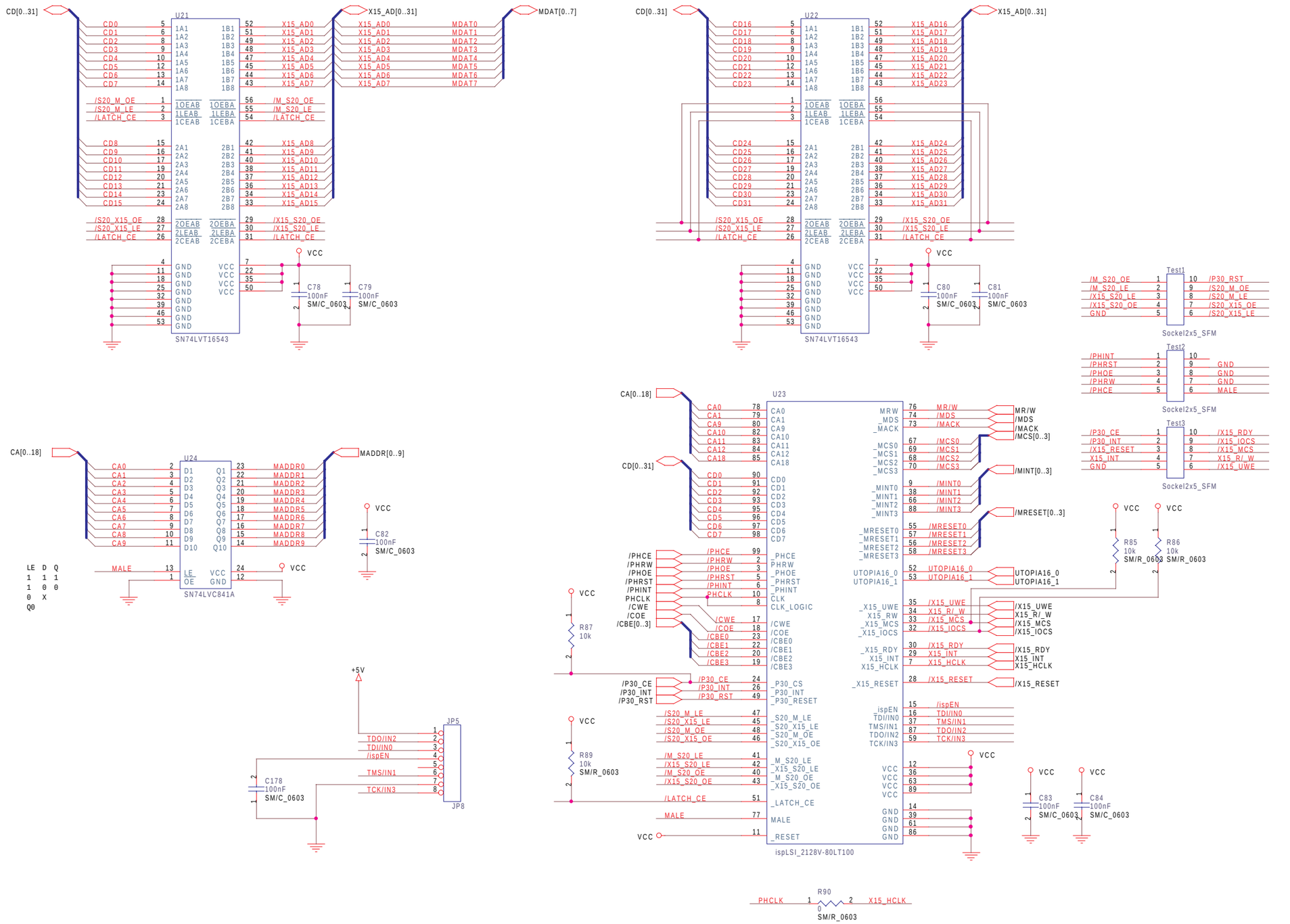
Phase-out/Discontinued

Figure A-6. X15 ATM Demo Board Circuit (PCI-JTAG Scanpath Connector)



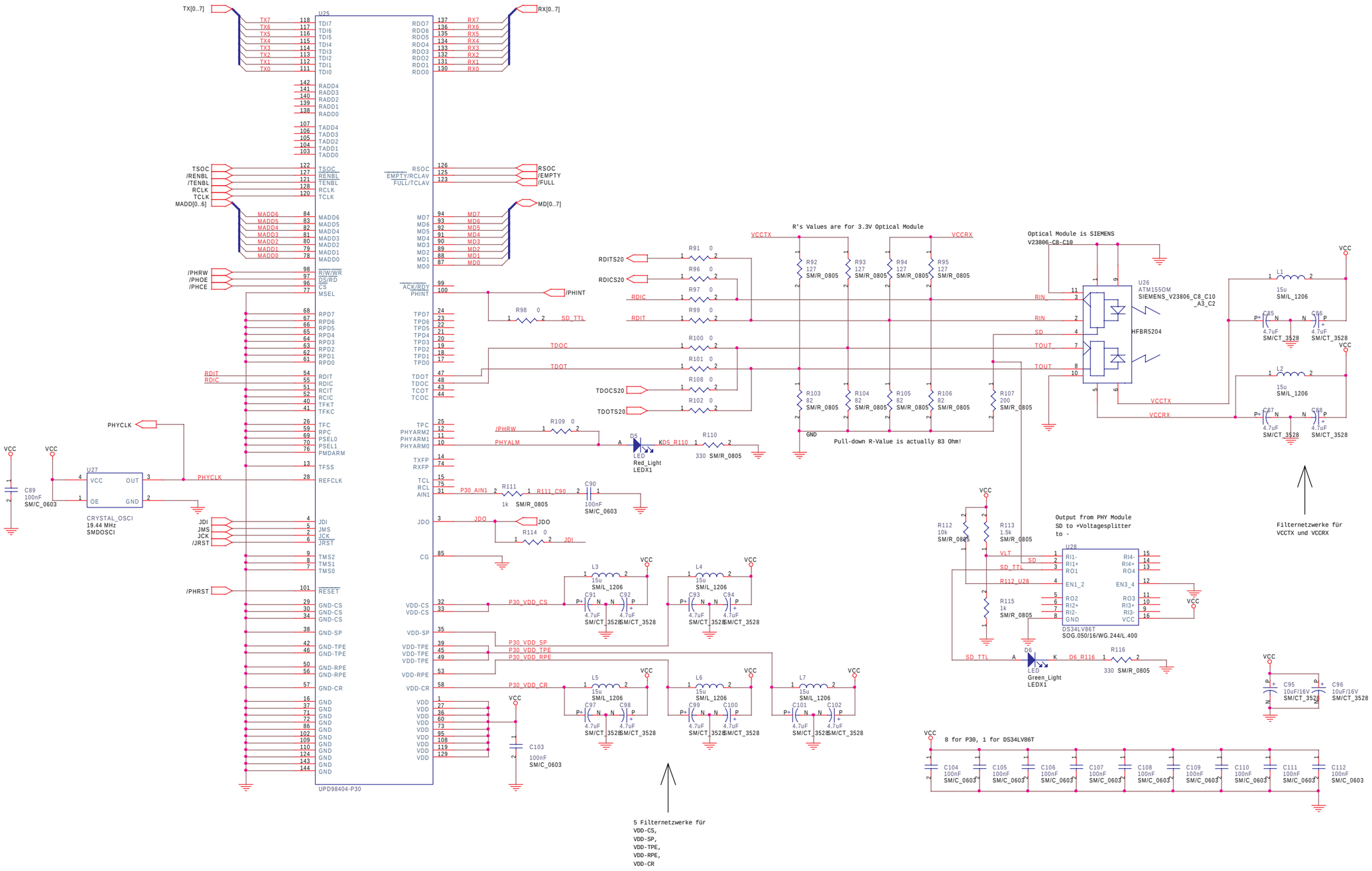
Phase-out/Discontinued

Figure A-7. X15 ATM Demo Board Circuit (Management)



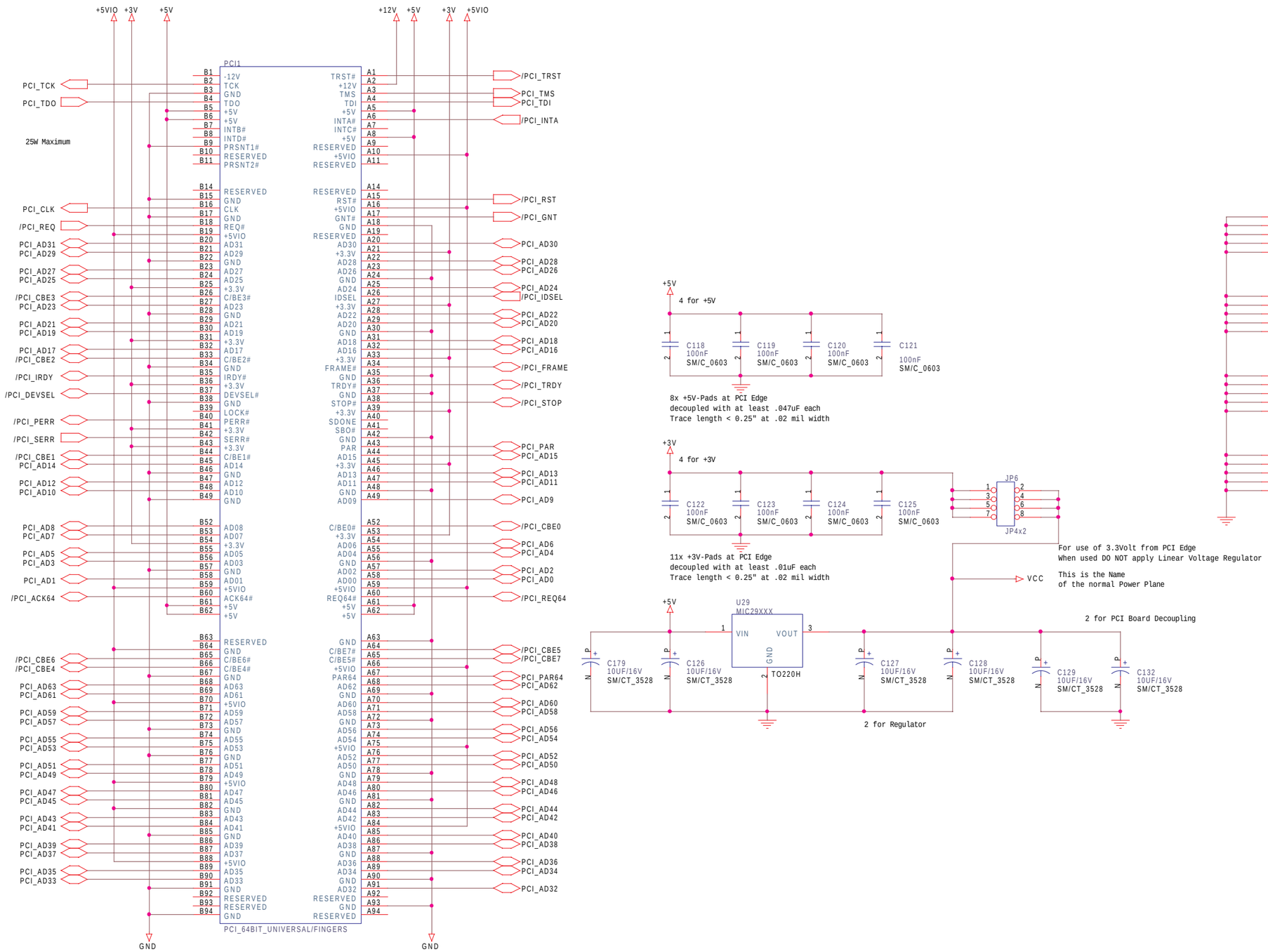
Phase-out/Discontinued

Figure A-8. X15 ATM Demo Board Circuit (P30)



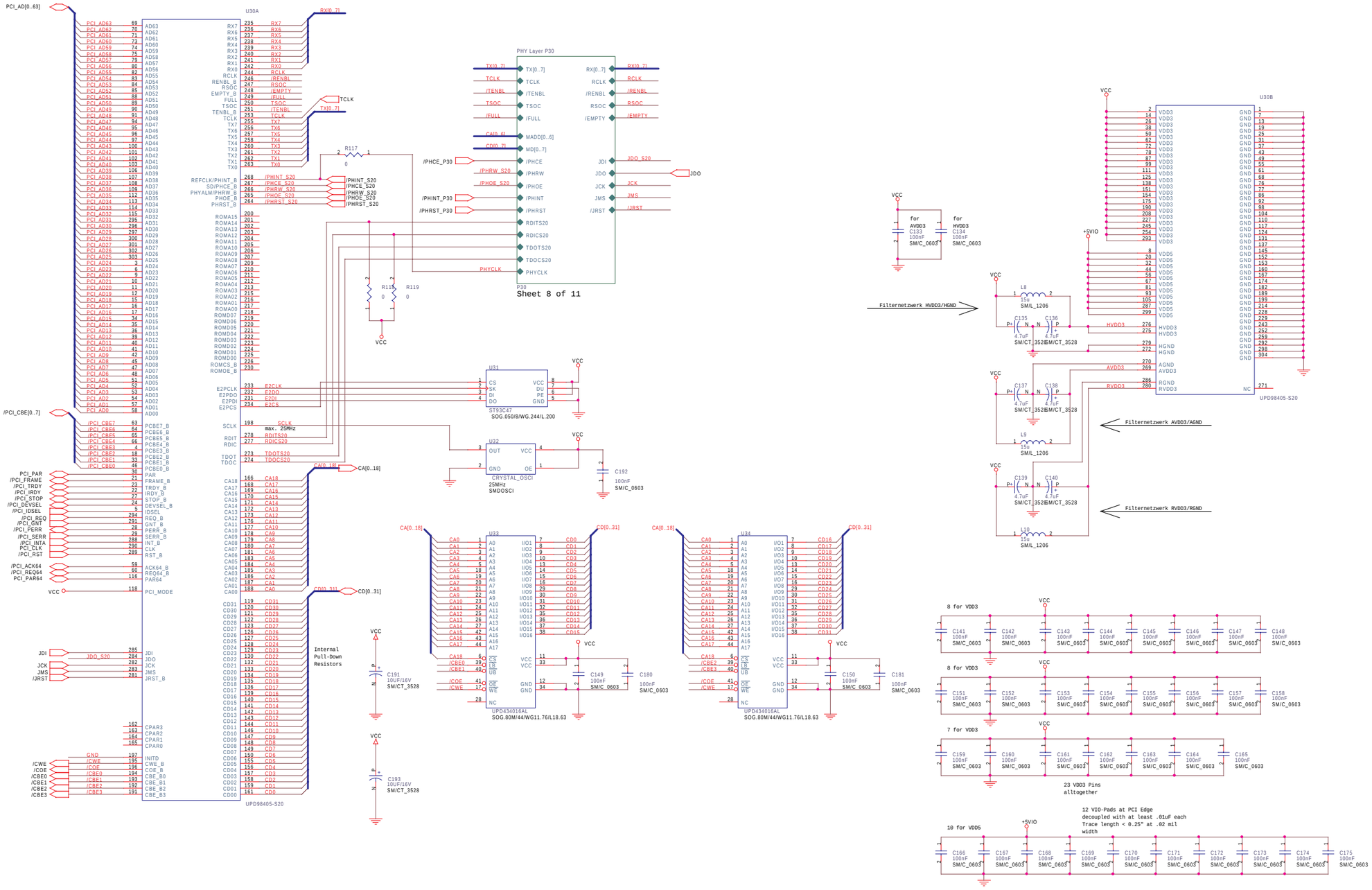
Phase-out/Discontinued

Figure A-9. X15 ATM Demo Board Circuit (PCI Bus)



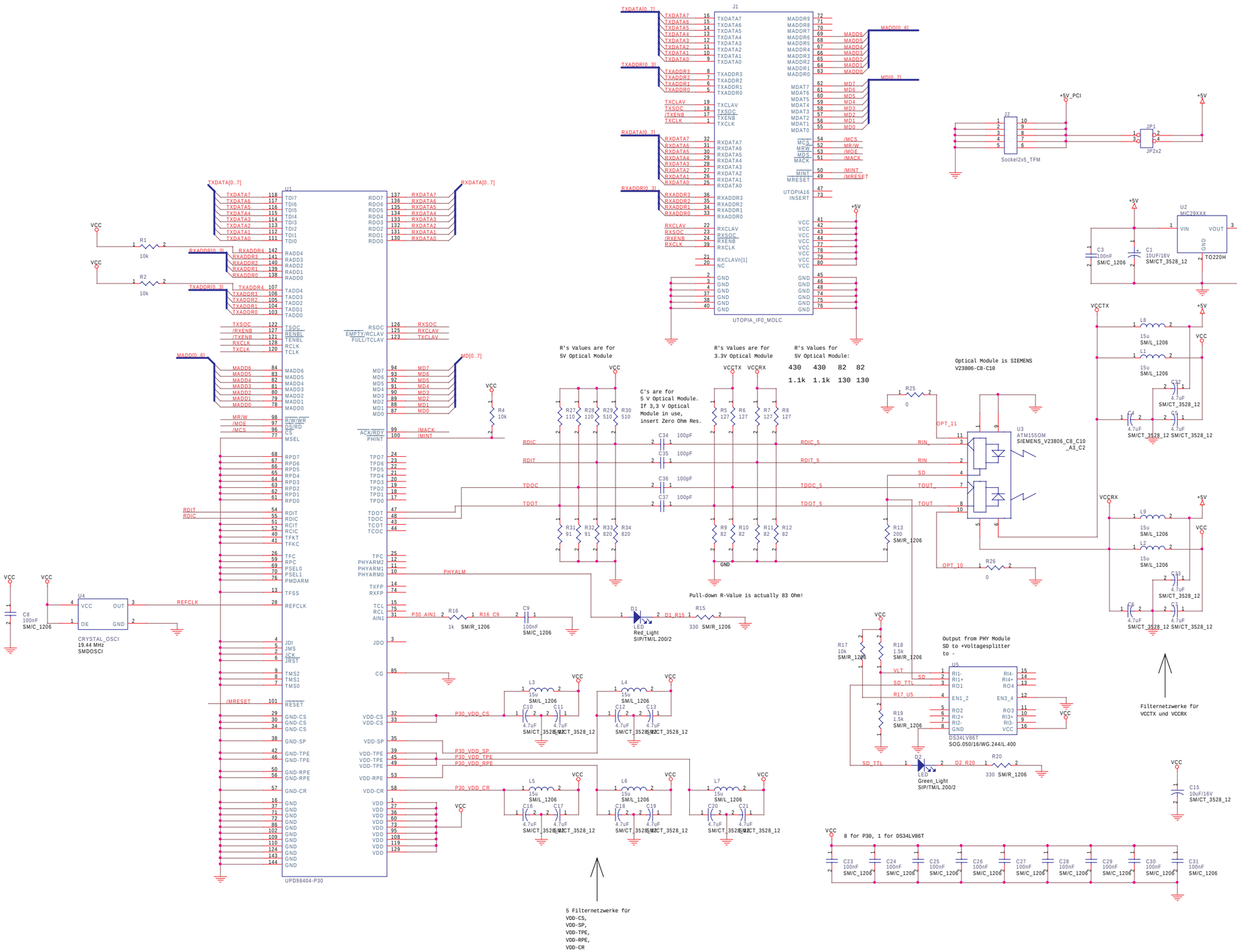
Phase-out/Discontinued

Figure A-10. X15 ATM Demo Board Circuit (SAR S20)



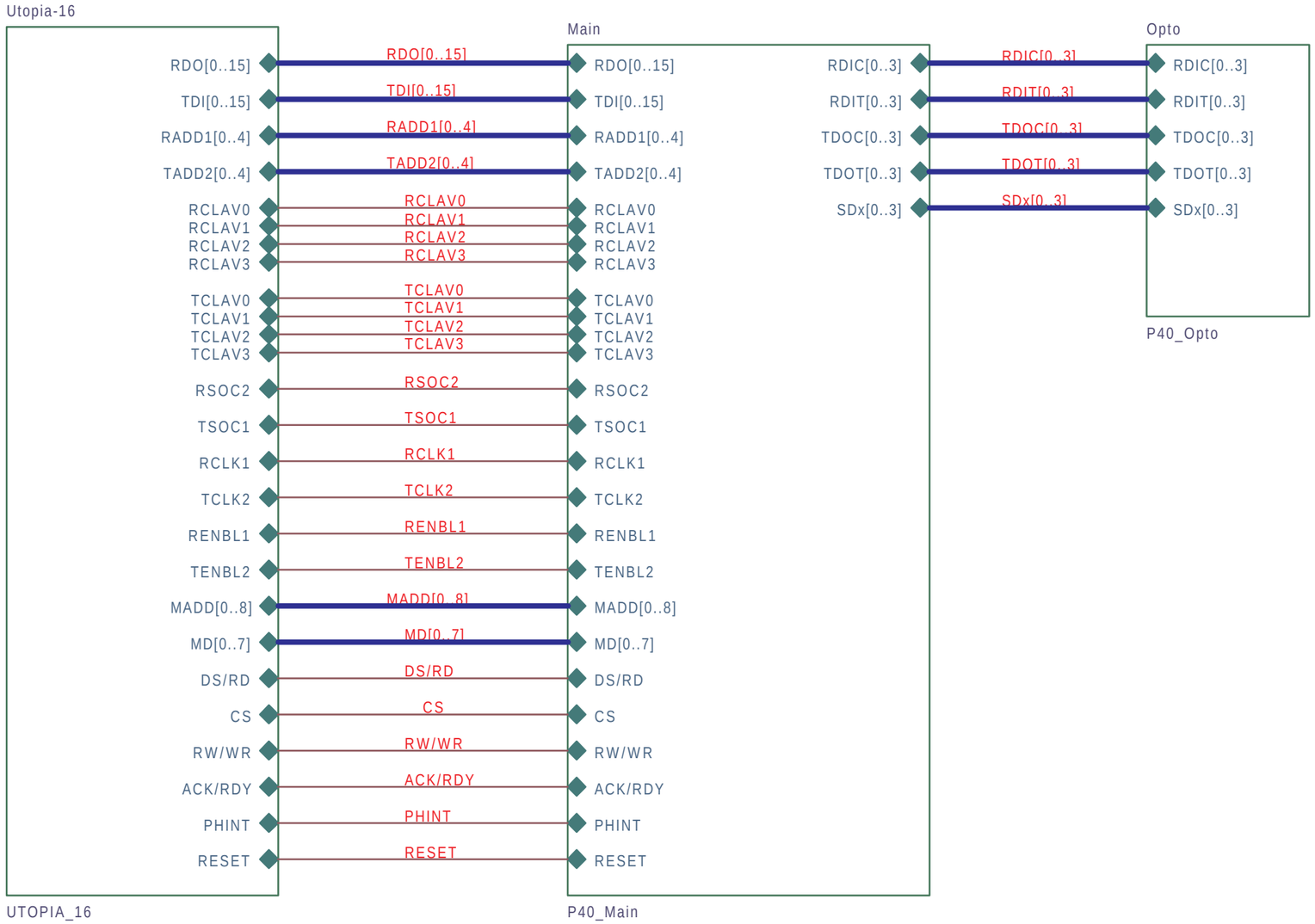
Phase-out/Discontinued

Figure A-11. P30 PHY Module Circuit



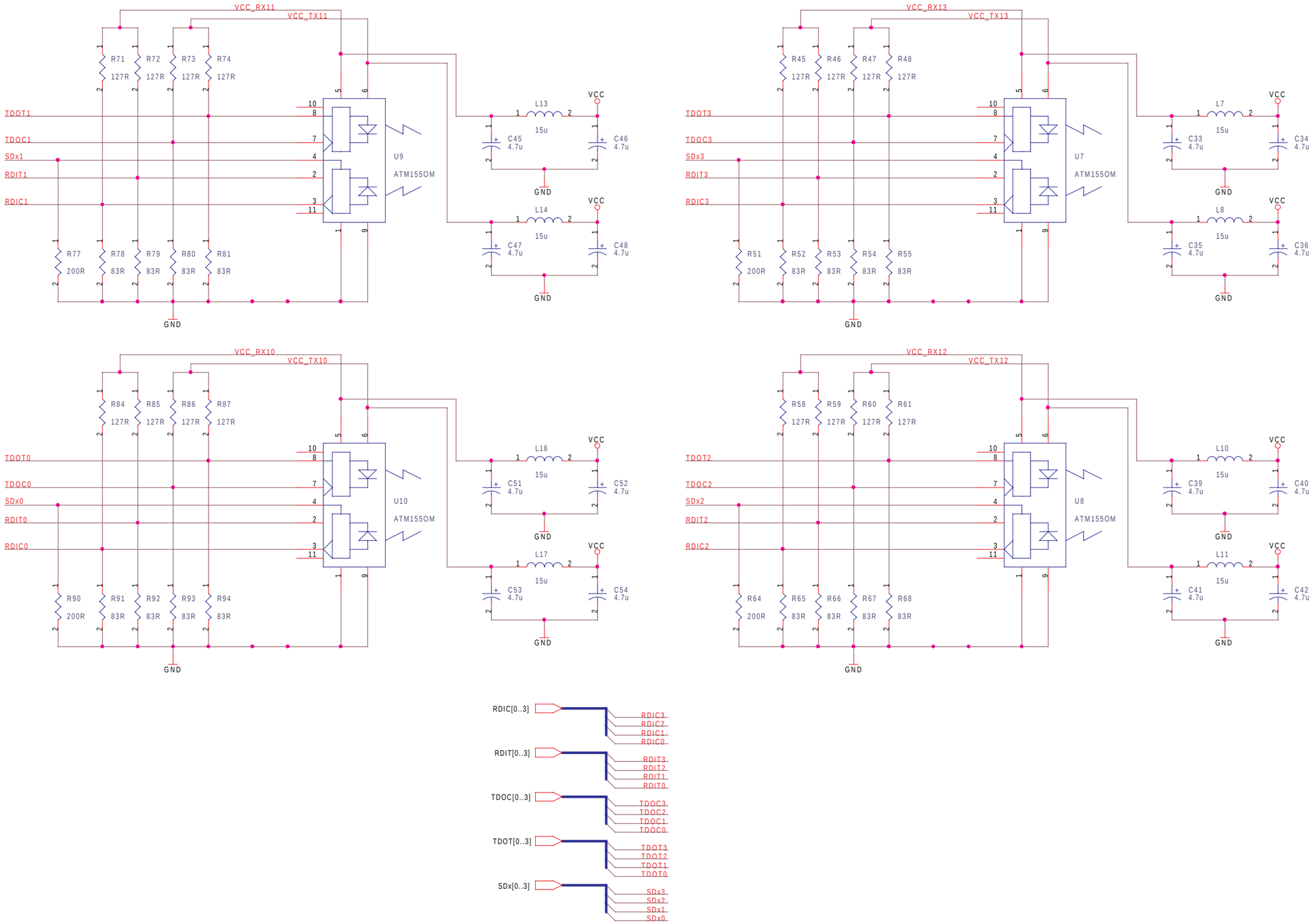
Phase-out/Discontinued

Figure A-12. P40 PHY Module Circuit (1)



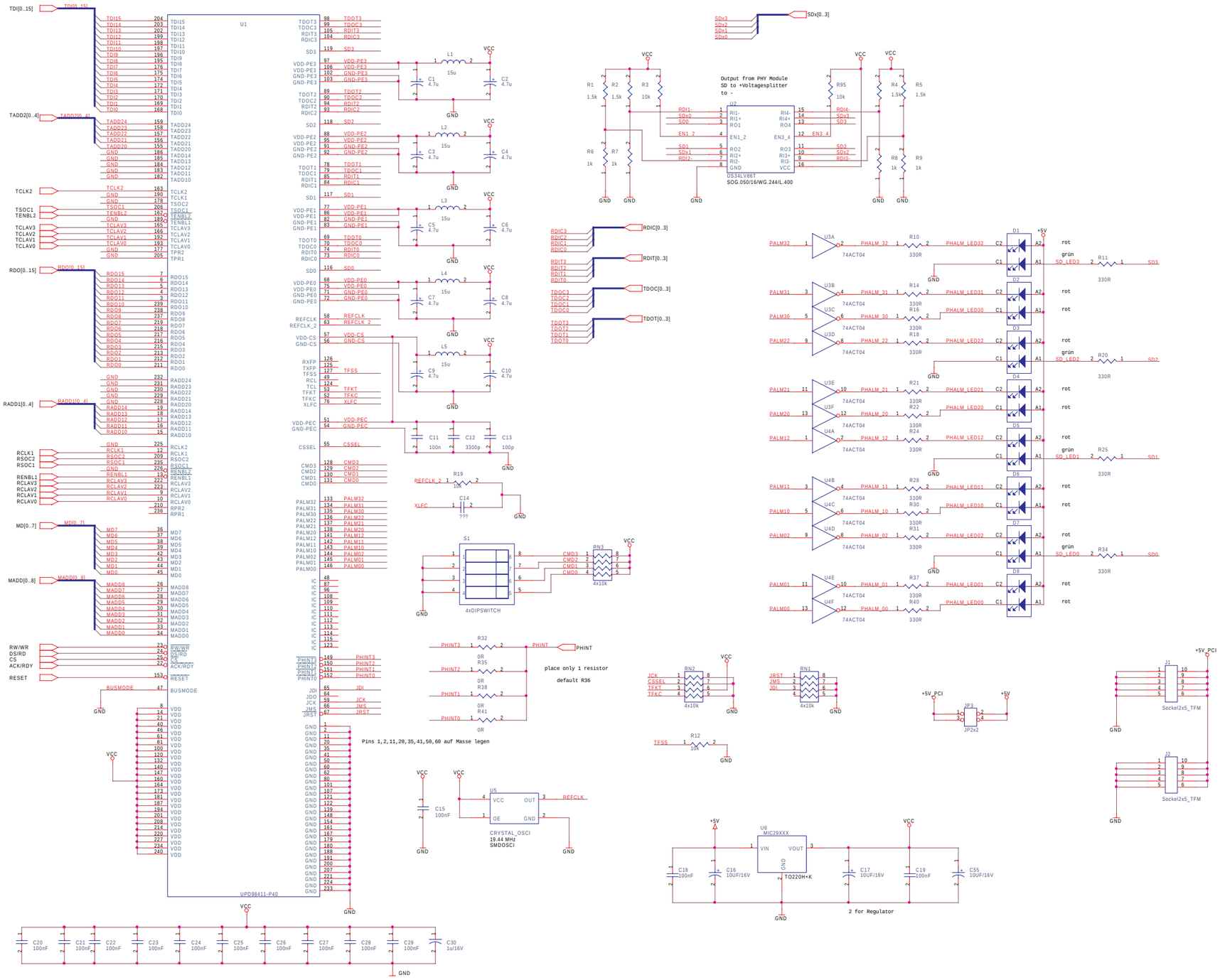
Phase-out/Discontinued

Figure A-13. P40 PHY Module Circuit (2)



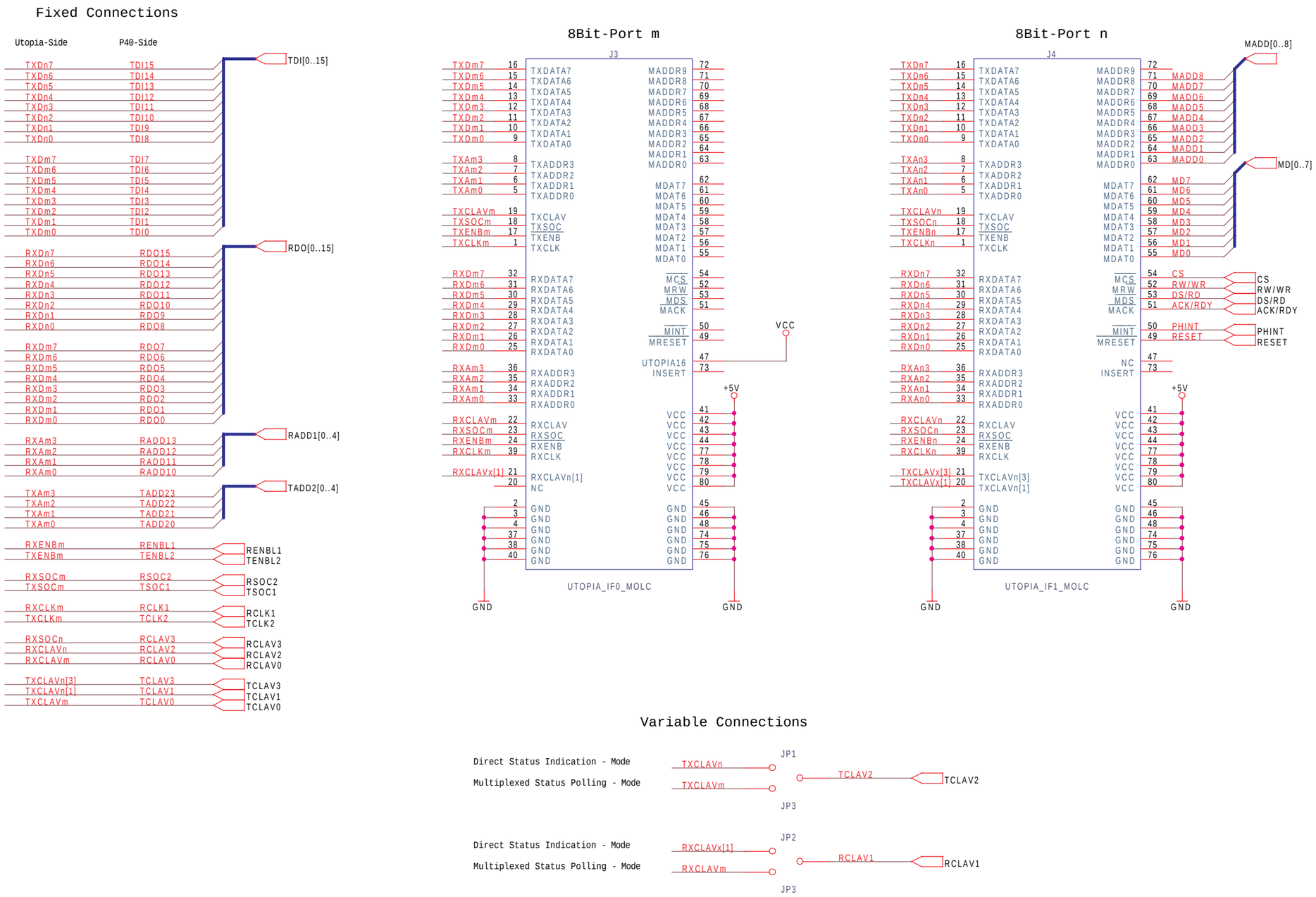
Phase-out/Discontinued

Figure A-14. P40 PHY Module Circuit (3)



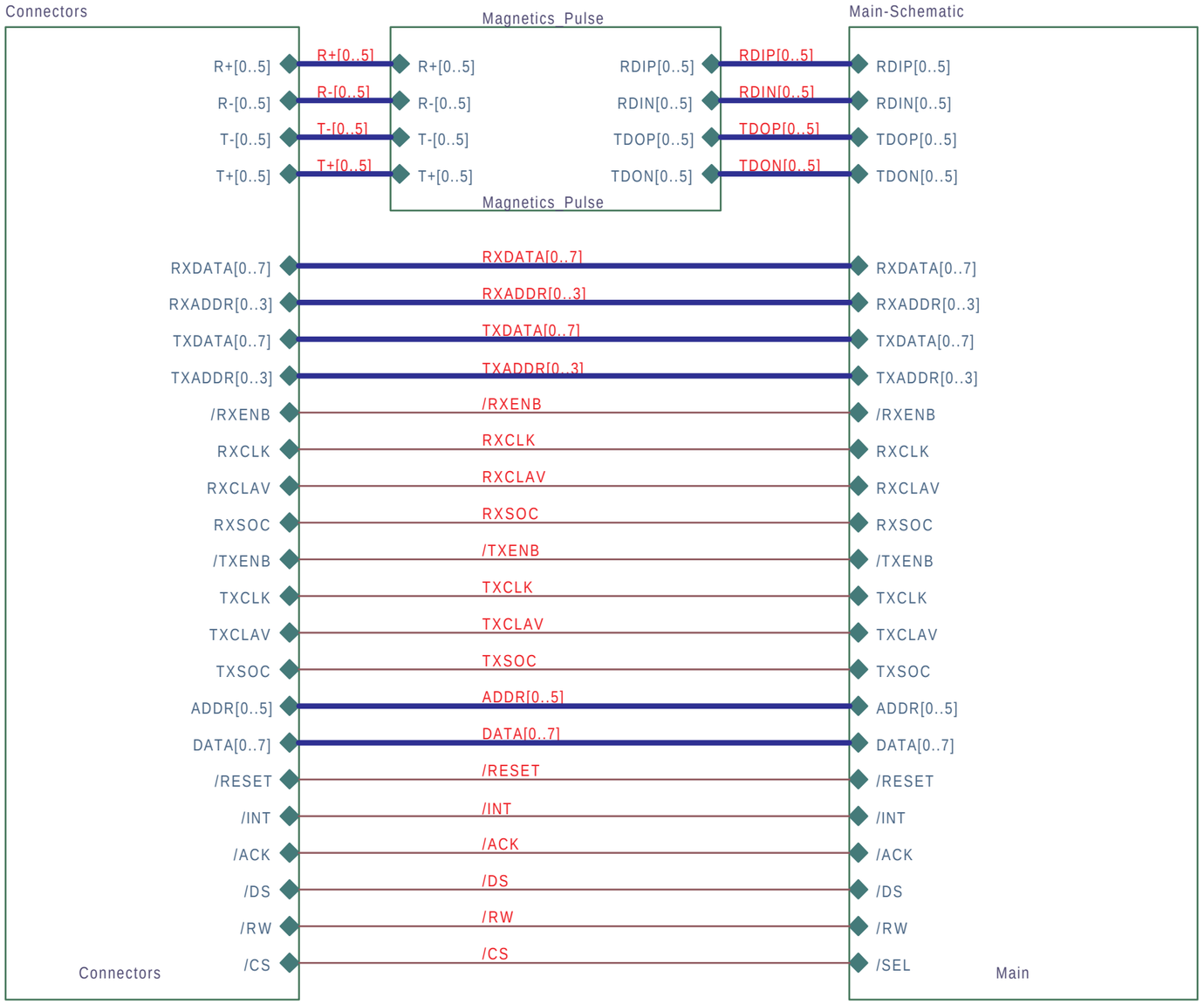
Phase-out/Discontinued

Figure A-15. P40 PHY Module Circuit (4)



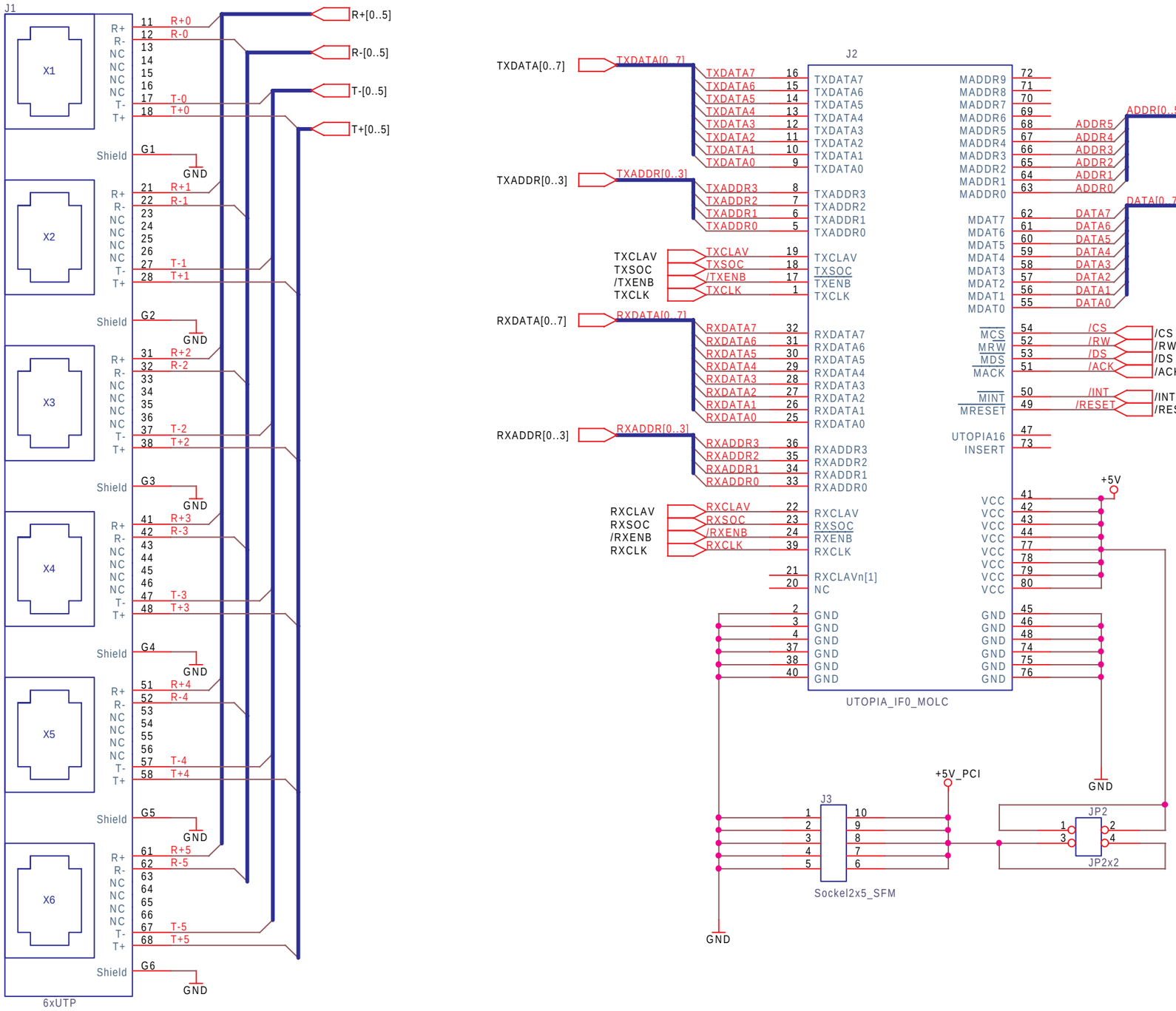
Phase-out/Discontinued

Figure A-16. T20 PHY Module Circuit (1)



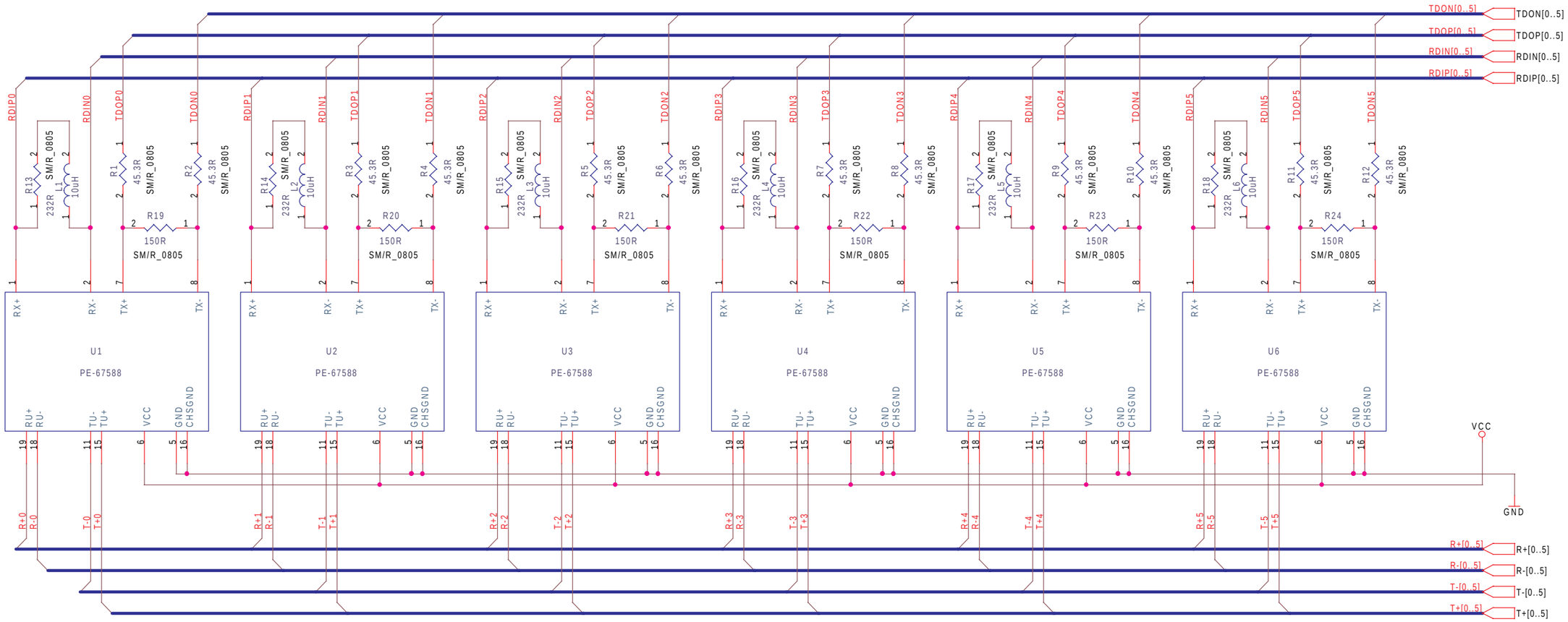
Phase-out/Discontinued

Figure A-17. T20 PHY Module Circuit (2)



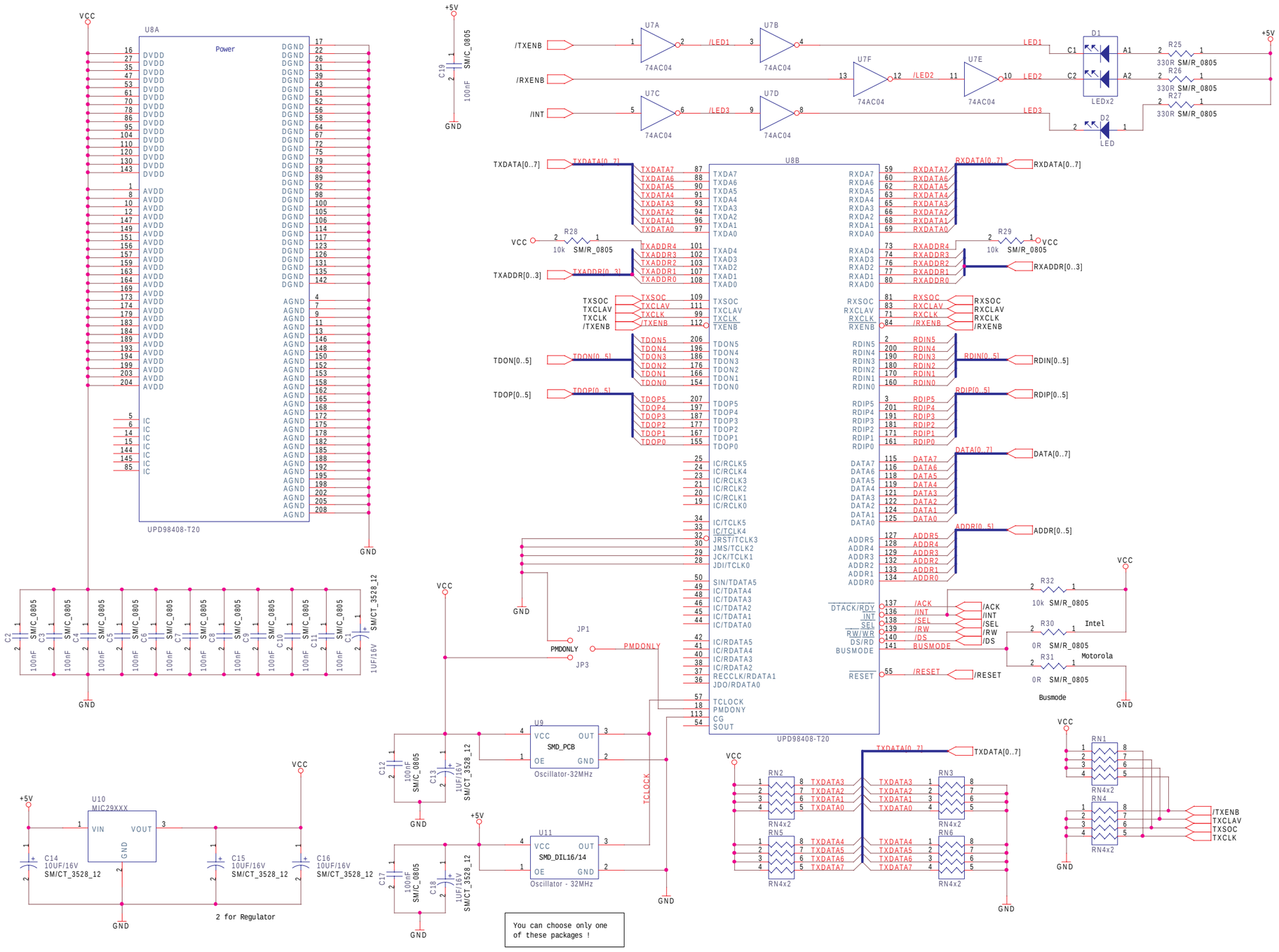
Phase-out/Discontinued

Figure A-18. T20 PHY Module Circuit (3)



Phase-out/Discontinued

Figure A-19. T20 PHY Module Circuit (4)



Phase-out/Discontinued

Table A-1. X15 ATM Switch Demo-Board Parts List (1/2)

NO.	AMOUNT	LOCATION	NAME	Remark
1	144	C1, C2, C5, C6, C9, C10, C13, C14, C17, C18, C19, C20, C21, C22, C23, C24, C25, C26, C27, C28, C29, C30, C31, C32, C33, C34, C35, C36, C37, C38, C39, C40, C41, C42, C43, C44, C45, C46, C47, C48, C49, C50, C51, C52, C53, C54, C55, C56, C57, C58, C59, C60, C61, C62, C63, C64, C65, C68, C69, C70, C71, C72, C73, C74, C75, C76, C77, C78, C79, C80, C81, C82, C83, C84, C89, C90, C103, C104, C105, C106, C107, C108, C109, C110, C111, C112, C118, C119, C120, C121, C122, C 123, C124, C125, C133, C134, C141, C142, C143, C144, C145, C146, C147, C148, C149, C150, C151, C152, C153, C154, C155, C156, C157, C158, C159, C160, C161, C162, C163, C164, C165, C166, C167, C168, C169, C170, C171, C172, C173, C174, C175, C178, C180, C181, C182, C183, C184, C185, C186, C187, C188, C189, C190, C192	Ceramic condenser GRM39F104Z25 (0.1 μF)	
2	24	C3, C4, C7, C8, C11, C12, C15, C16, C66, C67, C95, C96, C126, C127, C128, C129, C130, C131, C132, C176, C177, C179, C191, C193	Tantalum condenser TEMSVB21C106M8R (10 μF/16 V)	
3	20	C85, C86, C87, C88, C91, C92, C93, C94, C97, C98, C99, C100, C101, C102, C135, C136, C137, C138, C139, C140	Tantalum condenser 25MCM475MB2 (4.7 μF/25 V)	
4	4	D1, D2, D3, D4	LED 553-01-33 (3 mm) (yellow x 2)	
5	1	D5	LED 551-0407 (3 mm) (red)	
6	1	D6	LED 551-0207 (3 mm) (green)	
7	2	JP2, JP1	PS-3PF-S4T1-PKL1	
8	1	JP3	PS-10PF-D4T1-PKL1	
9	1	JP4	350424-1	
10	1	JP5	PS-10PF-S4T1-PKL1	
11	2	JP7, JP6	PS-10PF-D4T1-PKL1	
12	2	J2, J1 UTPOIA_IF0_FOLC	FOLC-120-L2-S-Q-LC	
13	2	J4, J3 UTOPIA_IF1_FOLC	FOLC-120-L2-S-Q-LC	
14	3	Test1, Test2, Test3	Socket 2 x 5_SFM	Non-mount
15	4	J5, J6, J7, J8	SFM-105-L2-S-D	
16	10	L1, L2, L3, L4, L5, L6, L7, L8, L9, L10	Inductor MLF3216C150M (15 μH)	
17	11	RN5, RN6, RN7, RN8, RN13, RN14, RN15, RN16, RN21, RN25, RN26	NW register CN1J4A 10 KΩJ	

Phase-out/Discontinued

Table A-1. X15 ATM Switch Demo-Board Parts List (2/2)

NO.	AMOUNT	LOCATION	NAME	Remark
18	46	R1, R2, R3, R12, R13, R14, R15, R16, R17, R18, R19, R20, R21, R22, R23, R24, R25, R26, R27, R28, R29, R30, R31, R32, R33, R34, R35, R36, R48, R49, R52, R53, R54, R70, R71, R73, R75, R85, R86, R87, R89, R112, R120, R121, R122, R123	Register RK73K1J 10 KΩJ	R13 to R16, R29 to R36, R89, R120 to R123 are non-mount.
19	6	RN17, RN18, RN19, RN22, RN23, RN24	NW register CN1J4A 100 ΩJ	
20	12	R63, R64, R65, R66, R67, R68, R69, R72, R74, R76, R77, R78	Register RK73K1J 100 ΩJ	
21	10	R4, R5, R6, R7, R8, R9, R10, R11, R110, R116	Register RK73K1J 330 ΩJ	
22	13	R38, R39, R40, R43, R44, R45, R46, R51, R55, R56, R59, R60, R61	Register RK73K1J 20 ΩJ	
23	15	R79, R80, R81, R82, R83, R84, R90, R98, R109, R114, R117, R118, R119, R124, R125	Register RK73K1J 0 ΩJ	R79 to R82, R84, R90, R98, R109, R114, R117 are non-mount.
24	8	R91, R96, R97, R99, R100, R101, R102, R108	Register RK73K2B 0 ΩJ	R91, R96, R102, R108 are non-mount.
25	4	R92, R93, R94, R95	Register RK73K2A 130 ΩJ	
26	4	R103, R104, R105, R106	Register RK73K2A 82 ΩJ	
27	1	R107	Register RK73K2A 200 ΩJ	
28	3	R111, R113, R115	Register RK73K2A 1 KΩJ	
29	2	U1, U2	IC 74ACT08	
30	1	U3	IC μPD98412-X15	
31	2	U4, U7	IC socket IC26-0803-GS4 mount parts SG8002DCPTC 33 MHz	
32	2	U5, U8	IC socket IC26-0803-GS4 mount parts SG8002DCPTC 50 MHz	
33	5	U9	IC socket IC26-0803-GS4 mount part TC0711S4 40 MHz	
34	1	U6	IC 74ACT04	
35	2	U10, U11	IC CDC208	
36	11	U12, U13, U14, U15, U16, U17, U18, U19, U20, U33, U34	IC μPD434016ALG5-A12-7KF	
37	2	U21, U22	IC SN74LVT16543	
38	1	U23	IC ispLSI_2128V-80LT10	
39	1	U24	IC SN74LVTH16543DGG	
40	1	U25	IC μPD98404-P30	
41	1	U26	Optical module V23809-C8-C10	
42	1	U32	OSC SG8002JCSCC 25.000 MHz	
43	1	U27	OSC SG8002JCSCC 19.440 MHz	
44	1	U28	IC DS34LV86T	
45	2	U35, U29	Regulator MIC29500-3.3BT	
46	1	U30	IC μPD98405-S20	
47	1	U31	IC M93C56-WMN6	

Phase-out/Discontinued

Table A-2. P30 PHY Module Parts List

NO.	AMOUNT	LOCATION	NAME	Remark
1	3	C1, C2, C15	Tantalum condenser TEMSVB21C106M8R (10 μF/16 V)	
2	13	C3, C8, C9, C22, C23, C24, C25, C26, C27, C28, C29, C30, C31	Ceramic condenser GRM42-6B104K50 (0.1 μF)	
3	16	C4, C5, C6, C7, C10, C11, C12, C13, C16, C17, C18, C19, C20, C21, C32, C33	Tantalum condenser 25MCM475MB2 (4.7 μF/25 V)	C32, C33 are non-mount.
4	4	C34, C35, C36, C37	Register RK73K2B 0ΩJ	Register-mount
5	1	D1	LED 551-0407 (3 mm) (red)	
6	1	D2	LED 551-0207 (3 mm) (green)	
7	1	JP 1	Jumper PS-10PF-D4T1-PKL1	Non-mount
8	1	J1 UTOPIA_IF0_MOLC	Connector MOLC-120-L2-S-Q-LC	
9	1	J2 Socket 2 x 5_TFM	Connector TFM-105-L2-S-D	
10	9	L1, L2, L3, L4, L5, L6, L7, L8, L9	Inductor MLF3216C150M (15 μH)	L8, L9 are non-mount.
11	4	R1, R2, R4, R17	Register RK73K2B 10 KΩJ	
12	4	R5, R6, R7, R8	Register RK73K2B 130 ΩJ	R7, R8 are non-mount.
13	4	R9, R10, R11, R12	Register RK73K2B 82 ΩJ	R11, R12 are non-mount.
14	1	R13	Register RK73K2B 200 ΩJ	
15	2	R15, R20	Register RK73K2B 330 ΩJ	
16	1	R16	Register RK73K2B 1 KΩJ	
17	2	R19, R18	Register RK73K2B 1.5 KΩJ	
18	2	R25, R26	Register RK73K2B 0 ΩJ	Non-mount
19	2	R28, R27	110	Non-mount
20	2	R30, R29	Register RK73K2B 130 ΩJ	130 Ω-mount
21	2	R32, R31	91	Non-mount
22	2	R34, R33	Register RK73K2B 82 ΩJ	82 Ω-mount
23	1	U1	IC μPD98404-P30	
24	1	U2	Regulator MIC29150 3.3BT	
25	1	U3	Optical module V23809-C8-C10	
26	1	U4	OSC SG8002JCSCC 19.440 MHz	
27	1	U5	IC DS34LV86T	

Phase-out/Discontinued

Table A-3. P40 PHY Module Parts List

NO.	AMOUNT	LOCATION	NAME	Remark
1	26	C1, C2, C3, C4, C5, C6, C7, C8, C9, C10, C33, C34, C35, C36, C39, C40, C41, C42, C45, C46, C47, C48, C51, C52, C53, C54	Tantalum condenser 25MCM475MB2 (4.7 μF/25 V)	
2	1	C12 3300p	Ceramic condenser GRM42-6CH332J50 (3300 pF)	
3	1	C13 100p	Ceramic condenser GRM40-6CH101J50 (100 pF)	
4	1	C14		Non-mount
5	14	C11, C15, C18, C19, C20, C21, C22, C23, C24, C25, C26, C27, C28, C29	Ceramic condenser GRM40F104Z50 (0.1 μF)	
6	3	C16, C17, C55	Tantalum condenser TEMSVB21C106M8R (10 μF/16 V)	
7	1	C30	Tantalum condenser 35MCM105MA (1 μF/35V)	
8	4	D1, D3, D5, D7	LED 553-07-12 (3 mm) (red x green)	
9	4	D2, D4, D6,D8	LED 553-01-11 (red x 2)	
10	2	JP1, JP2	Jumper PS-3PF-S4T1-PKL1	
11	1	JP3	Jumper PS-10PF-D4T1-PKL1	
12	2	J2, J1 Socket 2 x 5_TFM	Connector TFM-105-L2-S-D	Non-mount
13	1	J3 UTOPIA_IF0_MOLC	Connector MOLC-120-L2-S-Q-LC	
14	1	J4 UTOPIA_IF1_MOLC	Connector MOLC-120-L2-S-Q-LC	
15	13	L1, L2, L3, L4, L5, L7, L8, L10, L11, L13, L14, L16, L17	Inductor MLF3216C150M (15 μH)	
16	3	RN1, RN2, RN3	NW register NMR14 (CRML08W) 10 KΩJ	
17	4	R1, R2, R4, R5	Register RK73K2A 1.5 KΩJ	
18	4	R3, R12, R19, R95	Register RK73K2A 10 KΩJ	
19	4	R6, R7, R8, R9	Register RK73K2A 1 KΩJ	
20	16	R10, R11, R14, R16, R18, R20, R21, R22, R24, R25, R28, R30, R31, R34, R37, R40	Register RK73K2A 330 ΩJ	
21	4	R32, R35, R38, R41	Register RK73K2A 0 ΩJ	R32, R35, R38 are non-mount.
22	16	R45, R46, R47, R48, R58, R59, R60, R61, R71, R72, R73, R74, R84, R85, R86, R87	Register RK73K2B 130 ΩJ	
23	4	R51, R64, R77, R90	Register RK73K2A 200 ΩJ	
24	16	R52, R53, R54, R55, R65, R66, R67, R68, R78, R79, R80, R81, R91, R92, R93, R94	Register RK73K2B 82 ΩJ	
25	1	S1	DIPSW DSS104	
26	1	U1	IC μPD98411-P40	
27	1	U2	IC DS34LV86T	
28	2	U3, U4	IC 74ACT04	
29	1	U5	OSC SG8002JCSCC 19.440 MHz	
30	1	U6	Regulator MIC29150 3.3BT	
31	4	U7, U8, U9, U10	Optical module V23809-C8-C10	

Phase-out/Discontinued

Table A-4. T20 PHY Module Parts List

NO.	AMOUNT	LOCATION	NAME	Remark
1	3	C1, C13, C18	Tantalum condenser 35MCM105MA (1 μF/35V)	C18 is non-mount.
2	13	C2, C3, C4, C5, C6, C7, C8, C9, C10, C11, C12, C17, C19	Ceramic condenser GRM40F104Z50 (0.1 μF)	C12 is non-mount.
3	3	C14, C15, C16	Tantalum condenser TEMSVB21C106M8R (10 μF/16 V)	C15 is non-mount.
4	1	D1	LED 553-01-33 (3 mm) (yellow x 2)	
5	1	D2	LED 551-0407 (3 mm) (red)	
6	1	JP1	Jumper PS-3PF-D4T1-PKL1	Non-mount
7	1	JP2	Jumper PS-10PF-D4T1-PKL1	
8	1	J1	Modular jack 569261-1	
9	1	J2 UTOPIA_IF0_MOLC	Connector MOLLC-120-L2-S-Q-LC	
10	1	J3	Connector TFM-105-L2-S-D	
11	6	L1, L2, L3, L4, L5, L6	Inductor MLF3216C150M (10 μH)	
12	6	RN1, RN2, RN3, RN4, RN5, RN6	NW register CN1J4A 10 KΩJ	Non-mount
13	12	R1, R2, R3, R4, R5, R6, R7, R8, R9, R10, R11, R12	Register RK73K2A 47 ΩJ	
14	6	R13, R14, R15, R16, R17, R18	Register RK73K2A 270 ΩJ	
15	6	R19, R20, R21, R22, R23, R24	Register RK73K2A 150 ΩJ	
16	3	R25, R26, R27	Register RK73K2A 330 ΩJ	
17	3	R28, R29, R32	Register RK73K2A 10 KΩJ	
18	2	R 30, R31	Register RK73K2A 0 ΩJ	R30 is non-mount.
19	6	U1, U2, U3, U4, U5, U6	Transmission PE-67588	
20	1	U7	IC 74ACT04	
21	1	U8	IC μPD98408-T20	
22	1	U9	OSC 32 MHz	Non-mount
23	1	U10	Regulator MIC29150 3.3BT	
24	1	U11	OSC TC0-711A 32 MHz	
25	1	additional parts	Diode 1SS123-L	

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