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TV microcomputer

Auto-Adjustments for Couples Chassis Software

1.0 Abstract

The following article introduces and shows an example of how to use the Auto-Adjustments for Couples Chassis Software.

2.0 Introduction

The explanation of this issue is applied to the following condition:
Applicable MCU: M37150Mx-XXXFP
ASIC: M61260/264FP(MULTI), M61250/251FP(NTSC)

Software Version: Ver. 0.62 (*)
Program File Name: meap_ver062.HEX
Font File Name: COUP_FON8.HEP
Checksum: 1BD3h(0000h to 1FFFFh)

*Includes a software program list for MULTI chassis applications.

3.0 VIF VCO Adjustment

3.1 Purpose of Adjustment

The purpose of the VIF VCO adjustment is to tune the VIF VCO free-running frequency to the optimum frequency. Adjusting the VIF VCO minimizes the deviation of the VIF VCO free-running frequency and standard IF frequency.

3.2 Required Settings

MCU functions and ROM/RAM size, as well as ASIC registers, are set during auto-adjustment to the values shown in Tables 1 and 2, respectively.

Table 1.MCU Resources Used in Application

IC Type	Functions	ROM/RAM Size
MCU	Multi-master I^2C Bus interface	91 bytes / 22 bytes
	Timer interrupt	

Table 2.ASIC Register Settings

IC Type	No. / Part / Register/Bit	M61260/264		M61250/251	
		ADR	BIT	ADR	BIT
ASIC	VIF VCO ADJ	01h	Bit 0-Bit 5	01h	Bit 0-Bit 5
	AFT0 (READ)	01h	Bit 2	00h	Bit 2
	AFT1 (READ)	01h	Bit 3	00h	Bit 3
	VIF DEFEAT	07h	Bit 7	07h	Bit 7

VIF VCO can be adjusted through the following procedures via the I^2C Bus (Note 1).

1.Set VIF DEFEAT to ON (=1), via I^2C Bus (BUS).
2.Start adjustment period count (5 sec). If AFT0 = 1 during the count period, execute processes in Steps 3, 4, and 5. If AFT0 = 0 during the count period, execute the process in Step 6.
3.If AFT1 = 1, increment VIF VCO value (+1) via BUS. If AFT1 = 0, decrement VIF VCO value (–1) via BUS.
4.Examine AFT0 state after 20 msec Wait. When AFT0 = 0, VIF VCO holds the optional value.
5.If AFT0 does not go to 0 within adjustment period count (set in Step 2), set VIF VCO to initial value (= 31) via BUS.
6.Set VIF DEFEAT to OFF (= 1) via BUS, which completes the adjustment.

Note 1: The VIF VCO can also be adjusted by examining the AFT OUT voltage (adjust to approximately 1/2Vcc), which requires a pin configured for an A-D converter (on MCU) as well as other related settings. In comparison, this above method minimizes system resources.

3.3 Auto-Adjustment Procedure

Figure 1 shows the auto-adjust flowchart.

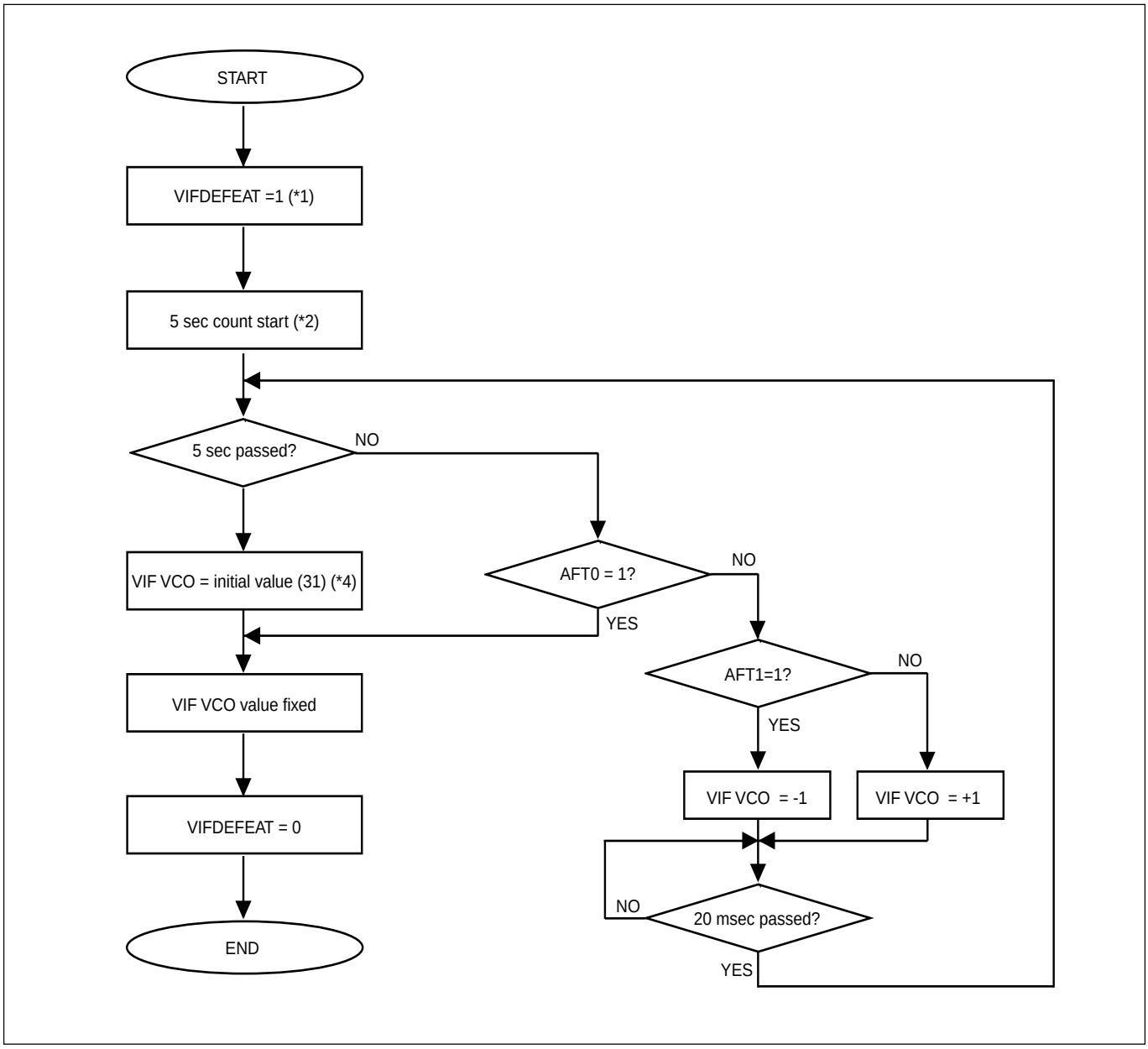

Figure 1.VIF VCO Auto-Adjust Flowchart

1: VIF DEFEAT setup process is not included in List 1 as a program list example.
2: The 5 sec. adjustment period is counted in the main routine (main cycle 10 msec). Not included in List 1.
3: Set 20 msec wait period after VIF VCO is updated. Counted in main routine. Not included in List 1.
4: VIF VCO initialization process during 5 sec time-out. Not included in List 1.

3.4 Auto-Adjustment Procedure

List 1 shows an example of a process program.

```
VIF_VCO_AUTO:
   X = [C_VIFVCO_AUTO]                ;5sec counter
      if Z==0                         ;Time out?   (5sec)
         if [f_V_AFT0] == 1           ;BUS AFT0 = 1 ?
            if [f_V_AFT1] == 1
               A =0                   ;BUS AFT1 = 1
               [F_UPDN]=0             ;Request Up
               JSR VCJ_DTUPDN_D       ;Transmit VIF VCO
            else
               A = 0                  ;BUS AFT1 = 0
               [F_UPDN]=1             ;Request Down
               JSR  VCJ_DTUPDN_D      ;Set VIF VCO
            endif
         else                         ;BUS AFT0 = 0 (adjustment completed)
            [C_VIFVCO_AUTO] = 1       ;Decrement by 1 after writing EEPROM
         endif
      endif
      RTS
```

List 1 VIF VCO Auto-Adjust Program Example

4.0 HVCO Adjustment

4.1 Purpose of Adjustment

The purpose of the HVCO adjust is to tune the horizontal free-running frequency to the optimum frequency. When the horizontal free-running frequency differs from the standard, adjusting the HVCO value minimizes the deviation of the horizontal free-running frequency and the standard horizontal oscillation frequency.

4.2 Required Settings

MCU functions and ROM/RAM size, as well as ASIC registers, are set during auto-adjustment to the values shown in Tables 3 and 4, respectively.

Table 3.MCU Resources Used in Application

IC Type	Functions	ROM/RAM Size
MCU	Multi-master I^2C Bus interface	206byte / 29byte
	Timer interrupt	
	VSYNC interrupt	

Table 4.ASIC Register Settings

IC Type	Part / No. / Register/Bit	M61260/264		M61250/251	
		ADR	BIT	ADR	BIT
ASIC	H VCO	10h	Bit 0-Bit 2	10h	Bit 0-Bit 2
	H FREE	13h	Bit 7	13h	Bit 7
	INTELLIGENT MONITOR	12h	Bit 4-Bit 7	12h	Bit 4-Bit 7
	MONITOR MSB	1Ah	Bit 6	1Ah	Bit 6

H VCO can be adjusted through the following procedures via the I^2C Bus.

1. Set H FREE to “1: set forced free-run mode via BUS.
2. Set INTELLIGENT MONITOR to “BGP (=4)” via BUS.
3. Set MONITOR MSB to “BGP (=1)” via BUS.
4. Set H VCO to the minimum value (=0) via BUS.
5. Start 2 msec count after VYSNC interrupt (Note 1).
6. Start 10 msec count after 2msec has passed. Count input pulses.
7. After 10 msec passes, if the count value equals the optimum value (Note 2), store the H VCO value at the optimum point in the RAM.
8. Repeat pulse determination process X times for each set value.
9. If the number of pulses does not reach the optimum value after X times, request renewal of the set value.
10. During X no. of re-tries, if the no. of optimum value matches exceeds the fixed no. of matches “Y” (X Y), the optimum value has been reached and value update is requested.
11. Increment H VCO by 1 via BUS.
12. Repeat Steps 3 through 10 until the H VCO maximum value (=7) is reached.
13. Set H VCO via BUS so that the count value is the optimum value.
14. If there are multiple optimum values for the H VCO, select the largest value via BUS
15. If the number of pulses does not reach the optimum value even after increasing the count to the maximum value, set H VCO to the initial value (=4) via BUS.
16. Set the following values: H FREE = 0, INTELLIGENT MONITOR = 0, and MONITOR MSB = 0. Transmit BUS, complete adjustment.

Notes 1: The 2 msec wait provides a period for the BGP output during the vertical blanking interval to stabilize.

2: The optimum count value of the auto-adjust setting in this software differs according to the standard oscillation frequency.

- **PAL standard horizontal oscillation frequency (15,625 Hz): optimum count value is 156 or 156 input pulses.**
- **NTSC reference horizontal oscillation frequency (15,734 Hz): optimum count value is 157 or 158 input pulses.**

4.3 Adjust Period

The optimum setting for each H VCO value is the optimum value resulting from the fixed number of input pulse count matches “Y” (X Y) during X number of re-tries. By increasing the number of examinations executed until the H VCO values are fixed, the accuracy of the adjustment can be greatly increased to prevent pulse-miscounts due to noise or other disturbances. The amount of time it took from start to completion of the auto-adjust process in actual examples, for both Y and X times, is shown in the table below.

Table 5.Comparison of Optimum Matches vs. Number of Examinations

No.of optimum matches(Y)/ No.of examinations(X) / Adjust results	**1 time/1 time** (Approximate)	**3 times/5 times** (Approximate)	**6 times/10 times** (Approximate)
Optimum value confirmed	174 msec	706 msec	1379 msec
Optimum value not confirmed	174 msec	747 msec	1462 msec

Although adjustment accuracy is improved by increasing the number of examinations until the set value is confirmed, this also increases processing time proportionately, making it necessary to create a balance between the desirable degree of accuracy and the total processing time. The actual measurements taken to obtain the above data with acceptable accuracy required 5 examination processes, 3 optimum value confirmations.

4.4 Auto-Adjustment Procedure

Figure 2 shows the auto-adjustment flowchart.

Figure 2.H VCO Auto-Adjust Flowchart

1: Uses TIMER 4 for 2 msec count. Not included in List 2 as program list example.
2: Uses TIMER 2 count source as external clock to count the number of input pulses. Not included in List 2.
3: Sets 10 msec pulse count period. Not included in List 2.

4.5 Program List

List 2 shows a process program example.

```
_jdg_count = X-1                                ;H VCO pulses - No. of examinations = X times
_ok_count = Y-1                                 ;H VCO pulses - No. of optimum matches = Y times
:HVCO_AUTO:
      if [f_ATHV_START] == _clr                 ;Adjust start BUS setting complete?
         [DT_HVCO] = 00                         ;H VCO= 0
         [BK_HVCO] = 00                         ;RAM for H VCO storage
         [OK_HVCO] = _ok_count                  ;Set no. of examinations
         [JG_HVCO] = _jdg_count                 ;Set no. of optimum matches
         [f_AHV_OK] = _clr                      ;Adjust OK/NG determination flag
         [f_wait_ms] = _clr                     ;10 msec Wait determination flag
         [f_ATHV_START] = _set                  ;Start set flag
         JSR SET_10_12_13                       ;Transmit ASIC BUS settings
         BRA  EXEC_AUTO
      else
         if [f_wait_ms] == _set                 ;10 msec Wait complete?
            A = [B_T2]                          ;TIMER2 event counter
            if A == 155 || A == 156             ;(MULTI) correct value?
               A = [OK_HVCO]                    ; Optimum no. of matches OK?
                  if z == _set
                     [BK_HVCO] = [DT_HVCO]      ;Update HVCO value
                     [f_AHV_OK] = _set          ;Updated value confirmed
                     A = [DT_HVCO]
                     if A < 7                   ;H VCO within max value?
                     [DT_HVCO] = ++A            ;H VCO +1
                     [OK_HVCO]=_ok_count        ;Set optimum no. of matches
                     [JG_HVCO]=_jdg_count       ;Set no. of examinations
                     BRA EXEC_AUTO
                     endif
                  else
                     A = [JG_HVCO]              ;No. of examinations OK?
                     if z == _clr
                     [OK_HVCO] = —[OK_HVCO]     ;No. of examinations -1
                     BRA RE_COUNT
                     endif
                     BRA NEXT_SET
                  endif
      else
NEXT_SET: A = [DT_HVCO]
         if A >= 7     ;H VCO = more than max. value?
            if [f_AHV_OK] == _clr               ;No request for update?
               [DT_HVCO] = 4                    ;Initialize H VCO value
            else
               [DT_HVCO] = [BK_HVCO]            ;Update H VCO
            endif
            [f_AUTO_HVCO] = _clr                ;H VCO auto-adjust completed
            JSR SET_10_12_13                    ;Transmit ASIC BUS settings
            RTS
         endif
         A = [JG_HVCO]                          ;Total no. of examinations completed?
         if z == _set
            [DT_HVCO] = ++[DT_HVCO]             ;H VCO +1
            [OK_HVCO]=_ok_count                 ;Reset optimum no. of matches
            [JG_HVCO]=_jdg_count                ;Reset no. of examinations
         else
RE_COUNT:    [JG_HVCO] =— [JG_HVCO]             ;No. of examinations -1
         endif
EXEC_AUTO:  JSR SET_10_12_13                    ;Transmit BUS data
         [B_T2] = 0                             ;Reset pulse counter
         [f_wait_ms] = 0                        ;Request 10 msec count
         [VSCE] = 1                             ;Enable V SYNC interrupt
         [VSCR] = 0                             ;Clear C SYNC interrupt request
      endif
      endif
      RTS
```

List 2. H VCO Auto-Adjust Program Example

5.0 S-TRAP Adjustment

5.1. Adjustment Purpose

The purpose of the S-TRAP (Sound Trap) adjustment is to tune the trap frequency to the optimum value in order to attenuate the voice signal overlaid on the picture signal. Adjusting the S-TRAP minimizes the deviation of the center frequency of the sound trap and the standard voice carrier frequency.

5.2 Required Settings

The MCU functions and ROM/RAM size, as well as ASIC registers, are set during auto-adjustment to the values shown in Tables 6 and 7, respectively.

Table 6.MCU Resources Used in Application

IC Type	Functions	ROM/RAM Size
MCU	Multi-master I^2C Bus interface	176 bytes / 29 bytes
	Timer interrupt	
	A-D converter	

Table 7.ASIC Register Settings

IC Type	No. / Part / Register/Bit	M61260/264		M61250/251	
		ADR	BIT	ADR	BIT
ASIC	S TRAP FINE ADJ	1Fh	Bit 7-Bit 5		
		20h	Bit 7		
	AFT DEFEAT	04h	Bit 6		
	VIF DEFEAT	07h	Bit 7		
	FSC FREE	09h	Bit 5		
	INTELLIGENT MONITOR	12h	Bit 4-Bit 7		
	SIF FREQ	14h	Bit 0-Bit 1		
	SIF 5.74	20h	Bit 2		
	STRAP TEST	25h	Bit 1		
	STRAP SELF1	25h	Bit 2		

S-TRAP can be adjusted through the following procedures via the I^2C Bus.
1. Set each value (Note 1) via I^2C Bus (BUS) (Note 1).
2. Set INTELLIGENT MONITOR to S TRAP OUTPUT LEVEL (=4) via BUS.
3. Set S-TRAP to minimum value (=0) via BUS.
4. Convert INTELLIGENT MONITOR output voltage (voltage =DT_ADVOL) after 10 msec (main counter).
5. Increment S-TRAP by 1 via BUS.
6. Convert INTELLIGENT MONITOR output voltage after 10 msec (main counter).
7. If current voltage is less than DT_ADVOL, update DT_ADVOL (DT_ADVOL = current voltage).
8. Repeat (15 times) Steps 2 to 7 until S-TRAP reaches maximum value (=15).
9. Set the value of S TRAP as the optimum value when INTELLIGENT MONITOR is at minimum voltage.
10. Transmit each setting (Note 1) via BUS, complete adjustment.

Note 1: BUS settings at adjust start and adjust completion are shown in Table 8 below.

Set Register \ value	At adjust start	At adjust completion
AFT DEFEAT	1	0
VIF DEFEAT	1	0
FSC FREE	1	0
INTELLIGENT MONITOR	4	0
SIF FREQ	2	*
SIF 5.74	0	*
STRAP TEST	1	0
STRAP SELF1	1	0
STRAP SELF2	0	

* Return to the value before setup.

Table 8.BUS Settings at Adjust Start and Completion

5.3 Auto-Adjust Procedure

Figure 3 shows an example of an auto-adjust flowchart.

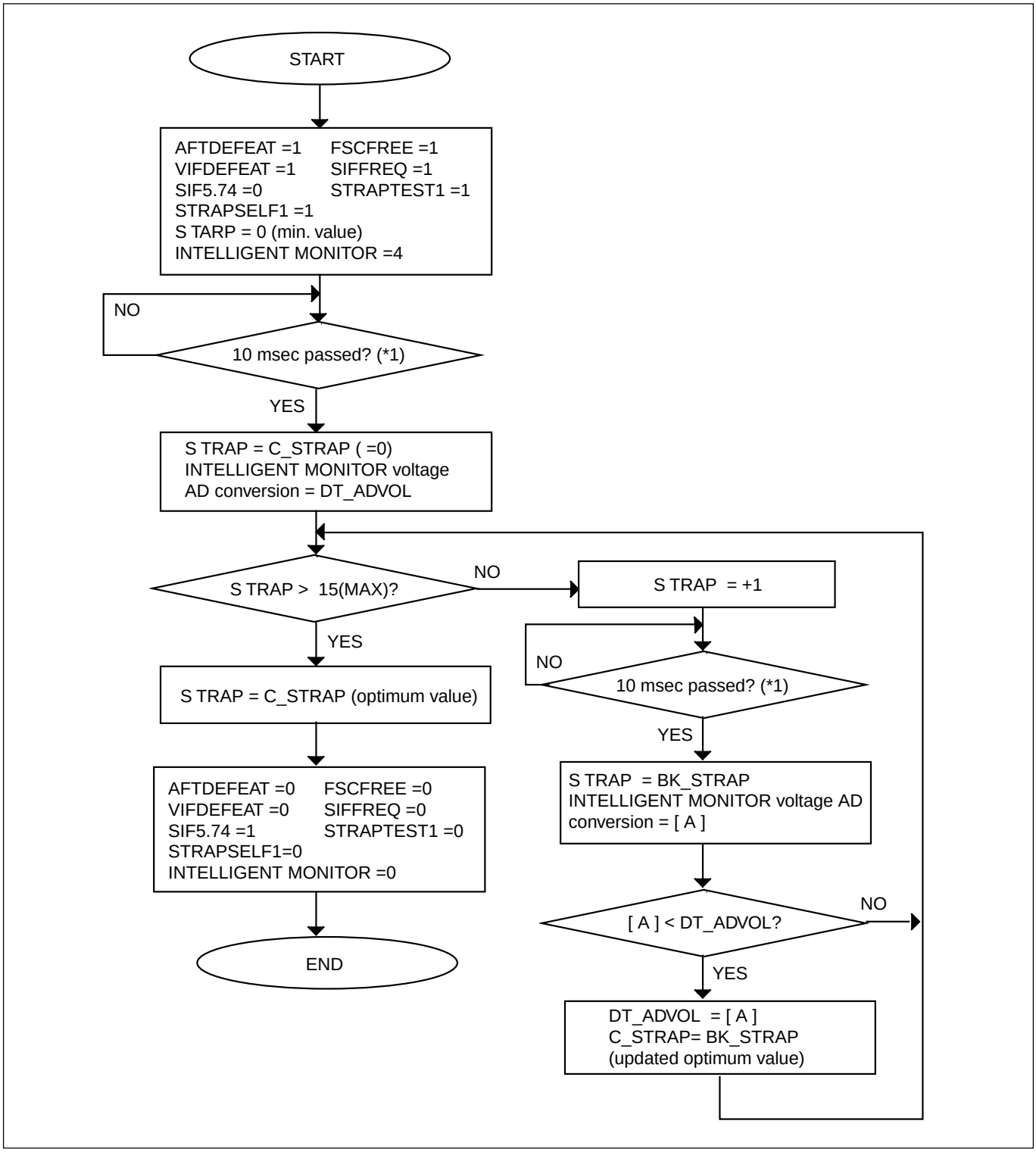

Figure 3.S-TRAP Auto-Adjust Flowchart

1. Set 10 msec wait period to occur after S-TRAP is updated. Counted in main routine. Not included in List 3 as program list example.

5.4 Program List

List 3 shows a process program example.

```
S_TRAP_AUTO:
        if [f_STRP_EXEC] == _clr                ; Adjust start BUS setting complete?
                [C_STRAP] = 00                  ; S TRAP = 0
                [BK_STRAP] = 00                 ; RAM for storing S TRAP
                [DT_ADVOL] = $7F                ; AD initial comparison value
                JSR SET_S_AUTO_ADR              ; Transmit BUS adjust start setting
                JSR SET_1F_20                   ; Transmit BUS S TRAP (=0)
                [f_STRP_EXEC] = _set            ; Adjust start BUS setting completed
                RTS
        endif
        JSR AD_READ                             ; INTELLIGENT MONITOR voltage AD conversion
        if A < [DT_ADVOL]                       ; Current voltage < comparison voltage?
                [DT_ADVOL] = A                  ; Update comparison voltage
                [BK_STRAP] = [C_STRAP]          ; Update optimum S TRAP value
    endif
    A = [C_STRAP]
    [C_STRAP] = ++A                             ; S TRAP + 1
    if A >= 16                                  ; STRAP > max. value?
                A = [BK_STRAP]                  ; STRAP at min. voltage
                A = A << 4
                [DT_STRAP] = A
                JSR SET_1F_20                   ; Update S TRAP (= optimum value)
                [f_STRP_EXEC] = _clr
                [f_AUTO_STRAP] = _clr           ; STRAP auto-adjust completed
                JSR SET_S_AUTO_ADR              ; Update normal BUS setting
    else
                JSR SET_1F_20                   ; Update BUS STRAP (=0)
    endif
    RTS
```

List 3. S-TRAP Auto-Adjust Program Example

* I^2C bus is a registered trademark of Philips.

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