Tsi577™
Design Notes

April 11, 2014

About this document

This document describes design notes for the Tsi577. Design notes are unique functional characteristics of the device that may or may not be described in the *Tsi577 User Manual* and should be reviewed when designing with the Tsi577. This document should also be used with the *Tsi577 Device Errat*a document.

Revision History

April 11, 2014

Added Packet discard on link partner failure

August 2009

There have been no technical changes to this document. The formatting was changed to reflect IDT.

January 2009

The following design note was added to this document, I2C Multi-master Clock Generation Issue.

August 2008

This is the first version of this document.

Design Notes

No.1. Port Power-down and Default Configuration

When a port is powered down, the port loses the port write destinationID that is stored for that particular port. Multicast settings, port write settings and other non-port specific registers return to their default power up settings after a port reset. After port reset, there is no way to determine that the configuration for a particular port is correct.

For example, if a port is shut down and then restored, the port write destination ID is reset to zero. The port write destination ID must be reset for the whole device after a port has been shut down and restored. Similarly, multicast settings for the entire device must be re-written when a port has been shut down and restored.

For more information on port power down registers that return to their default settings, refer to the *Tsi577 User Manual*.

Formal Status

No.2. Four 1x Links to 4x Port Training

Connecting four 1x links to a 4x port is not supported and may result in false lane alignment. The Tsi577 correctly detects alignment characters during the 4x training process. However, connecting a four lane 1x port to the Tsi577 while the Tsi577 is expecting to train with a 4x link partner causes the Tsi577 to remain in a PORT_UNINIT state and to never complete the training process in 1x mode.

This situation occurs because the Tsi577 is expecting align characters to be inserted on the four lanes by the link partner in order to complete the receive FIFO skew alignment process. Since the link partner is sending 1x links, it never inserts the align characters required to assist in the completion of the 4x link training process and since all four lanes are active, it never downgrades to 1x mode.

No.3. Default Port Transmit Electrical Characteristics May Not be Optimal

The Tsi577's default transmit amplitude and pre-emphasis settings may not be optimal in all applications, depending on the trace losses on the printed wiring board. This may result in a degradation in the Bit Error Rate (BER).

The BER can be improved by overwriting the power-on default values of the SRIO MAC x SerDes Configuration Global register to increase the output amplitude and apply more pre-emphasis to the output signal.

No.4. Masterless I^2C Bus Busy

This design note applies only to designs that require the Tsi577 to load registers from an I^2C EEPROM.

Because EEPROM devices do not have reset pins, if the Tsi577 is reset the EEPROM is unaffected and can continue to drive data. If the EEPROM continues to drive the I^2C data signal to 0, the Tsi577 is not able to load register values after reset is removed. Unexpected operation after a reset can result if register values cannot be loaded.

The *I^2C Specification (*for multiple master support) specifies that the I^2C bus is considered busy when the I^2C data signal is 0.

Hardware

To avoid this condition, design the reset of the Tsi577, and all other I^2C masters, so that the I^2C bus is always idle before asserting reset for the Tsi577 or any I^2C bus master.

Software

A software work around can be implemented to deal with this condition. The software work around has the following steps:

1. Determine that the I^2C bus is busy while there is no master
2. Issue a reset on the I^2C bus
3. Trigger a reset of the Tsi577 to perform the register value loading.

To implement the software work around, the Tsi577 must be configured to allow host processor access through RapidIO after reset using the power-up configuration pins.

For more information, refer to the *Tsi577 Hardware Manual*.

Testing

The software solution can be tested using the IDT JTAG Register Access Software (available at www.idt.com). This software includes scripts which recreate the Masterless I^2C Bus Busy condition.

Step 1: Masterless I²C Bus Busy

The registers listed in the following table must be read, and the register values must match those values described in the table, to determine that the bus is busy but there is no master.

Register Name	Register Offset	Register Value Descriptions
I²C Interrupt Status Register	1D11C	BL_OK and BL_FAIL bits are both 0
Internal I²C Status Register 1	1D300	0x00001F00 ANDed with the register value = 0
Internal I²C Status Register 2	1D3D0	0x0000000F ANDed with the register value = 0x0000000B
Internal I²C Status Register 3	1D3D4	Register Value = 0x0000021
Internal I²C Status Register 3, read 200 microseconds later	1D3D4	Register Value = 0x0000020
Internal I²C Status Register 4	1D3D8	0x00000E00 ANDed with the register value = 0x00000600

Step 2: Issue an I²C Bus Reset

Driving nine I²C clock cycles completes an interrupted transfer. An I²C clock cycle occurs whenever the I²C clock is driven low for at least five microseconds, and then is released to be high.

Multiple I²C EEPROM devices document driving nine I²C clock cycles for reset.

The register accesses listed in the following table drives I²C clock cycles to complete the interrupted I²C bus transfer. The sequence of writes in the table must be repeated nine times.

Register Name	Register Offset	Register Value
Internal I²C Control Register	1D3C0	Write 0x00000008, wait five microseconds.
Internal I²C Control Register	1D3C0	Write 0x00000000, wait five microseconds.

Step 3: Reset the Tsi577

There are a number of different methods to reset the Tsi577 documented in the *Tsi577 User Manual*. It is also possible for the host processor to reset the Tsi577 by system specific means.

No.5. I2C Multi-master Clock Generation Issue

When the Tsi577's I2C Interface is in a multi-master system, the I2C Interface does not generate a correct clock low period. The error can occur when all the following conditions are met:

- Both the external master and the I2C Interface are generating the clock
- The external master pulls the clock low two reference clock cycles before the I2C clock high timer expires

These conditions are possible only when an external master illegally attempts to use the bus when the Tsi577 is the bus master. In an expected configuration, two masters are unlikely to be operating at the same time. As well, experiencing this issue requires precise timing between the two masters. Because of these factors, this erratum is not likely to occur in a system.

This issue does not occur when theTsi577's I2C Interface is the only master.

No.6. Packet discard on link partner failure

The Tsi577 was designed to allow systems to continue operating when a link partner has been reset or otherwise failed. The device must perform two actions to allow a system to continue to operate:

- Notify the system host that a link partner has failed
- Discard packets destined for the failed link partner

Port-writes, triggered when the ERR_RATE_CNT bit in the RapidIO Port x Error Rate CSR exceeds the ERR_RFT bit threshold in the RapidIO Port x Error Rate Threshold CSR, should be used to notify the system host that a failure has occurred.

Two discard mechanisms should be used:

- Set the DROP_EN and STOP_FAIL_EN bits in the RapidIO Port x Control CSR to discard packets when ERR_RATE_CNT in the RapidIO Port x Error Rate CSR exceeds the ERR_RFT threshold in the RapidIO Port x Error Rate Threshold CSR, and the port is not in output error-stopped state. This is known as the "standard" discard mechanism.
- Enable the Dead Link Timer with the minimum time value in order to discard packets until the link has reinitialized.

Usually, systems follow a "fail stop" philosophy. Once a fault is detected on a link, all traffic destined for the link must be discarded until software recovers the link. Packet discard due to the Dead Link Timer will cease once the link has reinitialized. If the link partner has failed only temporarily, or the link has reinitialized due to a high temporary bit error rate, the standard discard mechanism will operate after the link has reinitialized. However, if the link partner was reset, the port will detect an ackID mismatch, enter output error-stopped state, and will be unable to discard packets.

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