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SH7280 Group

Transmission of Serial Data by the SCI in Asynchronous Mode

Introduction

This application note describes transmission of serial data by using the asynchronous transfer function of the serial communications interface (SCI). This application note is a summary for quick reference of information required in the design of user software.

Target Device

SH7285

Contents

1. Preface

1.1 Specifications

This sample application employs the asynchronous serial transfer function of the serial communications interface (SCI) to perform data transmission. Figure 1 shows an example of connection for transmission by the SCI in asynchronous mode.

- SCI0 is used.
- The communications format has an 8-bit data length, 1 stop bit, and no parity bit.
- The transmission interrupt is used to conduct asynchronous communications via SCI0. That is, the data-transfer controller (DTC) is activated by the transmit-data-empty interrupt.
- Once 32 bytes of data have been transmitted, operation for transmission is halted.

Figure 1 Connection Example for Transmission by the SCI in Asynchronous Mode

1.2 Module Used

- Serial communications interface (SCI0)

1.3 Applicable Conditions

- MCU SH7285
- Operating frequency Internal clock: 100 MHz
  Bus clock: 50 MHz
  Peripheral clock: 50 MHz
- C compiler SuperH RISC Engine Family C/C++ Compiler Package Ver.9.11
  (from Renesas Technology)

2. Description of the Sample Application

This sample application employs the transmit-data-empty interrupt (TXI) source of the SCI to handle the transmission of serial data in asynchronous mode.

2.1 Summary of MCU Module Used

In asynchronous mode, each transmitted or received character begins with a start bit and ends with a stop bit. Serial communication is synchronized in character units. The transmitting and receiving sections of the SCI are independent, so operations for transmission and reception can proceed simultaneously. Both the transmitter and receiver have a double-buffered structure so that data can be read or written during transmission or reception, which enables high-speed continuous data transfer.

In asynchronous serial communications, the communication line is normally held in the mark (high) state. The SCI monitors the line and starts serial communications when the line goes to the space (low) state, indicating a start bit.

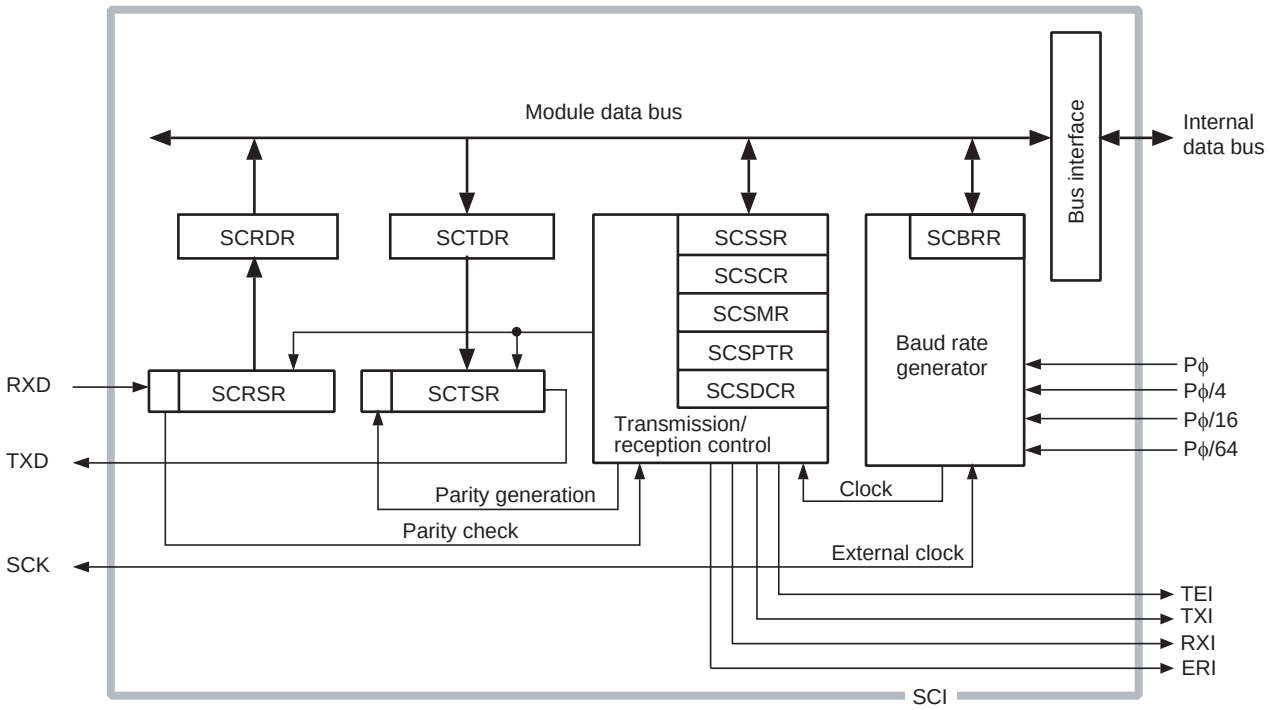
One serial character consists of a start bit (low), data (LSB first), parity bit (high or low), and stop bit (high), in this order.

For details on the SCI, please refer to the section on serial communication interface in the *SH7280 Group Hardware Manual.*

Table 1 gives an overview of serial communications in asynchronous mode. Figure 2 shows a block diagram of the SCI.

Table 1 Overview of Serial Data Communications in Asynchronous Mode

Item	Description
Number of interfaces	4 (SCI0, SCI1, SCI2, SCI4)
Clock sources	For internal clock: Pϕ, Pϕ/4, Pϕ/16, Pϕ/64 (Pϕ: peripheral clock) For external clock: input clock on the SCK pin
Data format	Transfer data length: 7 or 8 bits Order: LSB first and MSB first are selectable
Baud rate	For internal clock: 110 to 1,562,500 bps (Pϕ = 50 MHz) For external clock: up to 781,250 bps (Pϕ = 50 MHz, external input clock of 12.5000 MHz)
Error detection	Framing, parity, and overrun errors Breaks can also be detected.
Interrupt requests	Transmit-data-empty interrupt (TXI) Receive-data-full interrupt (RXI) Receive error interrupt (ERI) Transmit end interrupt (TEI)
Clock sources	Internal and external clocks are selectable • Internal clock When the internal clock has been selected, the clock from the baud-rate generator is used to operate the SCI and a clock signal at 16 times the frequency of the bit rate can be output. • External clock When the external clock has been selected, input of a clock signal at 16 times the frequency of the bit rate is required (The on-chip baud rate generator is not used.).



[Legend]
SCRSR: Receive shift register
SCRDR: Receive data register
SCTSR: Transmit shift register
SCTDR: Transmit data register
SCSMR: Serial mode register
SCSCR: Serial control register
SCSSR: Serial status register
SCBRR: Bit rate register
SCSPTR: Serial port register
SCSDCR: Serial direction control register

Figure 2 Block Diagram of the SCI

2.2 Description of the Sample Program

Table 2 shows the settings for the SCI communications function of this sample program, and figure 3 shows the operations in data transmission.

Table 2 Settings for Communications Function of the Sample Program

Item	Description
Module	SCI0
Communications mode	Asynchronous mode
Interrupt	Transmit-data-empty interrupt (TXI)
Transfer rate	38,400 bps
Number of data to be transmitted	32 bytes
Data length	8-bit data
Stop bit	1 stop bit
Parity	None
Bit order	LSB-first

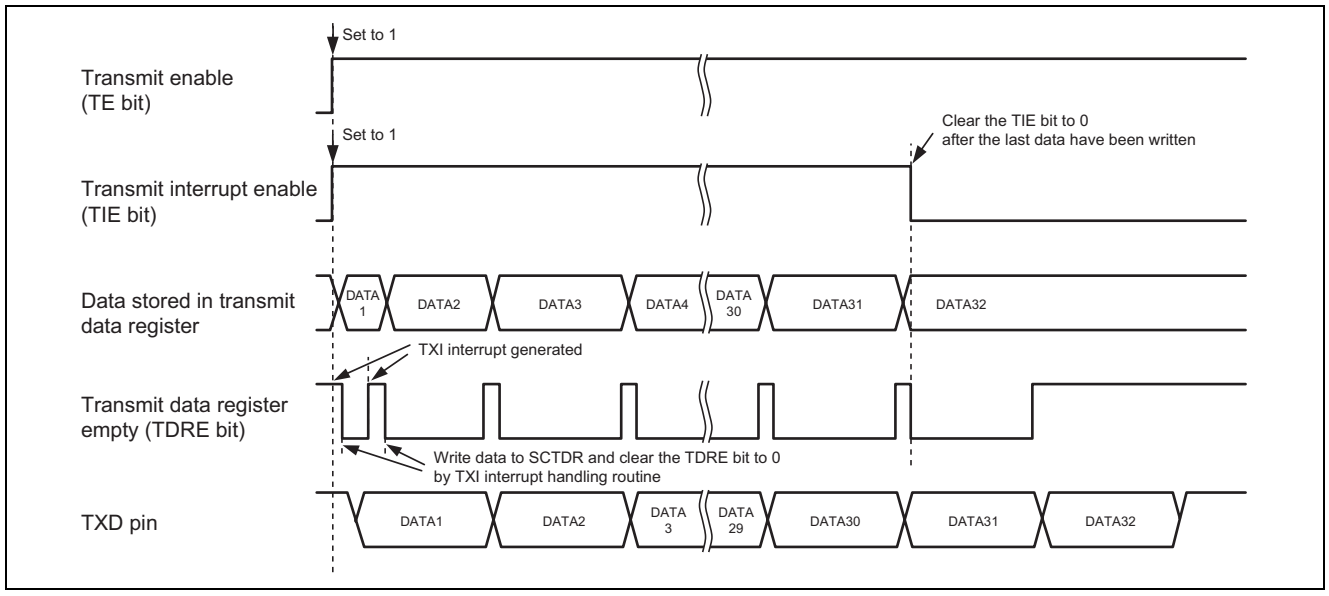


Figure 3 Operations for Data Transmission

2.3 Procedure for Setting Module Used

This section describes the procedure for setting up SCI0 for asynchronous mode operation.

Figure 4 shows the flow of processing by the sample program, figure 5 shows the flow of settings for release from module-standby mode, figure 6 shows the flow for setting up the pin function controller, figure 7 shows the flow for initialization of data transmission in asynchronous mode, and figure 8 shows the flow for handling transmit interrupts in asynchronous mode. For details on the settings of individual registers, see the *SH7280 Group Hardware Manual*.

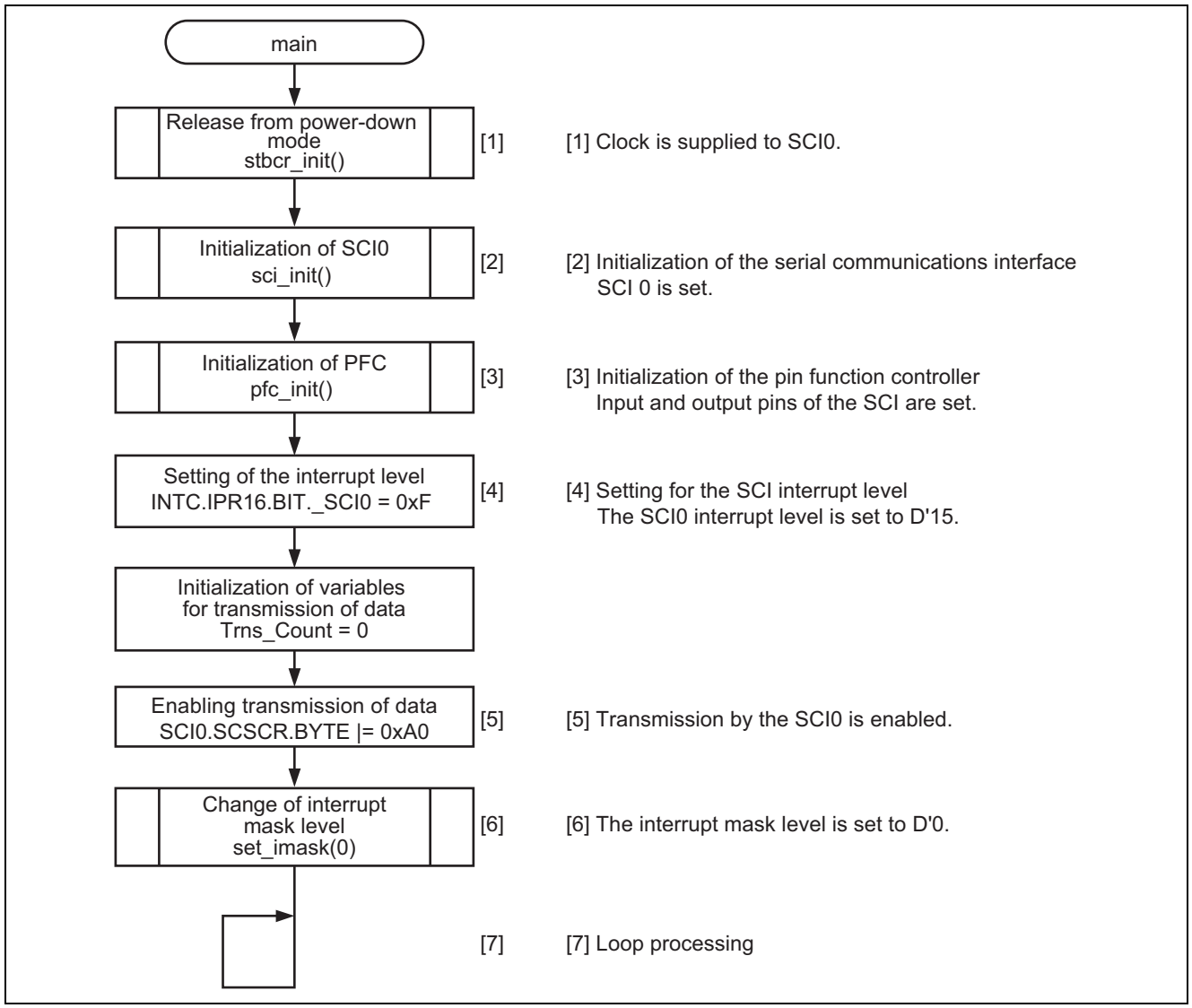


Figure 4 Flow of Processing by the Sample Program

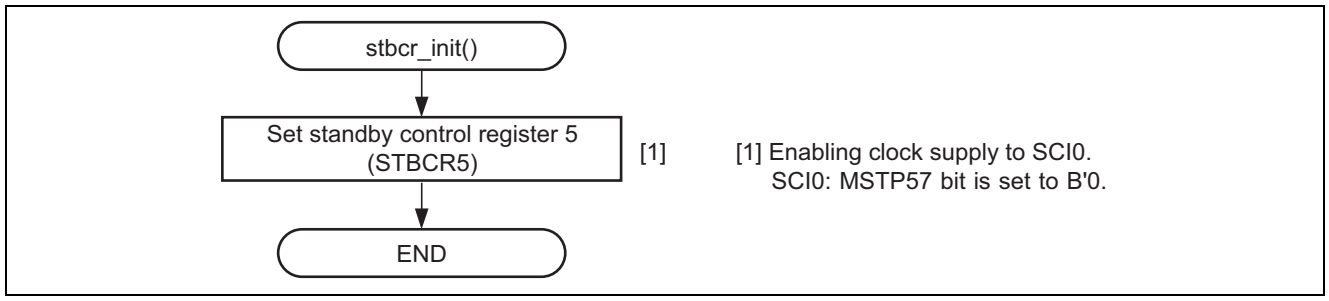


Figure 5 Flow of Settings for Release from Module-Standby Mode

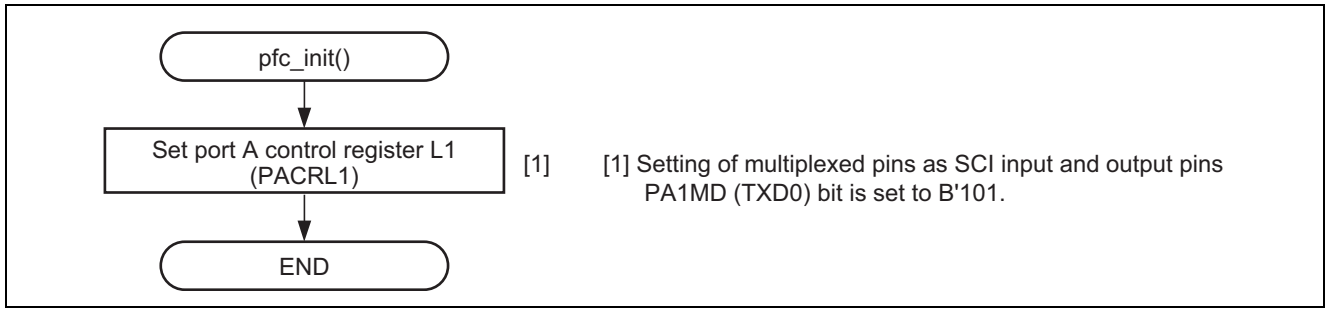


Figure 6 Flow for Setting up the Pin Function Controller

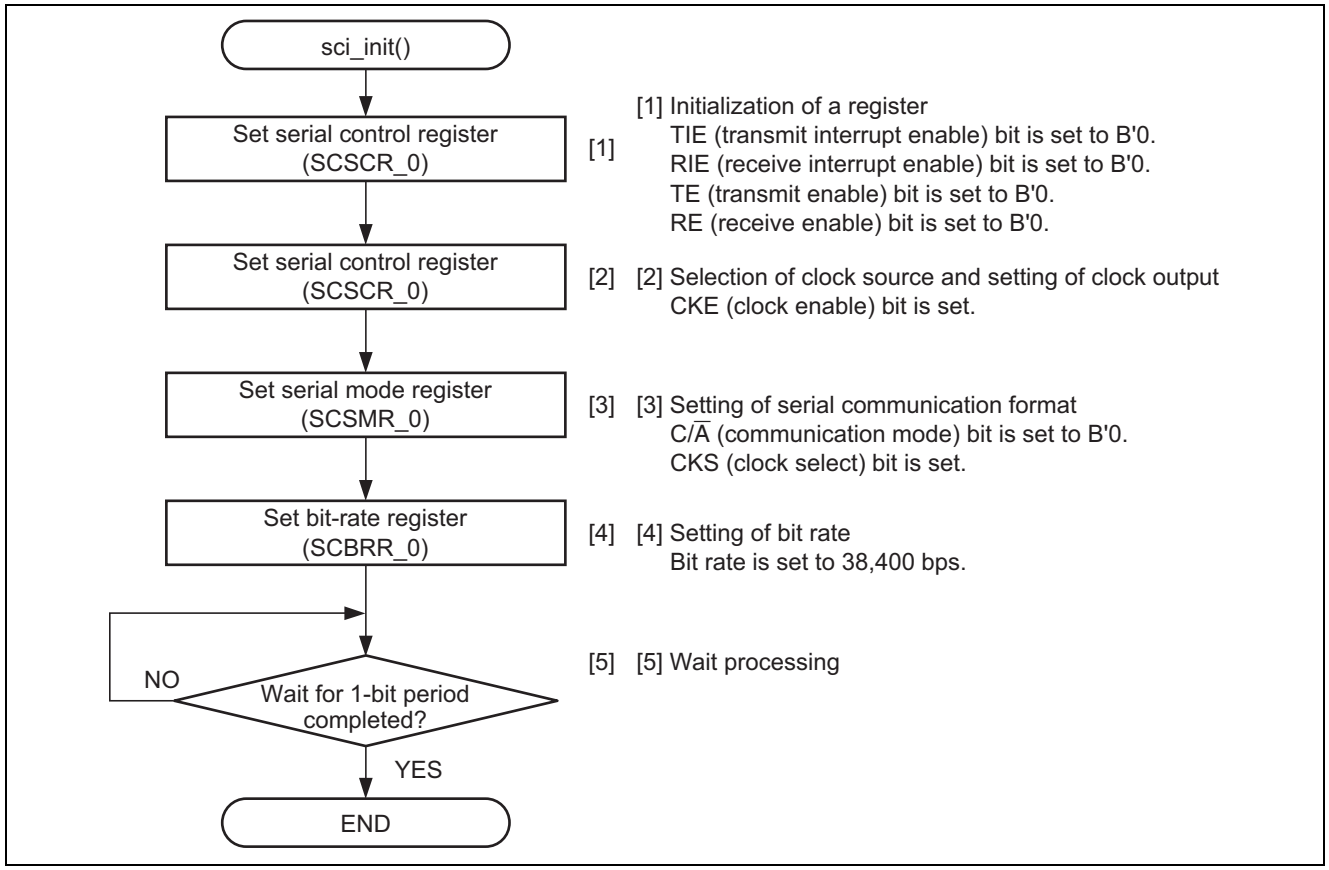


Figure 7 Flow for Initialization of Data Transmission in Asynchronous Mode

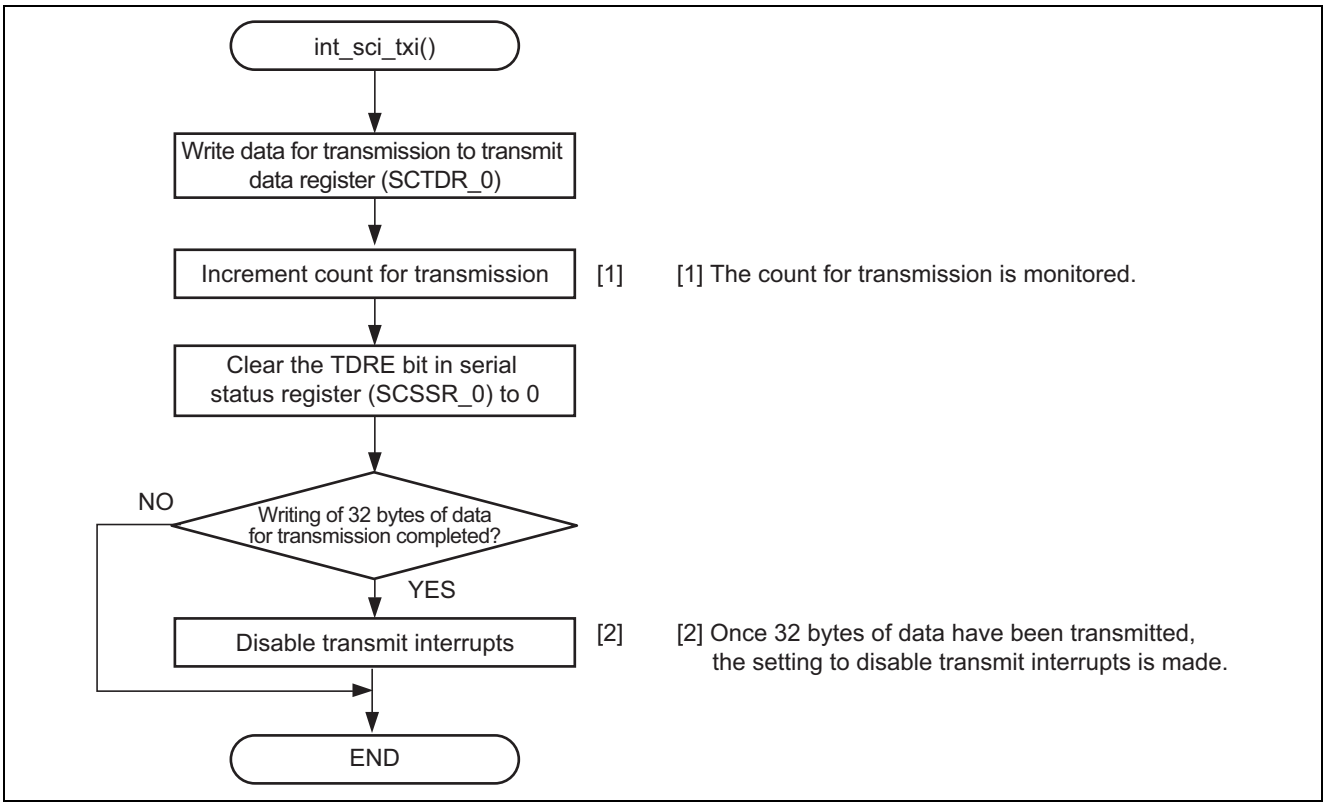


Figure 8 Flow for Handling Transmit Interrupts in Asynchronous Mode

2.4 Procedure for Processing by the Sample Program

In this sample program, character strings are transmitted after initialization of SCI0 for data transmission in asynchronous mode.

2.4.1 Clock Pulse Generator (CPG)

Table 3 gives settings for the register of the clock pulse generator in the sample program.

Table 3 Settings for Register in Clock Pulse Generator

Register Name	Address	Setting	Description
Frequency control register (FRQCR)	H'FFFE0010	H'0101	STC [2:0] = B'001: × 1/2 (Bϕ) IFC [2:0] = B'000: × 1 (Iϕ) PFC [2:0] = B'001: × 1/2 (Pϕ)

2.4.2 Standby Control Register

Table 4 gives settings for the standby control register in the sample program.

Table 4 Settings for Standby Control Register

Register Name	Address	Setting	Description
Standby control register 5 (STBCR5)	H'FFFE0418	H'7F	MSTP57 = B'0: SCI0 operates

2.4.3 Interrupt Controller (INTC)

Table 5 gives settings for the register of the interrupt controller in the sample program.

Table 5 Settings for Register of Interrupt Controller

Register Name	Address	Setting	Description
Interrupt priority registers 16 (IPR16)	H'FFFE0C14	H'F000	IPR16 [15:12] = H'F: SCI0 is at a level 15

2.4.4 Pin Function Controller (PFC)

Table 6 gives settings for the register of the pin function controller in the sample program.

Table 6 Settings for Register of Pin Function Controller

Register Name	Address	Setting	Description
Port A control register L1 (PACRL1)	H'FFFE3816	H'0050	PA1MD [2:0] = B'101: TXD0 output

2.4.5 Serial Communications Interface

Table 7 gives settings for the registers of the SCI in the sample program.

Table 7 Settings for SCI Register

Register Name	Address	Setting	Description
Serial mode register (SCSMR_0)	H'FFFE8000	H'00	C/$\overline{A}$ = B'0: Asynchronous mode CHR = B'0: 8-bit data PE = B'0: Disables adding and checking of parity bits STOP = B'0: 1 stop bit CKS [1:0] = B'00: Pϕ clock
Bit rate register (SCBRR_0)	H'FFFE8002	D'40	Asynchronous mode Bit rate: 38400 (bit/s) *[1]
Serial control register (SCSCR_0)	H'FFFE8004	H'00	Initialization TIE = B'0: Disables transmit-data-empty interrupt (TXI) request RIE = B'0: Disables receive-data-full interrupt (RXI) and receive error interrupt (ERI) requests TE = B'0: Disables transmission of data RE = B'0: Disables reception of data
			At the time of setting Asynchronous mode CKE [1:0] = B'00: Internal clock, and the SCK pin is used as an input pin
		H'A0	When transmitting and receiving operations are enabled TIE = B'1: Enables transmit-data-empty interrupt (TXI) request TE = B'1: Enables transmission of data
Serial status register (SCSSR_0)	H'FFFE8008	H'84	Initial value TDRE = B'1: Transmit-data-register-empty flag TEND = B'1: Transmit end flag
		H'04	At the time of setting TDRE flag is cleared to 0.

Note: 1. For details on bit rate settings, see the table of bit rates and SCBRR settings in the section on the serial communication interface of the *SH7280 Group Hardware Manual*.

3. Documents for Reference

- Software Manual
  SH-2A, SH2A-FPU Software Manual
  The most up-to-date version of this document is available on the Renesas Technology Website.

- Hardware Manual
  SH7280 Group Hardware Manual
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Revision Record

		Description	
Rev.	Date	Page	Summary
1.00	Aug.27.08	—	First edition issued

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