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SH7137 Group

Transmission of Serial Data by the SCI in Asynchronous Mode

Introduction

This application note describes transmission of serial data by using the asynchronous transfer function of the serial communication interface (SCI). This application note is a summary for quick reference of information required in the design of user software.

Target Device

SH7137

Contents

1. Preface

1.1 Specifications

In this sample task, data are transmitted by using the asynchronous serial data communications function of the SCI.

Figure 1 shows an example of connection for transmission by the SCI in asynchronous mode.

- SCI 1 is used.
- The communications format has an 8-bit data length, 1 stop bit, and no parity bit.
- The transmission interrupt is used to conduct asynchronous communications on SCI 1. That is, the data-transfer controller (DTC) is activated by the transmit-data-empty interrupt.
- Once 32 bits of data have been transmitted, operation for transmission is halted.

Figure 1 Connection Example for Transmission by the SCI in Asynchronous Mode

1.2 Module Used

- Serial communication interface (SCI 1)

1.3 Applicable Conditions

• MCU	SH7137
• Operating frequency	Internal clock: 80 MHz Bus clock: 40 MHz Peripheral clock: 40 MHz
• C compiler	SuperH RISC Engine Family C/C++ Compiler Package Ver.9.11 from Renesas Technology

2. Description of the Sample Application

The sample program uses interrupt sources of the SCI and a transmit-data-empty interrupt (TXI) to transmit serial data in asynchronous mode.

2.1 Operational Overview of Module Used

In asynchronous mode, each transmitted or received character begins with a start bit and ends with a stop bit. Serial communication is synchronized one character at a time. The transmitting and receiving sections of the SCI are independent, so full duplex communication is possible. Both the transmitter and receiver have a double-buffered structure so that data can be read or written during transmission or reception, enabling continuous data transfer.

In asynchronous serial communication, the communication line is normally held in the mark (high) state. The SCI monitors the line and starts serial communication when the line goes to the space (low) state, indicating a start bit.

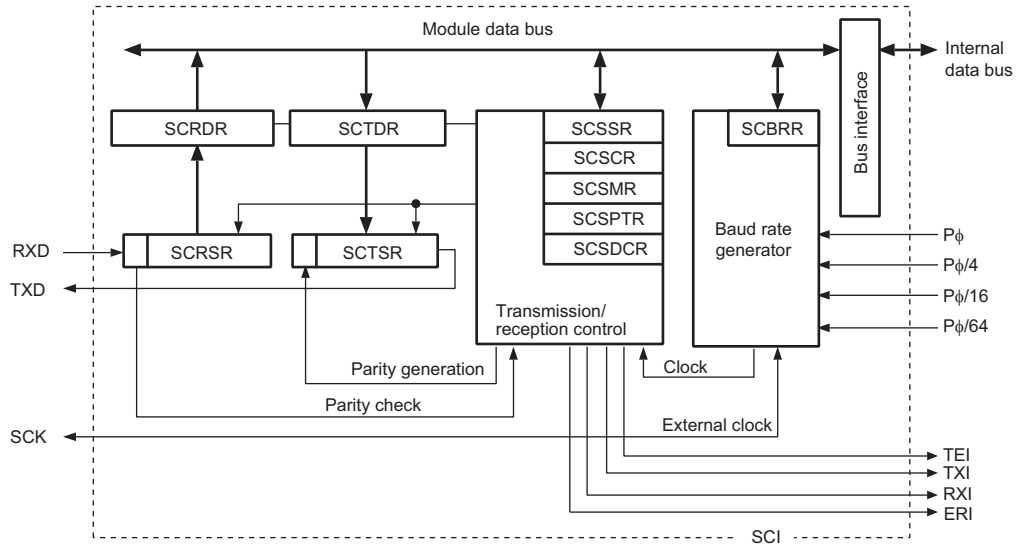
One serial character consists of a start bit (low), data (LSB first), parity bit (high or low), and stop bit (high), in that order.

For details on the SCI, see the section on serial communication interface in the *SH7137 Group Hardware Manual*.

Table 1 gives an overview of communications in asynchronous mode and figure 2 shows a block diagram of the SCI.

Table 1 Overview of Serial Data Communications in Asynchronous Mode

Item	Description
Number of interfaces	3 (SCI0, SCI1, SCI2)
Clock source	For internal clock: Pϕ, Pϕ/4, Pϕ/16, Pϕ/64 (Pϕ: peripheral clock) For external clock: input clock on pin SCK
Data format	Data length: 7 or 8 bits Order: LSB first or MSB first
Baud rate	For internal clock: 110 bps to 1.25 Mbps (Pϕ = 40 MHz) For external clock: up to 625 kbps (P = 40 MHz, external input clock of 10.0000 MHz)
Error detection	Framing, parity, and overrun errors Break can also be detected.
Interrupt request	Transmit-data-empty interrupt (TXI) Receive-data-full interrupt (RXI) Receive error interrupt (ERI) Transmit end interrupt (TEI)
Clock sources	Internal or external clock • Internal clock When the internal clock has been selected, the clock from the baud-rate generator is used to operate the SCI and a clock signal at 16 times the frequency of the bit rate can be output. • External clock When the external clock has been selected, input of a clock signal at 16 times the frequency of the bit rate is required (internal baud rate generator is not used).



[Legend]
SCRSR : Receive shift register
SCRDR : Receive data register
SCTSR : Transmit shift register
SCTDR : Transmit data register
SCSMR : Serial mode register
SCSCR : Serial control register
SCSSR : Serial status register
SCBRR : Bit rate register
SCSPTR: Serial port register
SCSDCR: Serial direction control register

Figure 2 Block Diagram of the SCI

2.2 Operation of the Sample Program

Table 2 gives settings for SCI communications and figure 3 shows the timing of operations for data transmission.

Table 2 Settings for Communications Function in the Sample Program

Item	Description
Module	SCI 1
Communications mode	Asynchronous mode
Interrupts	Transmit-data-empty interrupt (TXI)
Transfer rate	19,200 bps
Number of data to be received and transmitted	32 bytes
Data length	8-bit data
Stop bit	1 stop bit
Parity	None
Bit order	LSB-first

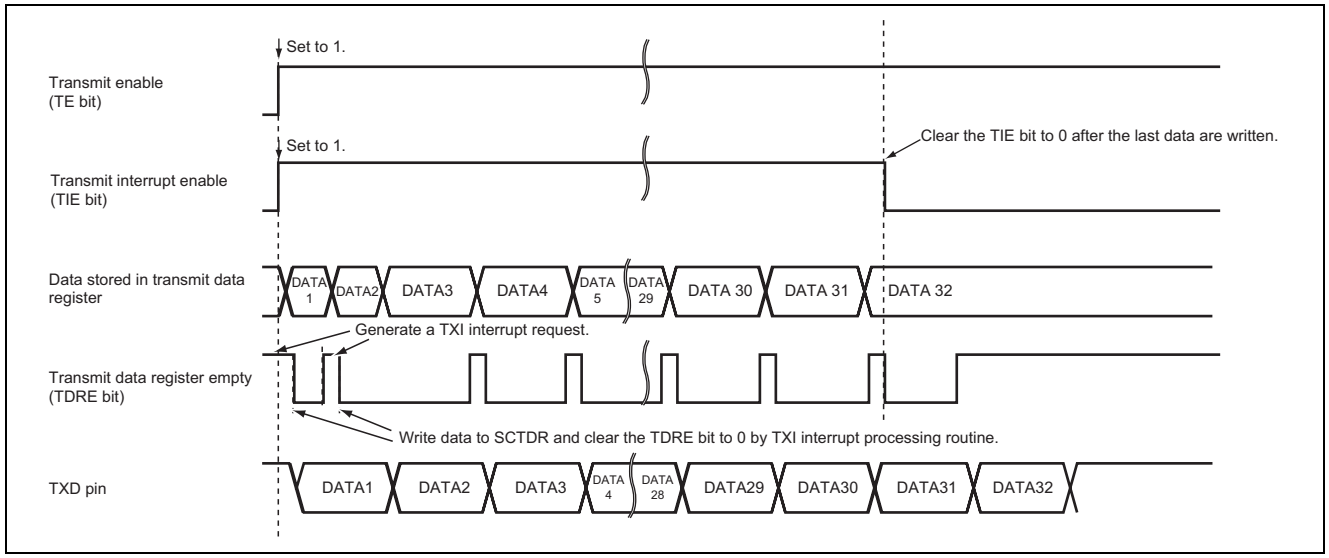


Figure 3 Timing of Operations for Data Transmission

2.3 Procedure for Setting Module Used

This section describes the procedure for setting up SCI 1 for asynchronous mode operation.

Figure 4 shows the flow of processing by the sample program, figure 5 shows the flow of settings for release from module-standby mode, figure 6 shows the flow for setting up the pin function controller, and figure 7 shows the flow for initialization of data transmission in asynchronous mode. Furthermore, figure 8 shows the flow for handling transmit interrupts in asynchronous mode. For details on the settings of individual registers, see the *SH7137 Group Hardware Manual*.

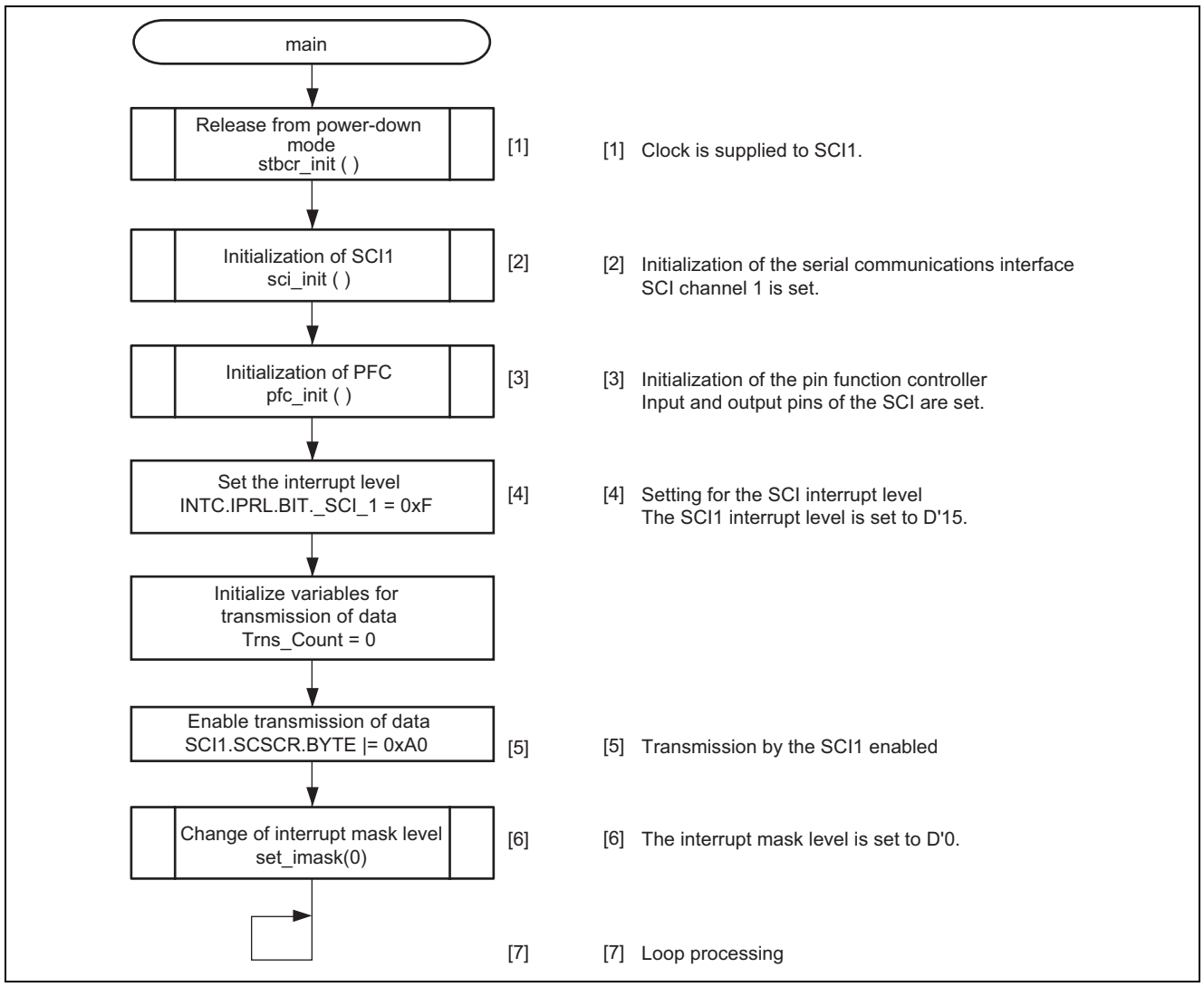


Figure 4 Flow of Processing by the Sample Program

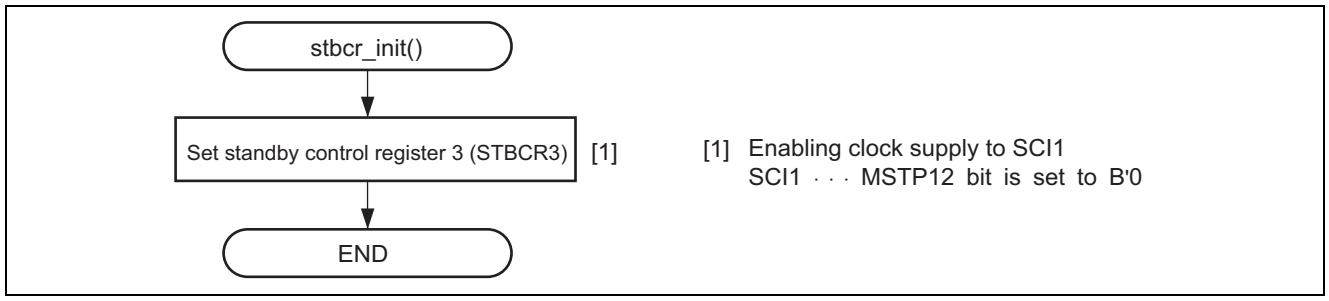


Figure 5 Flow of Settings for Release from Module-Standby Mode

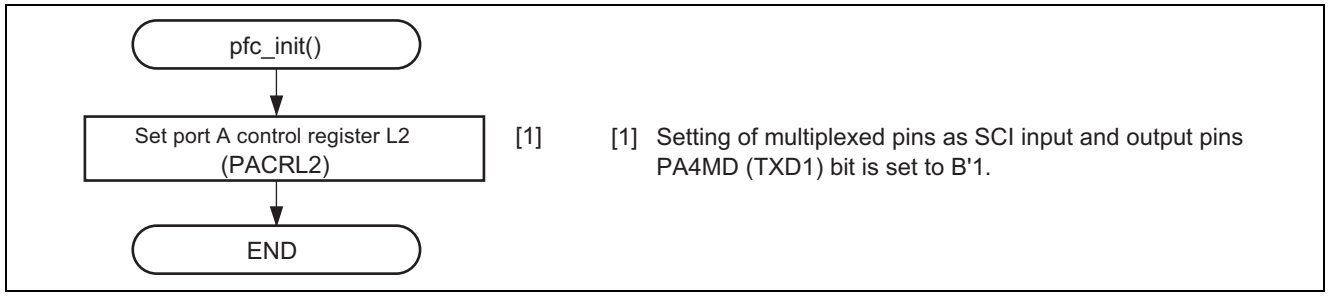


Figure 6 Flow for Setting up the Pin Function Controller

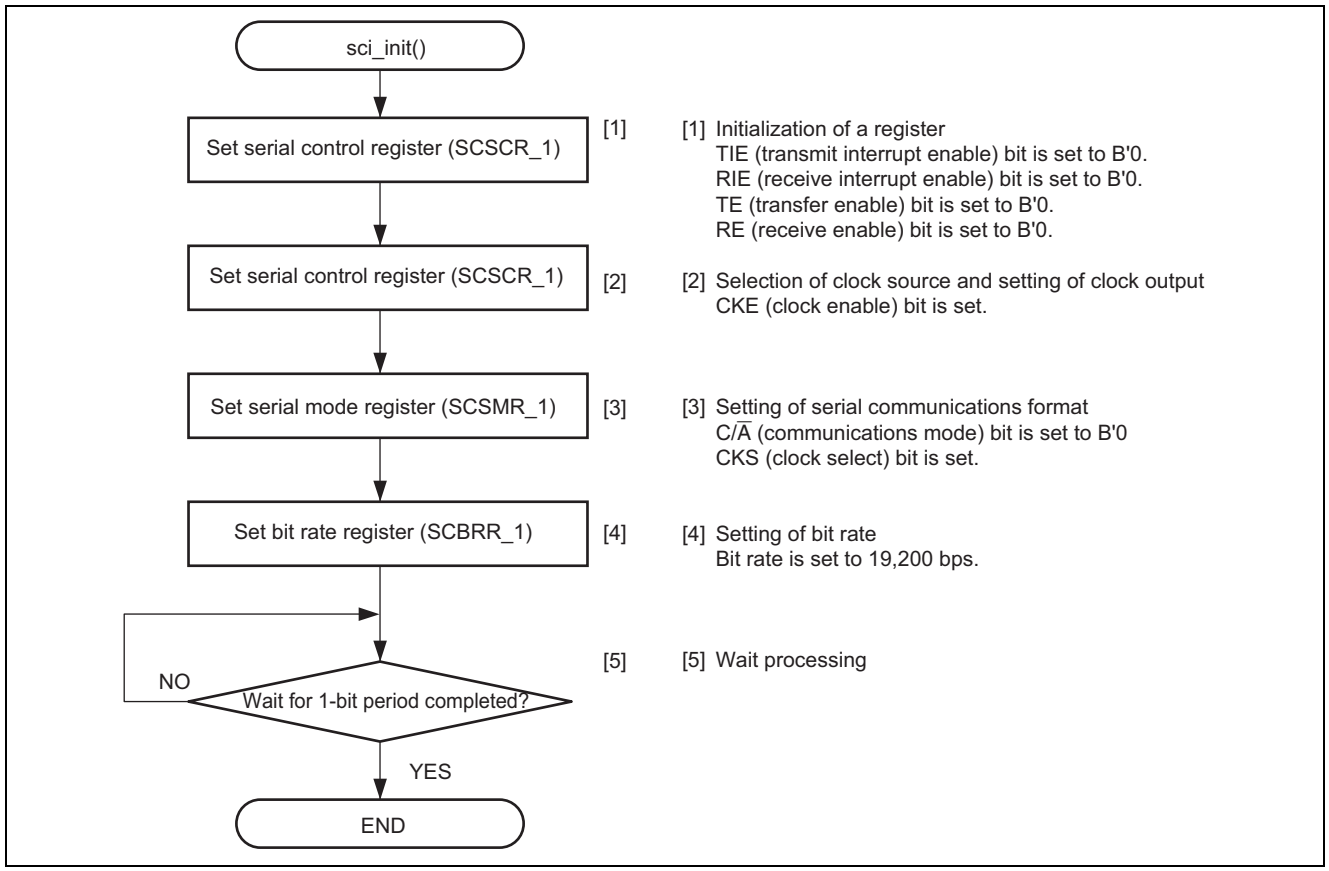


Figure 7 Flow for Initialization of Data Transmission in Asynchronous Mode

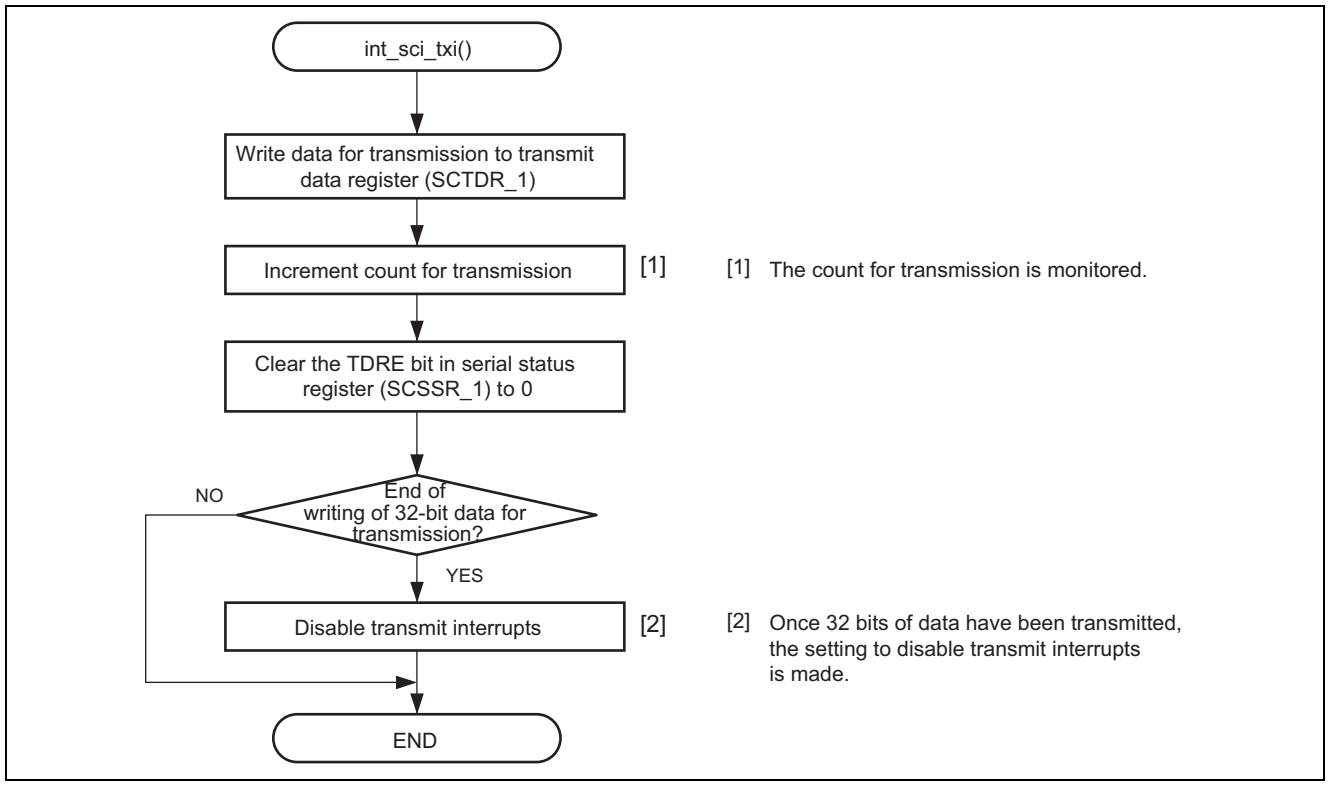


Figure 8 Flow for Handling Transmit Interrupts in Asynchronous Mode

2.4 Processing Sequence of the Sample Program

In this sample program, character strings are transmitted after initialization of SCI 1 for data transmission in asynchronous mode.

2.4.1 Clock Pulse Generator (CPG)

Table 3 gives settings for the register of the clock pulse generator in the sample program.

Table 3 Settings for Register in Clock Pulse Generator

Register Name	Address	Setting	Description
Frequency control register (FRQCR)	H'FFFFE800	H'0241	IFC[2:0] = B'000: × 1 (Iϕ) BFC[2:0] = B'001: × 1/2 (Bϕ) PFC[2:0] = B'001: × 1/2 (Pϕ) MIF[2:0] = B'000: × 1 (MIϕ) MPFC[2:0] = B'001: × 1/2 (MPϕ)

2.4.2 Standby Control Register

Table 4 gives settings for the standby control register in the sample program.

Table 4 Settings for Standby Control Register

Register Name	Address	Setting	Description
Standby control register 3 (STBCR3)	H'FFFFE806	H'EF	MSTP12 = B'0: SCI1 operates

2.4.3 Interrupt Controller (INTC)

Table 5 gives settings for the interrupt control register in the sample program.

Table 5 Settings for Interrupt Control Register

Register Name	Address	Setting	Description
Interrupt priority register L (IPRL)	H'FFFFE992	H'0F00	IPR[11:8] = H'F: SCI1 is at a level 15

Note: Interrupt priorities of RXI_1 and TXI_1 are in order of offset address in the vector table for interrupts. For details on interrupt priorities, see the description of the interrupt exception handling vector table in the section on the interrupt controller of the *SH7137 Group Hardware Manual*.

2.4.4 Pin Function Controller (PFC)

Table 6 gives settings for the register of the pin function controller in the sample program.

Table 6 Settings for Pin Function Control Register

Register Name	Address	Setting	Description
Port A control register L2 (PACRL2)	H'FFFFD114	H'0001	PA4MD[2:0] = 1: TXD1 output

2.4.5 Serial Communication Interface

Table 7 gives settings for registers of the SCI in the sample program.

Table 7 Settings for SCI Register

Register Name	Address	Setting	Description
Serial mode register (SCSMR_1)	H'FFFFC080	H'00	C/$\overline{A}$ = B'0: Asynchronous mode CHR = B'0: 8-bit data PE = B'0: Disables appending and checking of parity bits STOP = B'0: 1 stop bit CKS [1:0] = B'00: Pϕ clock
Bit rate register (SCBRR_1)	H'FFFFC082	D'64	Asynchronous mode Bit rate: 19,200 (bit/s)[*1]
Serial control register (SCSCR_1)	H'FFFFC084	H'00	Initialization TIE = B'0: Disables transmit-data-empty interrupt (TXI) request RIE = B'0: Disables receive-data-full interrupt (RXI) and receive error interrupt (ERI) requests TE = B'1: Disables transmission of data RE = B'0: Disables reception of data
			At the time of setting Asynchronous mode CKE[1:0] = B'00: Internal clock and the SCK pin are used for an input pin
		H'A0	Enabling transmission of data TIE = B'1: Enables transmit-data-empty interrupt (TXI) request TE = B'1: Enables transmission of data
Serial status register (SCSSR_1)	H'FFFFC088	H'84	Initial value TDRE = B'1: Transmit-data-empty flag TEND = B'1: Transmit end flag
		H'04	At the time of setting All flags are cleared.

Note: * For details on bit rate settings, see the table of bit rates and SCBRR settings in the section on the serial communication interface in the *SH7137 Group Hardware Manual*.

3. Documents for Reference

- Software Manual
  SH-1/SH-2/SH-DSP Software Manual
  The most up-to-date version of this document is available on the Renesas Technology Website.
- Hardware Manual
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Rev.	**Date**	**Page**	**Summary**
1.00	May.20.08	—	First edition issued

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