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April 1st, 2010
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H8SX Family

Transfer between Synchronous DRAM and External SRAM with EXDMAC (Offset Addition)

Introduction

Data are transferred by the EXDMAC function from the synchronous DRAM area (hereafter referred to as SDRAM) to the SRAM area using normal transfer mode where the transfer address is updated by adding a specified offset.

Use of EXDMAC enables reducing CPU loads and transferring data between external memories.

Moreover, address update by offset addition enables transferring data at addresses that are not placed continuously.

This program can be used on other H8SX Series that include the same I/O registers as those of the H8SX/1668R Group. Note that a part of the functions of those series may be changed, or new functions may be added to the series. Therefore, be sure to check their manuals for details. Perform thorough evaluation when using this application note.

Target Device

H8SX/1668R

Contents

1. Specifications

An overview of operation in this application note is given in figure 1, and connections between the external memory and the CPU are shown in figure 2.

The operation in this application note is explained as follows:

- EXDMAC is activated on the falling edge of the $\overline{\text{EDREQ}}$ pin.
- TPU compare match output is used as the input to the $\overline{\text{EDREQ}}$ pin.
- Offset addition is selected for updating the transfer source/destination address.
- EXDMAC uses offset addition (+2) to update addresses.
- EXDMAC transfers 128-byte data from the SDRAM area to the SRAM area.
- SDRAM and SRAM use area 2 and area 4, respectively.
- After an EXDMAC transfer, the source and destination data are compared, and the result of the comparison is output to an I/O port.

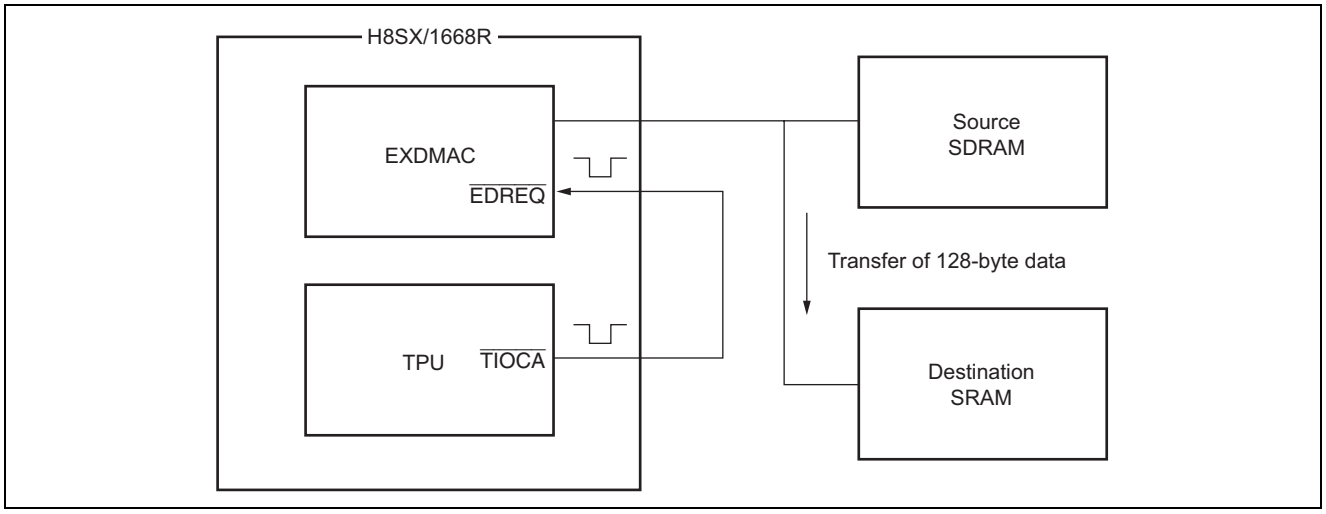

Figure 1 Operation Overview

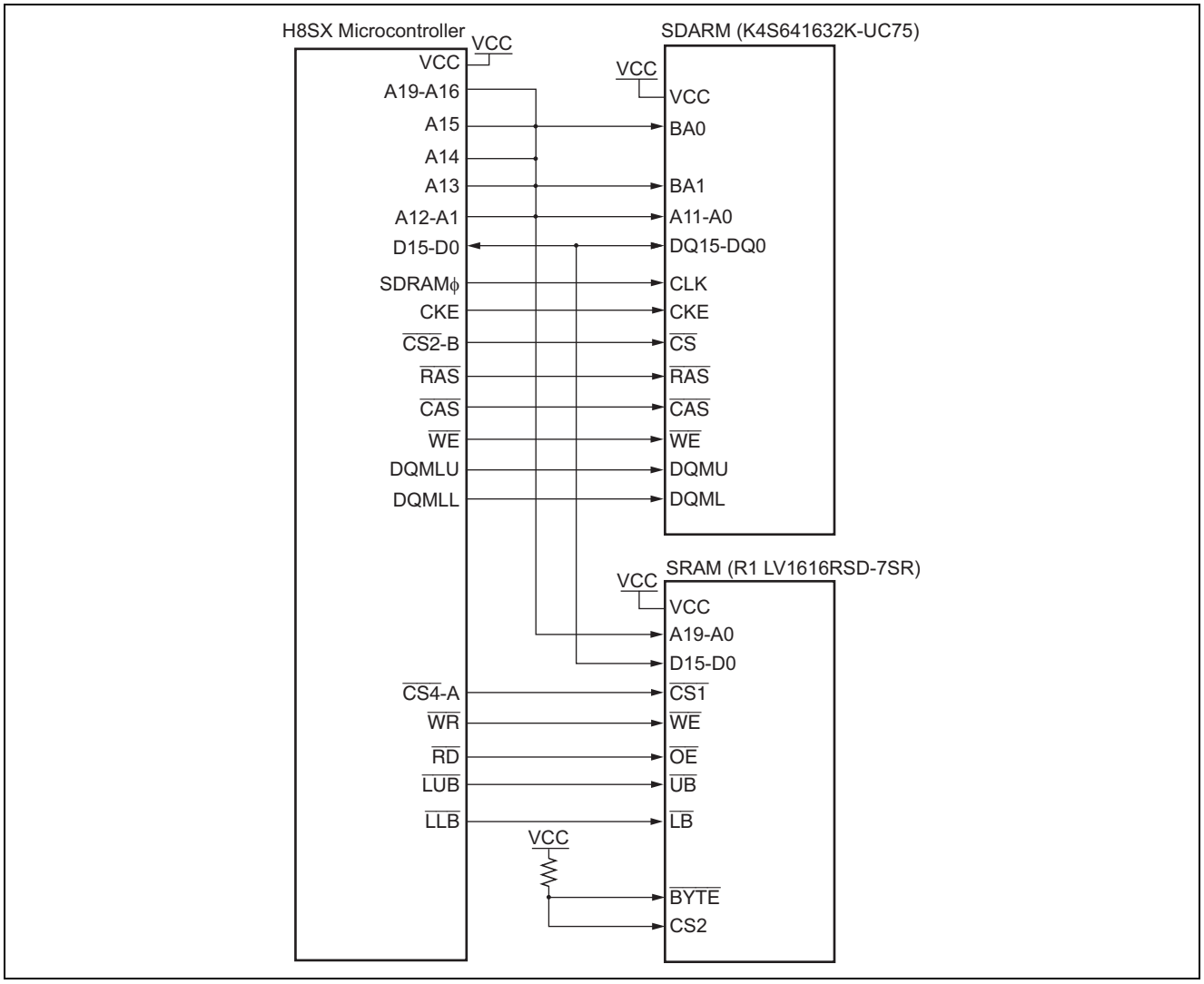

Figure 2 Connections between External Memory and CPU

EXDMAC transfer settings are listed in table 1.

In addition, comparison of data transferred is listed in table 2.

Table 1 EXDMAC Transfer Settings

Item	Setting
EXDMAC transfer request	External request mode
Bus mode	Cycle steal mode
Transfer mode	Normal transfer mode
Address mode	Dual address mode
Transfer size	Byte size
Source/destination address update	Offset addition
Extended repeat area	Not specified

Table 2 Comparison of Data Transferred

Comparison Result	Output Value (using port 3)
Matched	H'55
Unmatched	H'FF

2. Applicable Conditions

Table 3 Applicable Conditions

Item	Detail	
Operation Frequency	Input clock	: 12.5 MHz
	System clock (Iϕ)	: 50 MHz (12.5 MHz multiplied by 4)
	Peripheral module clock (Pϕ)	: 25 MHz (12.5 MHz multiplied by 2)
	External bus clock (Bϕ)	: 50 MHz (12.5 MHz multiplied by 4)
Operation Voltage	3.3 V	
Operation Mode	Mode 6 (MD3 = 1, MD2 = 1, MD1 = 1, MD0 = 0, MD_CLK = 0)	
External Memory	• SDRAM (area 2)	: K4S641632K-UC75
	• SRAM (area 4)	: R1LV1616RSD-7SR
Development Tool	High-performance Embedded Workshop (HEW) Ver.4.03.00	
C/C++ Compiler	H8S, H8/300 SERIES C/C++ Compiler Ver. 6.01.03 manufactured by Renesas Technology	
Compile Option	-cpu = H8SXA:24MD, -optimize = 1	
Linker Option	-start = P/0400	

Table 4 SDRAM Specifications

Item	Detail
Product Name	K4S641632K-UC75 (Samsung Electronics Corp.)
Configuration	1 Mword × 16 bits × 4 banks
Capacity	64 Mbits
CAS Latency	2/3 (programmable)
Refresh Interval	4096 refresh cycles per 64 ms
Row Address	A11 - A0
Column Address	A7 - A0
Number of Banks	Four banks for operation controlled by BA0 and BA1.

Table 5 SRAM Specifications

Item	Detail
Product Name	R1LV1616RSD-7SR (Renesas Technology Corp.)
Configuration	1 Mword × 16 bits
Capacity	16 Mbits

Note: The upper 1 Mbyte of SRAM is used for this application note.
(Because the maximum area of area 4 is 1 Mbyte)

Table 6 SDRAM Mode Settings

Item	Setting
Operation Code (OPCODE)	Burst read/single write
CAS Latency (LMODE)	2
Burst Type (BT)	Sequential
Burst Length (BL)	1
SDRAM Access Address	H'400440

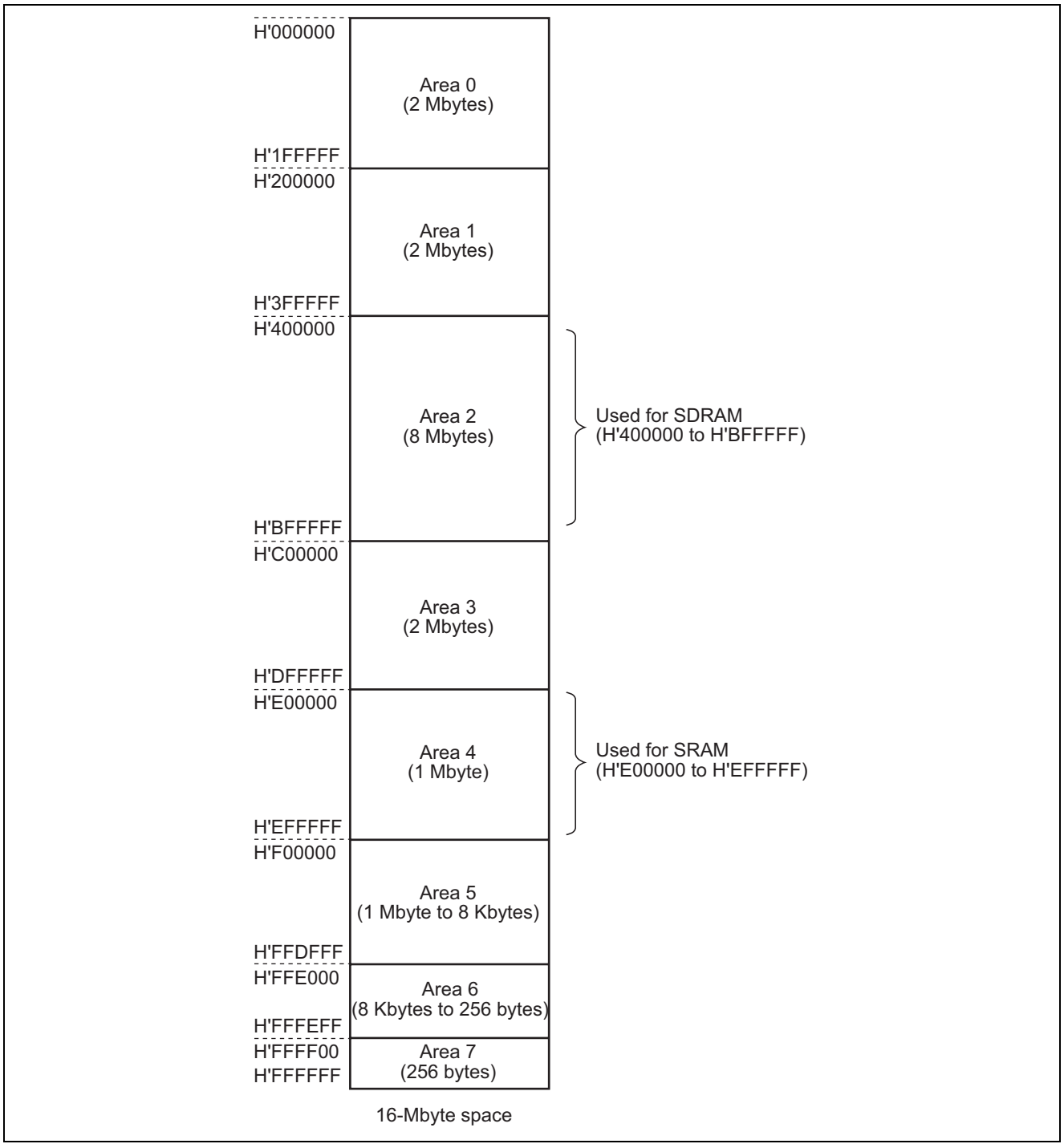

Figure 3 Address Space Area Division

3. Description of Modules Used

3.1 Normal Transfer Mode

In normal transfer mode, data is transferred in one-data access size units in response to each transfer request.

Total transfer size can be set up to 4 Gbytes in the EXDMA transfer count register (EDTCR).

Examples of timing and operation in this mode are shown in figure 4 and figure 5, respectively.

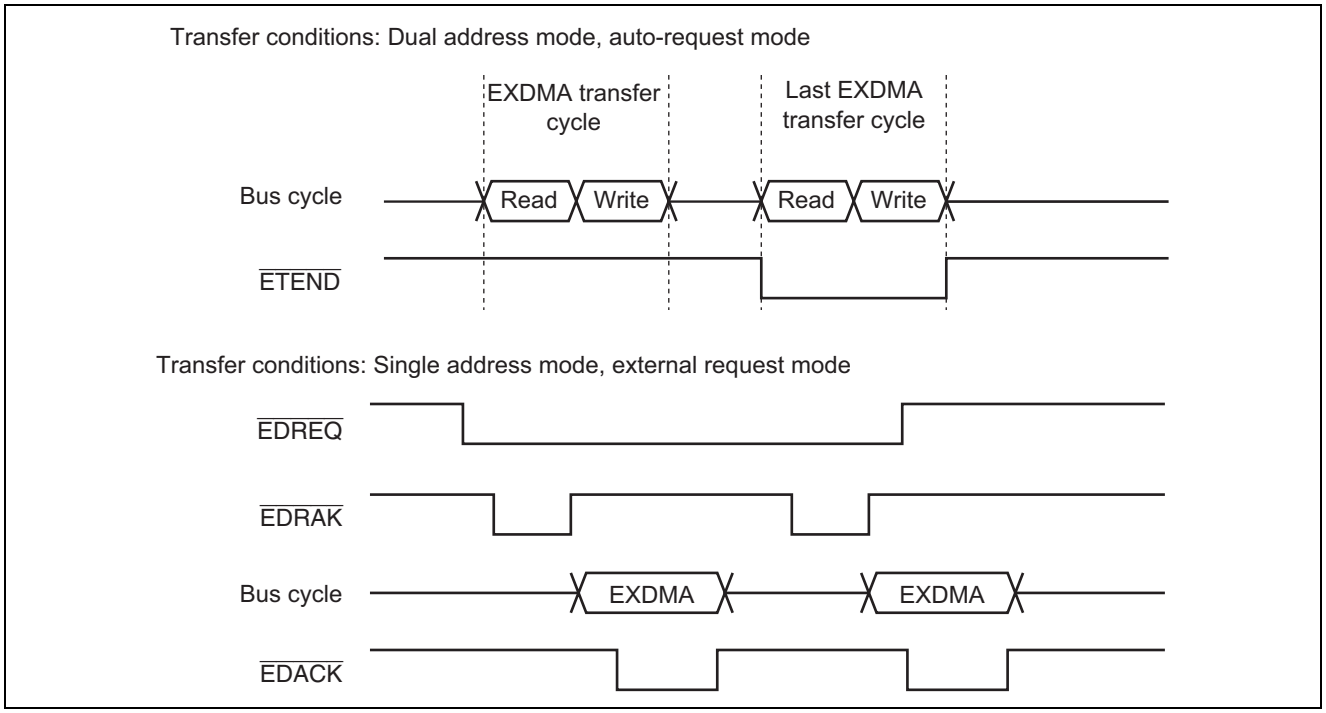

Figure 4 Example of Timing in Normal Transfer Mode

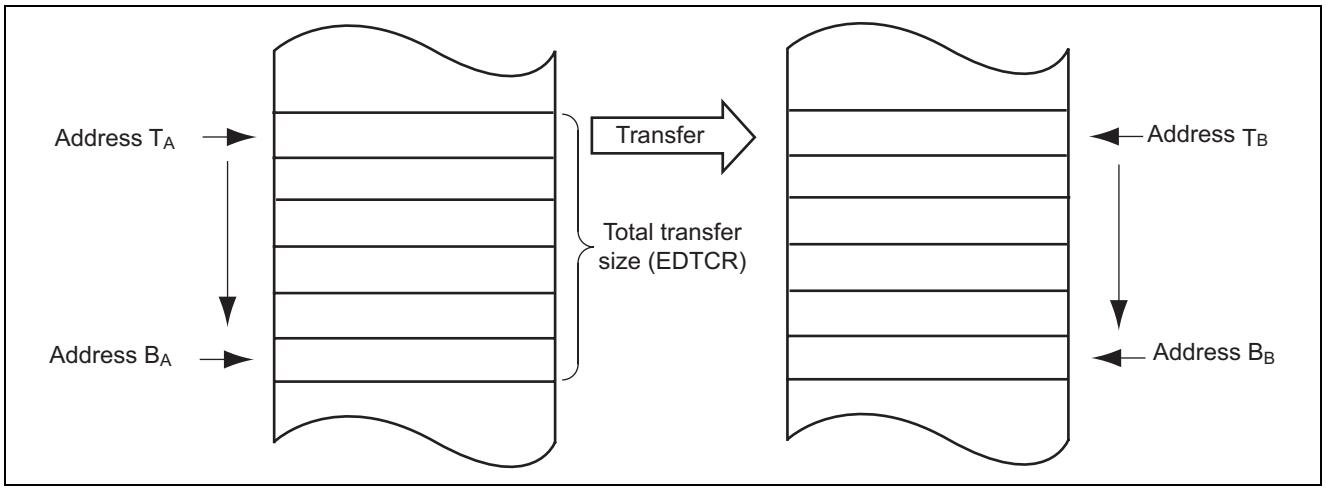

Figure 5 Example of Operation in Normal Transfer Mode

3.2 Address Update Function Using Offset Addition

When the offset addition is selected, the offset specified by the EXDMA offset register (EDOFR) is added to the address every time the EXDMAC transfers data of an access size. Also, the offset addition can be selected for both the source and destination addresses. This function enables the mid-addresses being skipped during data transfer.

In this application note, the offset addition is selected for both the source and destination addresses.

Figure 6 shows how to update an address.

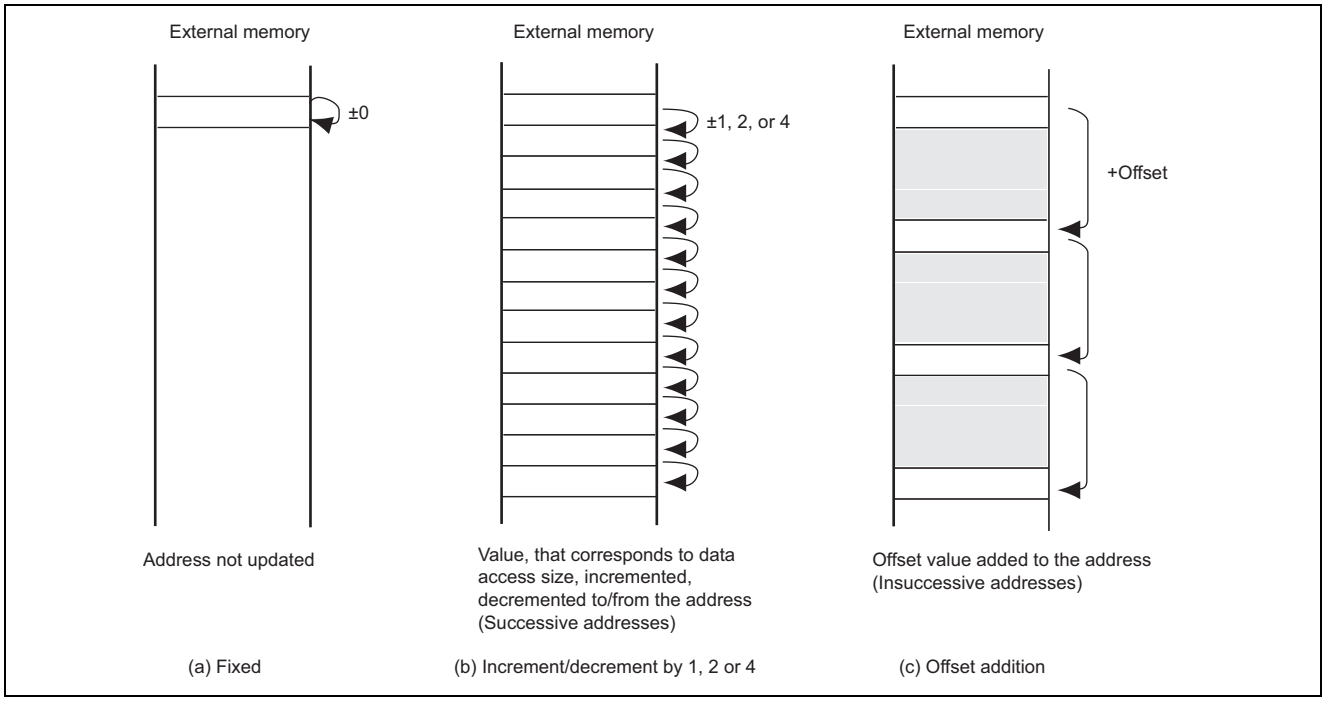

Figure 6 Address Update Methods

4. Principle of Operation

Operation in this application note is shown in figure 6.

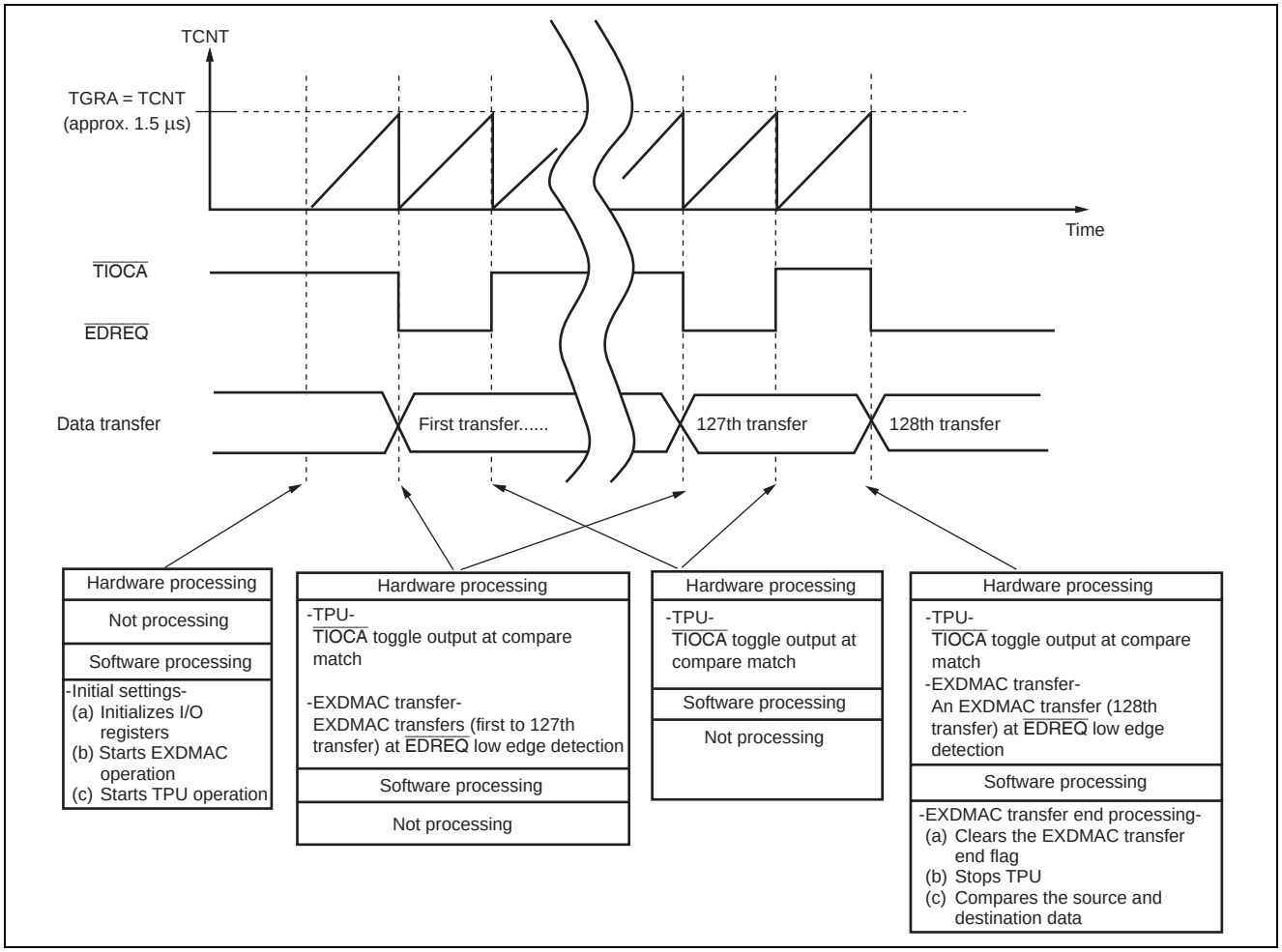

Figure 7 Operation

5. Description of Software

5.1 List of Functions

Table 7 List of Functions

Function Name	Description
main	• Main routine Calls functions of init and cmp_data, sets operations of EXDMAC and TPU, and judges whether an EXDMAC transfer is ended.
init	• Initialization routine Initializes registers and memory areas to be used, and sets data in the EXDMAC transfer source area.
cmp_data	• Transfer data compare routine Compares the source and destination data

5.2 Description of Functions

5.2.1 main Function

(1) Functional overview

Initialization of registers and RAM by calling init function.

Enables operations of EXDMAC and TPU. After end of EXDMAC transfer and by calling cmp_data function, compares data transferred.

(2) Arguments

None

(3) Return values

None

(4) Description of internal registers used

The internal registers used in this sample task are described below. The settings shown in these tables are the values used in this sample task and differ from the initial values.

- EXDMA Mode Control Register (EDMDR) Number of bits: 32 Address: H'FFFC94

Bit	Bit Name	Setting Value	R/W	Description
31	DTE	1	R/W	Data Transfer Enable Enables or disables data transfer on the corresponding channel. When this bit is set to 1, this indicates that an EXDMA operation is in operation. With external requests, transfer processing begins when a transfer request is issued after this bit has been set to 1. 1: Data transfer enabled (during an EXDMA operation)
16	DTIF	0	R/W	Data Transfer Interrupt Flag Flag indicating that a transfer end interrupt request has occurred by the transfer counter. 0: Transfer end interrupt request is not generated by the transfer counter

- Timer Start Register (TSTR) Number of bits: 8 Address: H'FFFFBC

Bit	Bit Name	Setting Value	R/W	Description
0	CST0	1	R/W	Counter Start 0 This bit selects operation or stoppage for TCNT. 1: TCNT_0 performs count operation

(5) Flowchart

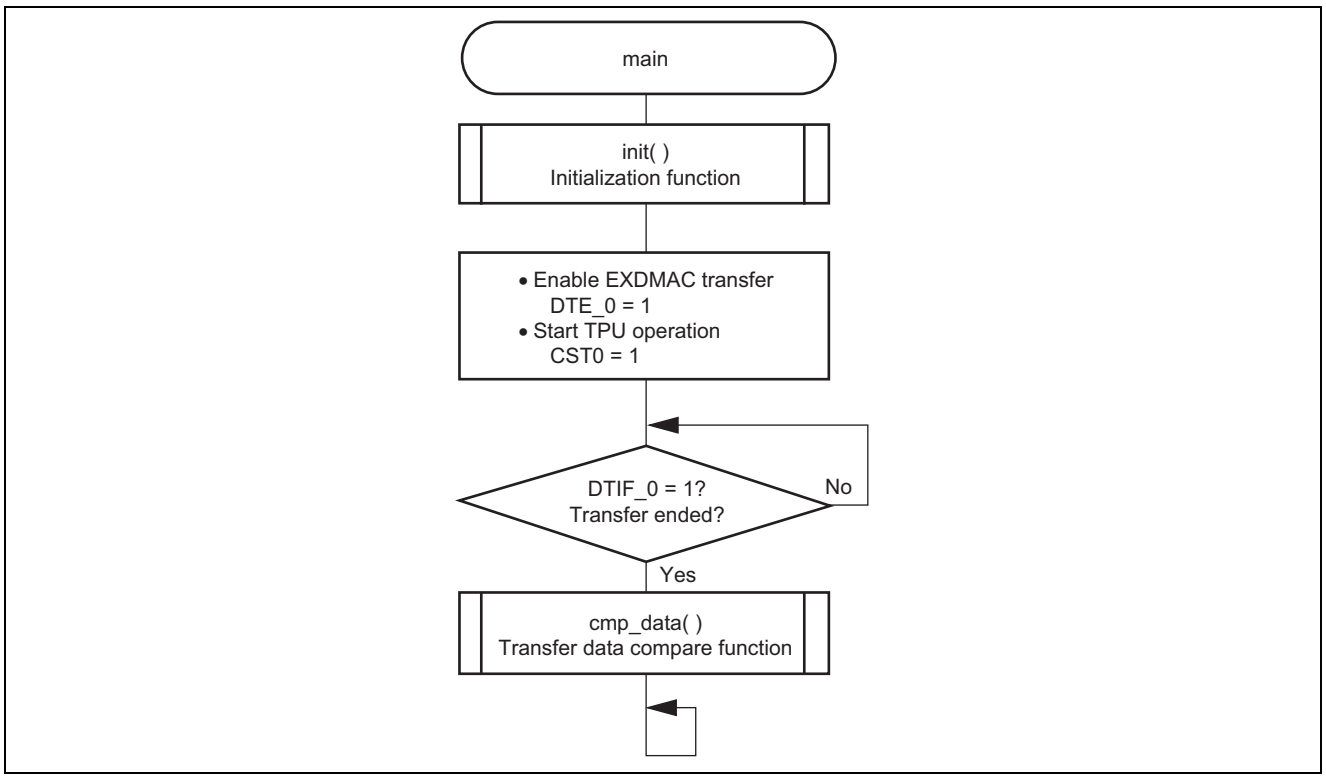

Figure 8 Flowchart (main)

5.2.2 init Function

(1) Functional overview

Initialization of I/O registers and memory by calling init function. Sets transfer source data.

(2) Arguments

None

(3) Return values

None

(4) Description of internal registers used

The internal registers used in this sample task are described below. The settings shown in these tables are the values used in this sample task and differ from the initial values.

- System Clock Control Register (SCKCR) Number of bits: 16 Address: H'FFFDC4

Bit	Bit Name	Setting Value	R/W	Description
10	ICK2	0	R/W	System Clock (Iϕ) Select
9	ICK1	0		These bits select the frequency of the system clock and the clock provided to the CPU, EXDMAC, DMAC, and DTC.
8	ICK0	0		000: Input clock × 4
6	PCK2	0	R/W	Peripheral Module Clock (Pϕ) Select
5	PCK1	0		These bits select the frequency of the peripheral module clock.
4	PCK0	1		001: Input clock × 2
2	BCK2	0	R/W	External Bus Clock (Bϕ) Select
1	BCK1	0		These bits select the frequency of the external bus clock.
0	BCK0	0		000: Input clock × 4

- MSTPCRA controls module stop mode. Setting a bit to 1 makes the corresponding module enter the stop mode, while clearing the bit to 0 makes the module exit the stop mode.

- Module Stop Control Register A (MSTPCRA) Number of bits: 16 Address: H'FFFDC8

Bit	Bit Name	Setting Value	R/W	Description
15	ACSE	0	R/W	All-Module-Clock-Stop Mode Enable Enables/disables all-module-clock-stop mode for reducing current consumption after the bus controller and I/O ports operation stop when the CPU executes the SLEEP instruction after all the on-chip peripheral modules controlled by MSTPCR has entered module stop mode 0: All-module-clock-stop mode disabled
14	MSTPA14	0	R/W	EXDMA controller (EXDMAC)
0	MSTPA0	0	R/W	16-bit timer pulse unit (TPU channels 5 to 0)

- Bus Width Control Register (ABWCR) Number of bits: 16 Address: H'FFFD84

Bit	Bit Name	Setting Value	R/W	Description
12	ABWH4	0	R/W	Area 7 to 0 Bus Width Control
10	ABWH2	0		These bits select whether the corresponding area is to be designated as 8-bit access space or 16-bit access space.
4	ABWL4	1		
2	ABWL2	1		ABWHn ABWLn (n = 7 to 0) 0 1: Area n is designated as 16-bit access space

- Access State Control Register (ASTCR) Number of bits: 16 Address: H'FFFD86

Bit	Bit Name	Setting Value	R/W	Description
12	AST4	1	R/W	These bits select whether the corresponding area is to be designated as 2- or 3-state access space. 1: Area n is designated as 3-state access space
10	AST2	1		

- Wait Control Register A (WTCRA) Number of bits: 16 Address: H'FFFD88

Bit	Bit Name	Setting Value	R/W	Description
2	W42	1	R/W	Area 4 Wait Control 2 to 0
1	W41	1		These bits select the number of program wait cycles when accessing area 4. 111: 7 program wait cycles inserted
0	W40	1		

- Wait Control Register B (WTCRB) Number of bits: 16 Address: H'FFFD8A

Bit	Bit Name	Setting Value	R/W	Description
10	W22	0	R/W	Area 2 Wait Control 2 to 0
9	W21	0		These bits select the number of program wait cycles when accessing area 2. When SDRAM is connected, the CAS latency is specified. At this time, W22 is ignored. 01: SDRAM with a CAS latency of 2 is connected.
8	W20	1		

- Idle Control Register (IDLCR) Number of bits: 16 Address: H'FFFD90

Bit	Bit Name	Setting Value	R/W	Description
15 to 12	IDLS2 to 0	0	R/W	Idle Cycle Insertion 3 to 0 Inserts an idle cycle between bus cycles 0: No idle cycle is inserted

- Endian Control Register (ENDIANCR) Number of bits: 8 Address: H'FFFD95

Bit	Bit Name	Setting Value	R/W	Description
4	LE4	0	R/W	Little Endian Select
2	LE2	0		Select the endian for the corresponding area. 0: Big endian

- SRAM Mode Control Register (SRAMCR) Number of bits: 16 Address: H'FFFD98

Bit	Bit Name	Setting Value	R/W	Description
12	BCSEL4	1	R/W	Byte Control SRAM Interface Select
10	BCSEL2	0		Select the bus interface for the corresponding area. 0: Basic bus interface 1: Byte control SRAM interface

- DRAM Control Register (DRAMCR) Number of bits: 16 Address: H'FFFDA0

Bit	Bit Name	Setting Value	R/W	Description
15	DRAME	1	R/W	Area 2 DRAM Interface Select Selects whether or not area 2 is specified as the DRAM/SDRAM interface. When this bit is set to 1, select the type of DRAM to be used in area 2 with the DTYPE bit. When this bit is set to 1, the BCSEL2 bit in SRAMCR should be set to 0. 1: DRAM/SDRAM interface
14	DTYPE	1	R/W	DRAM select Selects the type of DRAM to be connected to area 2. 1: SDRAM is connected to area 2
11	OEE	1	R/W	$\overline{OE}$ output enable The $\overline{OE}$ signal is output when DRAM with the EDO page mode is connected, whereas the CKE signal is output when SDRAM is connected. 1: $\overline{OE}$/CKE signal enabled
7	BE	1	R/W	Burst Access Enable Enables or disables a burst access to the DRAM/SDRAM. The DRAM/SDRAM is accessed in high-speed page mode. 1: DRAM/SDRAM is accessed in high-speed page mode

- DRAM Access Control Register (DRACCR) Number of bits: 16 Address: H'FFFDA2

Bit	Bit Name	Setting Value	R/W	Description
13	TPC1	0	R/W	Precharge Cycle Control
12	TPC0	0		Select the number of RAS precharge cycles on a normal access and a refresh. 00: One cycle
9	RCD1	0	R/W	$\overline{RAS}$-$\overline{CAS}$ Wait Control
8	RCD0	0		Determine whether to insert wait cycles between $\overline{RAS}$ and $\overline{CAS}$ assert cycles. 00: No wait cycle inserted

- Synchronous DRAM Control Register (SDCR) Number of bits: 16 Address: H'FFFDA4

Bit	Bit Name	Setting Value	R/W	Description
15	MRSE	0/1	R/W	Mode Register Set Enable Enables the setting in the SDRAM mode register. 0: Disables to set the SDRAM mode register 1: Enables to set the SDRAM mode register

Note: Setting the MRSE bit in SDCR to 1 enables the SDRAM mode register setting to set the SDRAM mode. After this, write to the SDRAM space in bytes.
After write access, clear the MRSE bit to 0 to disable the SDRAM mode setting.

- Refresh Control Register (REFCR) Number of bits: 16 Address: H'FFFDA6

Bit	Bit Name	Setting Value	R/W	Description
10	RTCK2	0	R/W	Refresh Counter Clock Select
9	RTCK1	1		Select a clock used to count up the refresh counter from the seven internal clocks generated by dividing the on-chip peripheral module clock (Pϕ). When the clock is selected, the refresh counter starts to count up.
8	RTCK0	0		010: Counts on Pϕ/8
7	RFSHE	1	R/W	Refresh Control Enables or disables refresh control. 1: Refresh control enabled

- Refresh Timer Counter (RTCNT) Number of bits: 8 Address: H'FFFDA8

  Description: RTCNT counts up on the internal clock selected by bits RTCS2 to RTCK0 in REFCR. When the RTCNT value matches the RTCOR value (compare match), the CMF flag in REFCR is set to 1 and RTCNT is cleared to H'00. At this time, when the RFSHE bit in REFCR is 1, a refresh cycle is generated.

  Setting Value: H'00

- Refresh Time Constant Register (RTCOR) Number of bits: 8 Address: H'FFFDA9

  Description: RTCOR specifies intervals at which a compare match for RTCOR and RTCNT is generated. The RTCOR value is always compared with the RTCNT value. When they match, the CMF flag in REFCR is set to 1 and RTCNT is cleared to H'00.

  Setting Value: H'30 (Refresh intervals: approx. 15.36 µs)

- Port Function Control Register 0 (PFCR0) Number of bits: 8 Address: H'FFFBC0

Bit	Bit Name	Setting Value	R/W	Description
4	CS4E	1	R/W	$\overline{CS7}$ to $\overline{CS0}$ Enable
2	CS2E	1		These bits enable/disable the corresponding $\overline{CS}$ output. 1: Pin functions as $\overline{CS}$ output pin

- Port Function Control Register 1 (PFCR1) Number of bits: 8 Address: H'FFFBC1

Bit	Bit Name	Setting Value	R/W	Description
1	CS4SA	0	R/W	$\overline{CS4}$ Output Pin Select
0	CS4SB	0		Selects the output pin for $\overline{CS4}$ when $\overline{CS4}$ output is enabled (CS4E = 1) 00: Specifies pin PB0 as $\overline{CS4}$-A output

- Port Function Control Register 2 (PFCR2) Number of bits: 8 Address: H'FFFBC2

Bit	Bit Name	Setting Value	R/W	Description
6	CS2S	1	R/W	$\overline{CS2}$ Output Pin Select Selects the output pin for $\overline{CS2}$ when $\overline{CS2}$ output is enabled (CS2E = 1). 1: Specifies pin PB1 as $\overline{CS2}$-B output

- Port Function Control Register 4 (PFCR4) Number of bits: 8 Address: H'FFFBC4

Bit	Bit Name	Setting Value	R/W	Description
7 to 0	A23E to A16E	1	R/W	Address A23 to A16 Enable Enable/disable the address output (A23 to A16). 1: Enables the A23 to A16 output

- Port Function Control Register 8 (PFCR8) Number of bits: 8 Address: H'FFFBC8

Bit	Bit Name	Setting Value	R/W	Description
1	EDMAS0A	0	R/W	EXDMAC Control Pin Select
0	EDMAS0B	0		Selects the I/O port to control EXDMAC_0. 00: Specify pins P10 to P13 as EXDMAC control pin

- Data Direction Register (P2DDR) Number of bits: 8 Address: H'FFFB81S
- Data Direction Register (P3DDR) Number of bits: 8 Address: H'FFFB82
- Data Direction Register (PDDDR) Number of bits: 8 Address: H'FFFB8A
- Data Direction Register (PEDDR) Number of bits: 8 Address: H'FFFB8D
- Data Direction Register (PFDDR) Number of bits: 8 Address: H'FFFB8E

  Description: DDR is an 8-bit write-only register that specifies a port I/O for each bit.
  Setting Value: H'FF

- Data Register (P3DR) Number of bits: 8 Address: H'FFFF52

  Description: DR is an 8-bit readable/writable register that stores output data of the pins to be used as the general output port.
  Setting Value: H'FF

- Input Buffer Control Register (P1ICR) Number of bits: 8 Address: H'FFFB90

  Description: ICR is an 8-bit readable/writable register that controls the port input buffers.
  Setting Value: H'01
  Note: This value is set to H'01 to use the EDREQ pin as the input pin.

- EXDMA Source Address Register (EDSAR) Number of bits: 32 Address: H'FFFC80

  Description: EDSAR is a 32-bit readable/writable register that specifies the transfer source address. An address update function is provided that updates the register contents to the next transfer source address each time transfer processing is performed.
  Setting Value: the start address of area 2.

- EXDMA Destination Address Register (EDDAR) Number of bits: 32 Address: H'FFFC84

  Description: EDDAR is a 32-bit readable/writable register that specifies the transfer destination address. An address update function is provided that updates the register contents to the next transfer destination address each time transfer processing is performed.
  Setting Value: the start address of area 4

- EXDMA Transfer Count Register (EDTCR) Number of bits: 32 Address: H'FFFC8C

  Description: EDTCR is a 32-bit readable/writable register that specifies the size of data to be transferred (total transfer size). The value according to the data access size is decremented every data transfer.
  Setting Value: H'80

- EXDMA Mode Control Register (EDMDR) Number of bits: 32 Address: H'FFFC94

Bit	Bit Name	Setting Value	R/W	Description
31	DTE	0	R/W	Data Transfer Enable Enables or disables data transfer on the corresponding channel. 0: Data transfer disabled
27	EDREQS	1	R/W	$\overline{\text{EDREQ}}$ select Selects whether low level or falling edge detection of the $\overline{\text{EDREQ}}$ signal is used in external request mode. 1: Falling edge detection (the first transfer is detected on a low level after a transfer is enabled.)
15 14	DTSZ1 DTSZ0	0 0	R/W	Data Access Size 1 and 0 Select the data access size for a transfer. 00: Byte-size (8 bits)
13 12	MDS1 MDS0	0 0	R/W	Transfer Mode Select 1 and 0 Select the transfer mode. 00: Normal transfer mode
8	DTIE	0	R/W	Data Transfer Interrupt Enable Enables or disables a transfer end interrupt request by the transfer counter. 0: Transfer end interrupt request disabled
7 6	DTF1 DTF0	1 1	R/W	Data Transfer Factor 1 and 0 Select a source to activate EXDMAC. 11: External request
2 1 0	EDMAP2 EDMAP1 EDMAP0	1 1 1	R/W	EXDMA Priority Levels 2 to 0 Select the EXDMAC priority level to determine the priority over CPU. 111: Priority level 7 (highest)

- EXDMA Address Control Register (EDACR) Number of bits: 32 Address: H'FFFC98

Bit	Bit Name	Setting Value	R/W	Description
31	AMS	0	R/W	Address Mode Select Selects single address mode or dual address mode. 0: Dual address mode
21 20	SAT1 SAT0	0 1	R/W	Source Address Update Mode 1 and 0 These bits specify incrementing/decrementing of the transfer source address (EDSAR). 01: Offset added
17 16	DAT1 DAT0	0 1	R/W	Destination Address Update Mode 1 and 0 These bits specify incrementing/decrementing of the transfer destination address (EDDAR). 01: Offset added

- Timer Control Register (TCR) Number of bits: 8 Address: H'FFFFC0

Bit	Bit Name	Setting Value	R/W	Description
7	CCLR2	0	R/W	Counter Clear 2 to 0
6	CCLR1	0		These bits select the TCNT counter clearing source.
5	CCLR0	1		001: TCNT cleared by TGRA compare match/input capture
4	CKEG1	0	R/W	Clock Edge 1 and 0
3	CKEG0	0		These bits select the input clock edge.
				00: Counted at an internal clock falling edge
2	TPSC2	0	R/W	Timer Prescaler 2 to 0
1	TPSC1	0		These bits select the TCNT counter clock.
0	TPSC0	0		000: Counts on internal clock Pϕ/1

- Timer I/O Control Register _H (TIOR_H) Number of bits: 8 Address: H'FFFFC2

Bit	Bit Name	Setting Value	R/W	Description
3	IOA3	0	R/W	I/O Control A3 to A0
2	IOA2	1		Specify the function of TGRA.
1	IOA1	1		0111: TIOCA0 pin initial value is 1. Toggle output at compare
0	IOA0	1		match.

- Timer Interrupt Enable Register (TIER) Number of bits: 8 Address: H'FFFFC4

Bit	Bit Name	Setting Value	R/W	Description
0	TGIEA	0	R/W	TGR Interrupt Enable A
				Enables/disables interrupt requests (TGIA) by the TGFA bit when the TGFA bit in TSR is set to 1.
				0: Interrupt requests (TGIA) by TGFA bit disabled

- Timer Counter (TCNT) Number of bits: 16 Address: H'FFFFC6
  Description: TCNT is a 16-bit readable/writable counter.
  TCNT is initialized to H'0000 by a reset or in hardware standby mode.
  Setting Value: H'0000

- Timer General Register (TGR) Number of bits: 16 Address: H'FFFFC8
  Description: TGR is a 16-bit readable/writable register for use in output compare and input capture.
  Setting Value: H'0025 (TPU period: approx. 1.5 μs)

- Timer Start Register (TSTR) Number of bits: 8 Address: H'FFFFBC

Bit	Bit Name	Setting Value	R/W	Description
0	CST0	0	R/W	Counter Start 0
				This bit selects operation or stoppage for TCNT.
				0: TCNT_0 count operation is stopped

(5) Flowchart

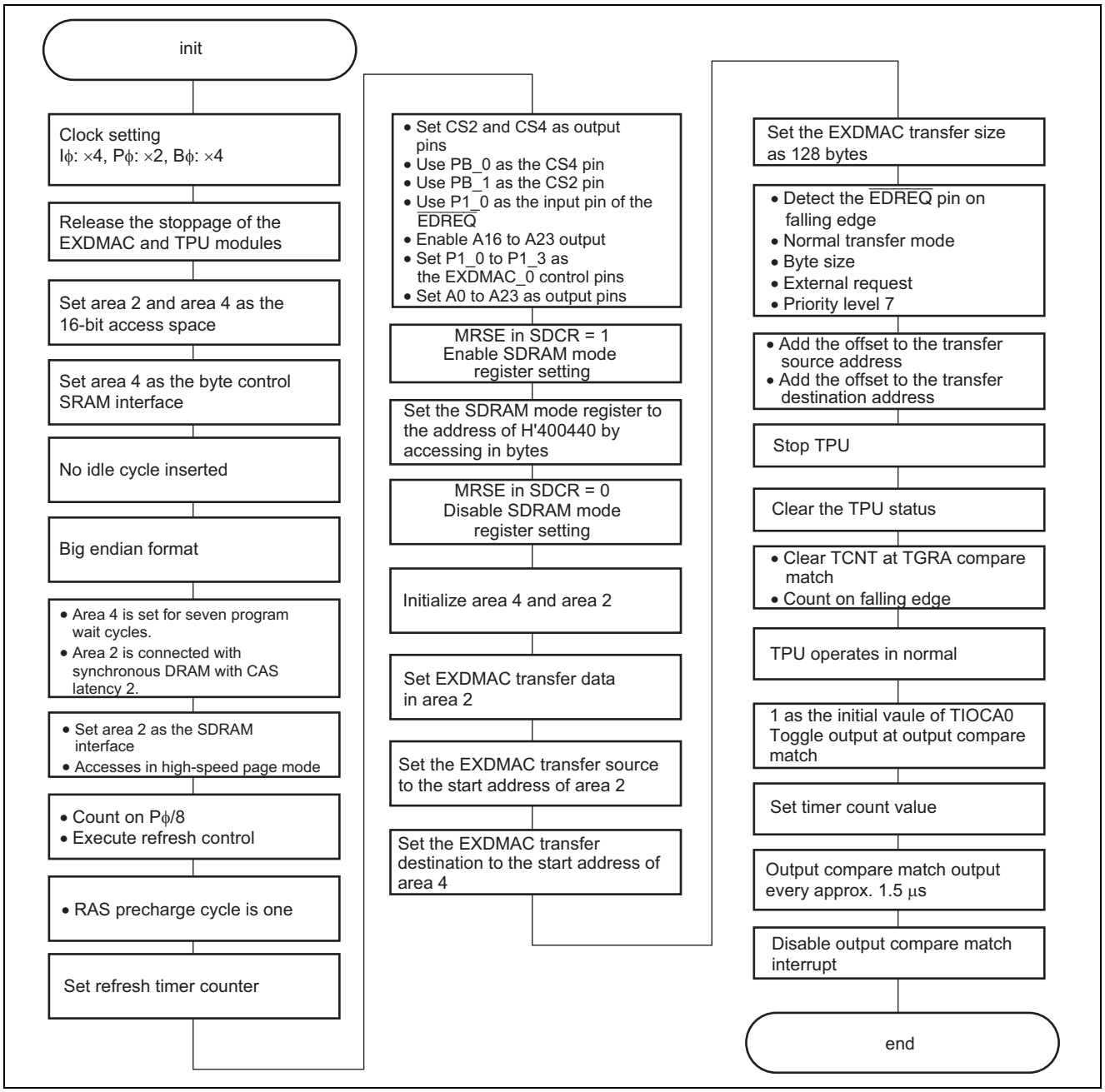

Figure 9 Flowchart

5.2.3 cmp_data Function

(1) Functional overview

The cmp_data function compares EXDMAC transfer data and outputs the result to a port.

(2) Arguments

None

(3) Return values

None

(4) Description of internal registers used

The internal registers used in this sample task are described below. The settings shown in these tables are the values used in this sample task and differ from the initial values.

- EXDMA Mode Control Register (EDMDR) Number of bits: 32 Address: H' 'FFFC94

Bit	Bit Name	Setting Value	R/W	Description
16	DTIF	0	R/W	Data Transfer Interrupt Flag Flag indicating that a transfer end interrupt request has occurred by the transfer counter. 0: Transfer end interrupt request is not generated by the transfer counter

- Timer Start Register (TSTR) Number of bits: 8 Address: H'FFFFBC

Bit	Bit Name	Setting Value	R/W	Description
0	CST0	0	R/W	Counter Start 0 This bit selects operation or stoppage for TCNT. 0: TCNT_0 count operation is stopped

- Data Register (P3DR) Number of bits: 8 Address: H'FFFF52

  Description: DR is an 8-bit readable/writable register that stores output data of the pins to be used as the general output port.

  Setting Value: H'55, H'FF

(5) Flowchart

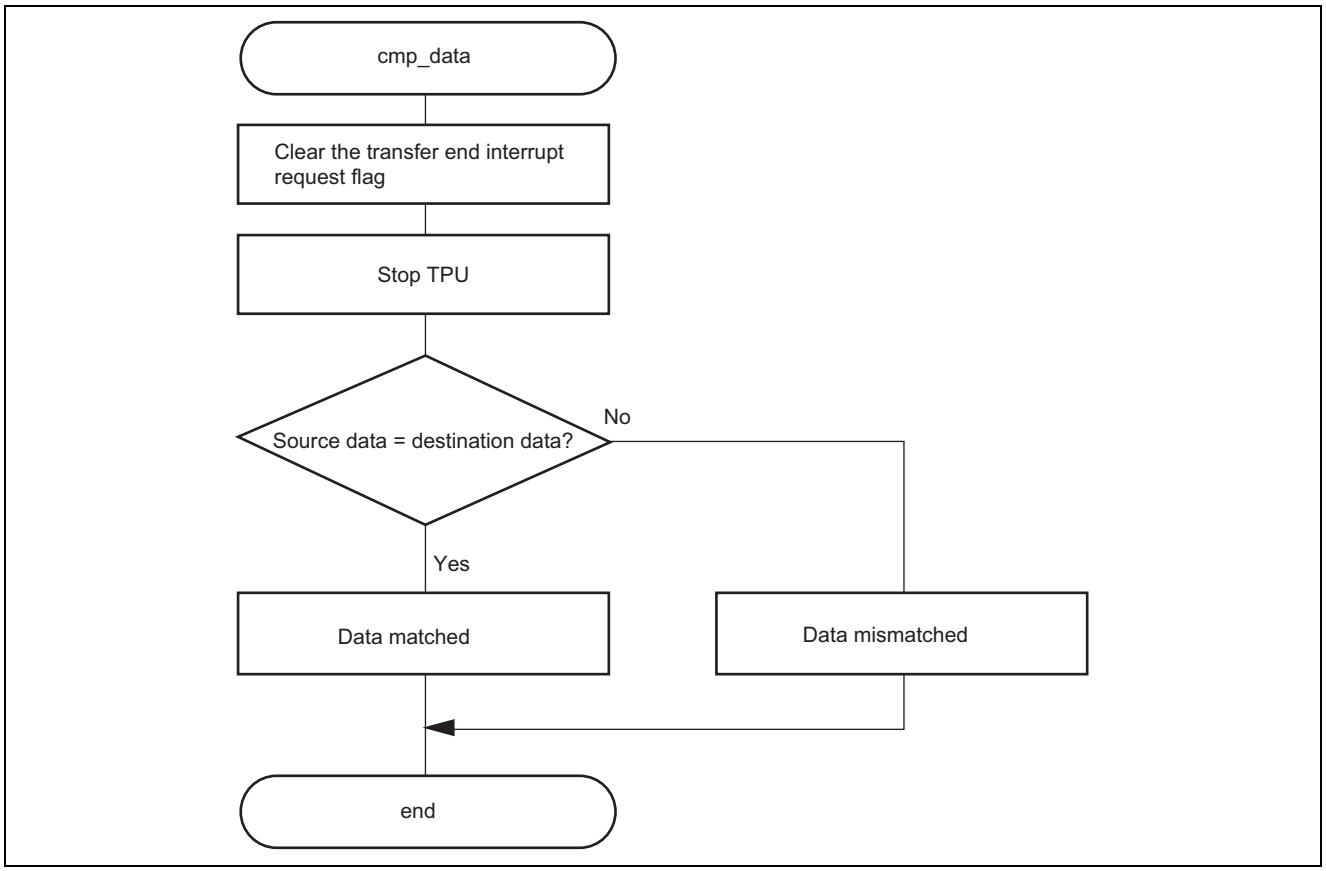

Figure 10 Flowchart

6. Precautions

(1) When pins of the device are used as the input pins of peripheral module, the corresponding bit in the input buffer control register (PnICR) is set as 1.
For details, refer to the appropriate hardware manual.

(2) Interrupt requests from the on-chip peripheral modules cannot be used as the sources of EXDMAC activation.
For details, refer to the following appropriate hardware manual.

7. Documents for Reference

- Hardware manual:
  H8SX/1668R Group Hardware Manual
  (Download the latest version from Renesas Technology's website.)
- Technical News, Technical Update
  (Obtain the latest information from Renesas Technology's website.)
- H8SX Family Application Note
  "Synchronous DRAM Interface" document No. REJ06B0659-0100
  (Download the latest information from Renesas Technology's website.)

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