To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

Send any inquiries to http://www.renesas.com/inquiry.

M16C/28,29 Group

Timer S Functions

1. Abstract

This application note shows the Timer S functions of M16C/28, 29 Group.

2. Introduction

This application note is applied to the following microcomputers:
MCU: M16C/28 Group
M16C/29 Group

3. Introduction of Applied Technology

3.1 Timer S

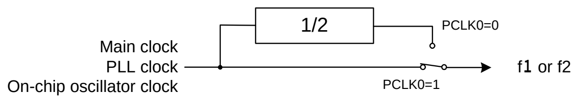
Timer S is a peripheral function of M16C/28, 29 Group, and composed of the time measurement and the waveform generation functions.
Table 1 shows Timer S functions.

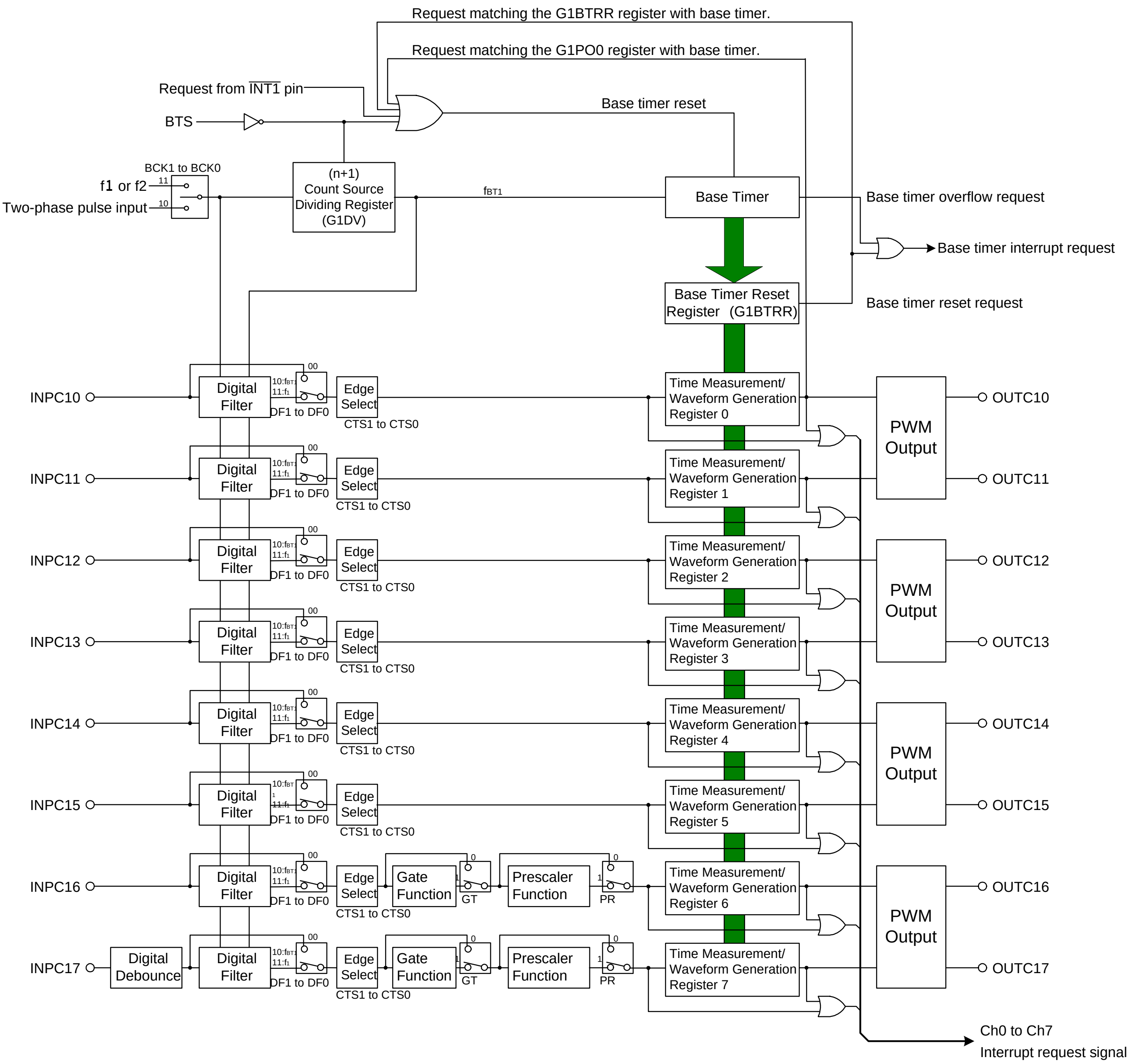
Table 1 Configuration of M16C/28, 29 Group Timer S Functions

Functions		Configuration
Base Timer		1 Channel
Time Measurement Function		8 Channel
	Digital Filter	8 Channel
	Trigger Input Prescaler	2 Channel
	Trigger Input Gate	2 Channel
Waveform Generation Function		8 Channel
	Single-phase Waveform Output	Valid
	Phase-delayed Waveform Output	Valid
	SR Waveform Output	Valid

3.2 Configuration of Timer S

Base timer operation is a basic element of the time measurement and the waveform generation functions. The base timer is a 16-bit free-running timer, and peripheral function clock is a count source of the base timer.





BCK1 to BCK0 : Bit in the G1BCR0 register
BTS : Bit in the G1BCR1 register
CTS1 **to** CTS0, DF1 to DF0, GT, PR : Bit in the G1TMCRj register(j=0 to 7)
PCLK0 : Bit in the PCLKR register

Figure 1 Timer S Block Diagram

3.3 Time Measurement Function (Input Capture)

When a trigger input signal is applied, the base timer value is stored in the time measurement register, and an interrupt request is generated.

At the timing when an external trigger signal is applied, the base timer value is stored in the time measurement register. A time measurement interrupt request is generated when a trigger input signal is applied.

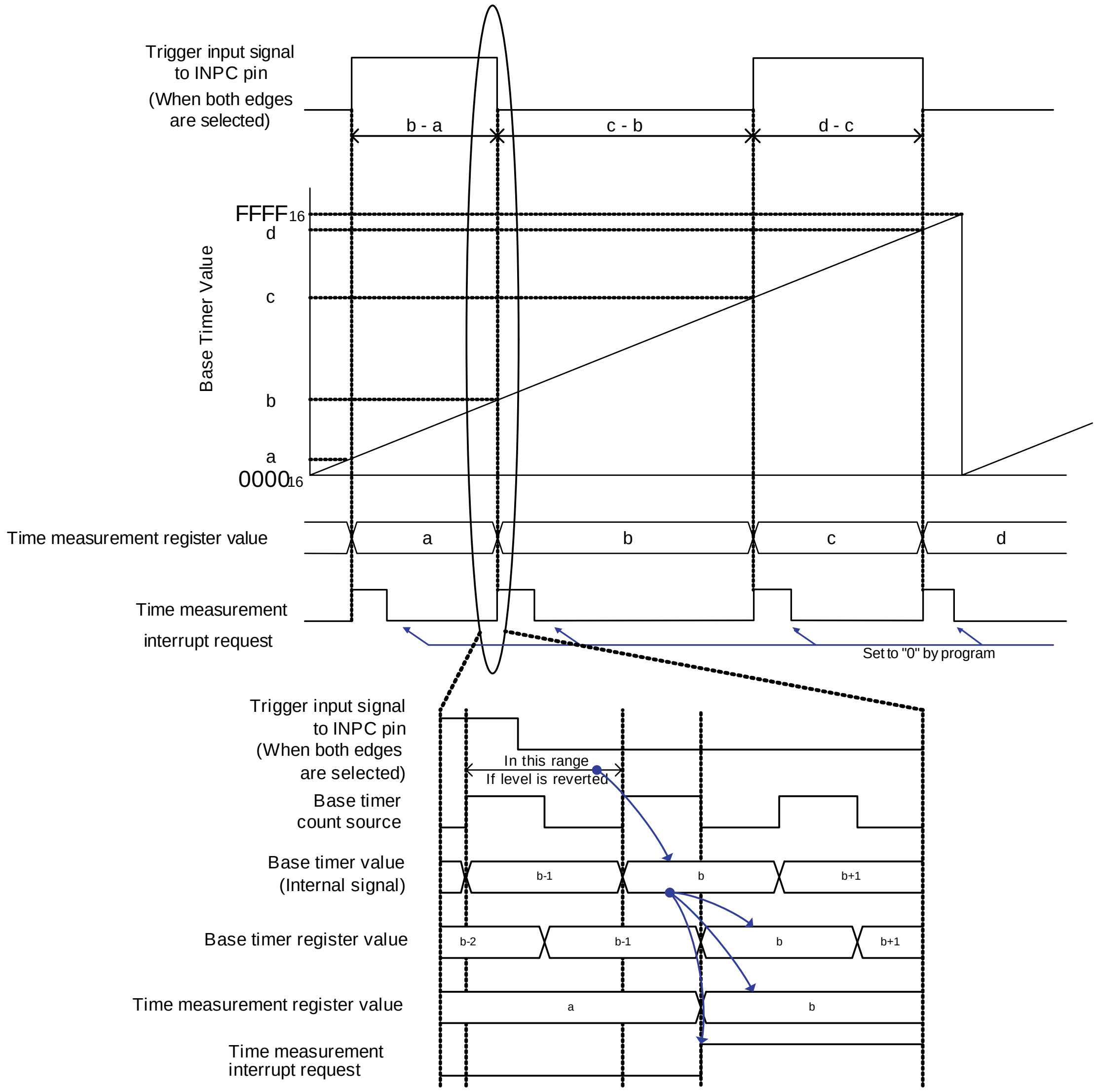


Figure 2 Operation Timing of Time Measurement Function

Time measurement function enables to measure signals for the following purposes.

Edge select function
Digital filter function
Gate function
Prescaler function
Digital debouce function

The following is the explanation for these functions.

3.3.1 Edge Select Function

Edge select function can select the trigger input polarity from rising edge, falling edge and both edges.

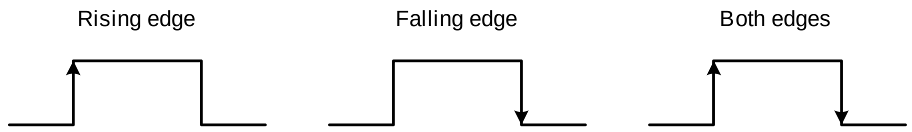


Figure 3 Edge Select

3.3.2 Digital Filter Function

In the digital filter function, the filter clock (f_1 or f_{BT1}) samples trigger input level and signals that matched three times are passed.

After the rising edge is applied to INPC pin, the level sampling is carried out every digital filter clock cycle.

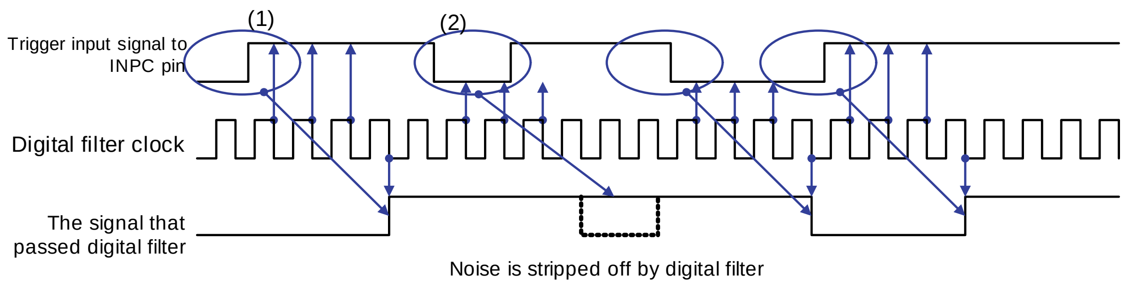


Figure 4 Digital Filter Operation Timing

(1) If the trigger input level matches three times continuously, the level which passed the digital filter changes.
(2) If the trigger input level does not match three times, the input signal is stripped off as noise and does not change after passing digital filter.

Time measurement can be carried out by the noise-free signal that passed digital filter.

When using the digital filter function, the trigger signal is delayed due to sampling of the trigger input level. However, time measurement can be carried out correctly since the delay happened in the over all process.

3.3.3 Gate Function

Gate function is a function that can disable the trigger input signal receiving at desired time after the initial trigger signal is applied. This disable state can be cleared by the program or by matching the waveform generation register with the base timer.
Gate function is mounted in the channel 6 and 7.

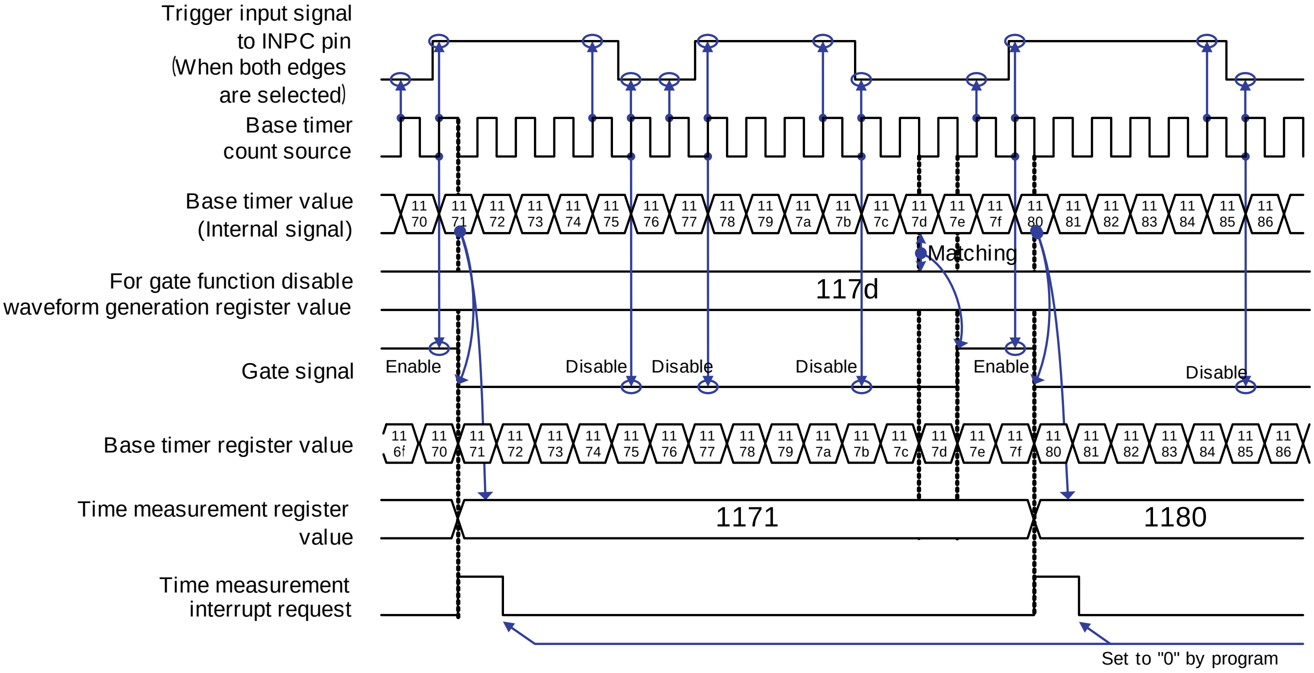


Figure 5 Gate Function Operation Timing Diagram

In Figure 5, when a trigger input signal is applied to the INPC pin, the base timer value is stored in the time measurement register, and the trigger input is disabled. However, the trigger input is enabled by matching the base timer value with the one written in the waveform generation register ($117d_{16}$). After trigger input inhibit is cleared, the base timer value is stored in the time measurement register at the timing when the trigger input is applied.

3.3.4 Prescaler Function

In the prescaler function, the trigger input is counted and received every designated number of times.
The base timer value is stored in the time measurement register when the trigger input signals are applied every designated number of times. The register that designates the prescaler value consists of 8 bits, and the prescaler value can be set up to 255 times. (The designated number of times stands for the prescaler setting value +1.)
Prescaler function is mounted in the channel 6 and 7.

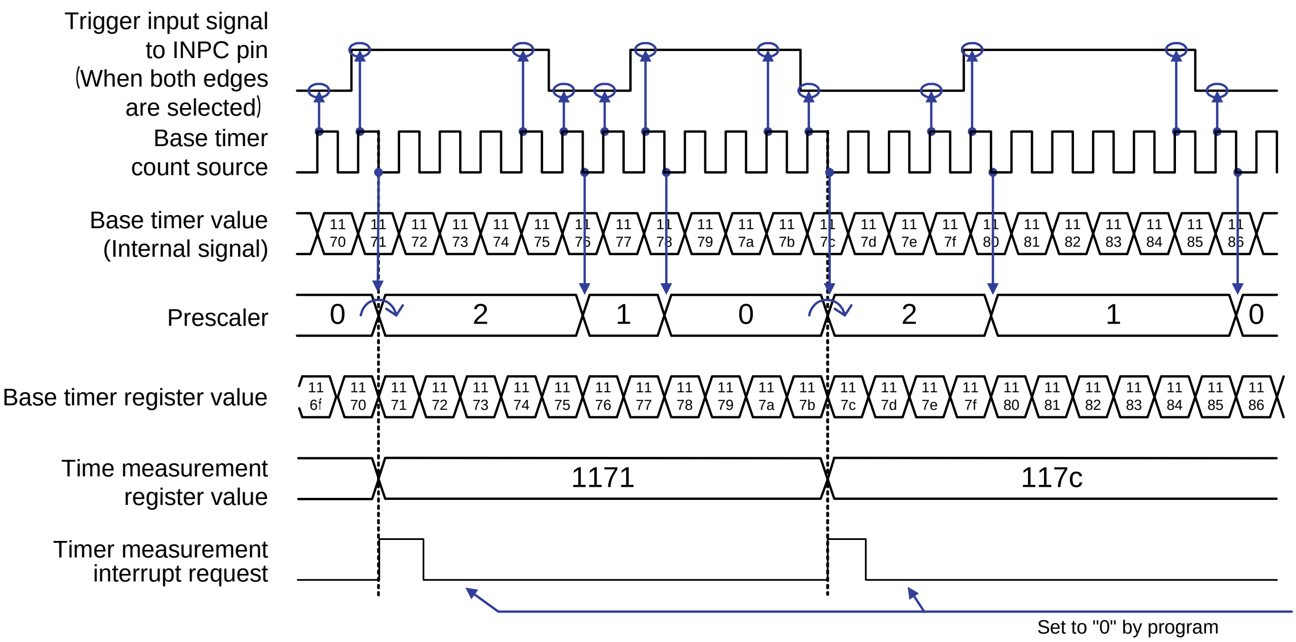


Figure 6 Prescaler Operation Timing Diagram

Figure 6 shows that the prescaler value is set to “2”. When the initial trigger input is applied, the base timer value is stored in the time measurement register. Then, the trigger input is counted and the base timer value is stored at the third trigger input.

3.3.5 Digital Debounce Function

In digital debounce function, the f_8 clock samples the trigger input level the designated number of times (=the setting value in the $P1_7$ digital debouce register +1), and then matched trigger input level is passed.

If the trigger input level matches the number of designated times continuously, the level passes the digital debounce filter.
If the trigger input level does not match the number of designated times, the input signal is stripped off as noise .

In this function, only the channel 7 is valid when the input select bit in the base timer control register 0 is “1”.

3.4 Waveform Generation Function (Output Compare)

The output compare function can generate a matching signal at the timing when the base timer value matches that of the waveform generation register. An interrupt request is generated by this matching signal, and the output signal changes.

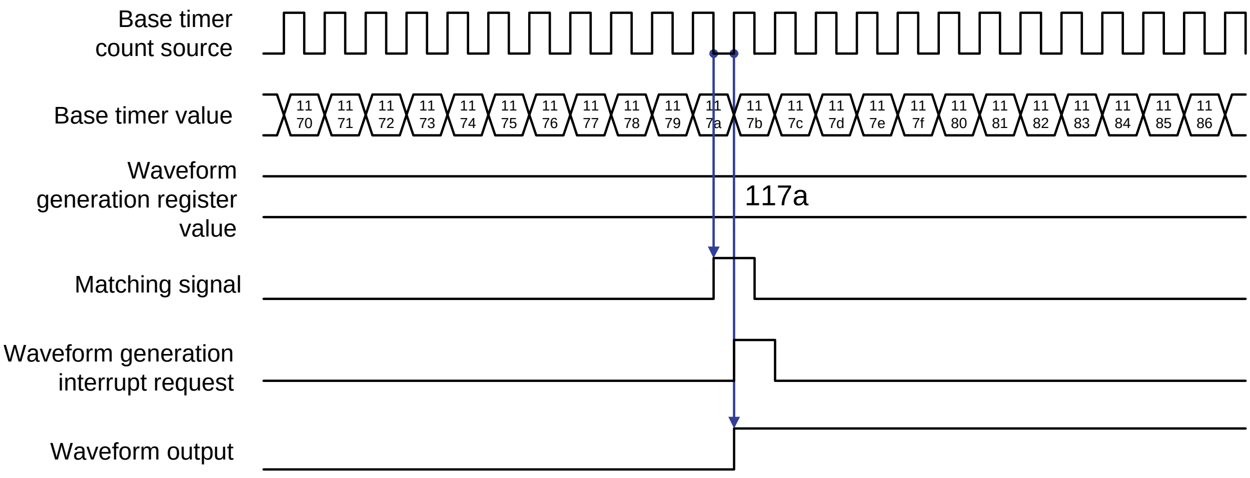


Figure 7 Waveform Generation Output Function (Output Compare) Operation Timing

3.4.1 Basic Waveform Output

(1) Single-phase Waveform Output

In the single-phase waveform output mode, the output level of the waveform output pin becomes "H" at the timing when the value of waveform generation register matches that of the base timer. The "H" signal switches to "L" when the base timer value reaches "0000_{16}".

(2) Phase-delayed Waveform Output

In the phase-delayed waveform output mode, the output level from the waveform output pin is inverted every time when the value of the waveform generation register matches that of the base timer.

(3) Set-reset (SR) Waveform Output

In the set-reset waveform output mode, the output level from the waveform output pin becomes "H" at the timing when the value of waveform generation register "n (n=0,2,4,6)" matches that of the base timer. The "H" signal switches to "L" at the timing when the value of the waveform generation register m (m=n+1) matches that of the base timer, or when the value of the base timer reaches "0000_{16}".

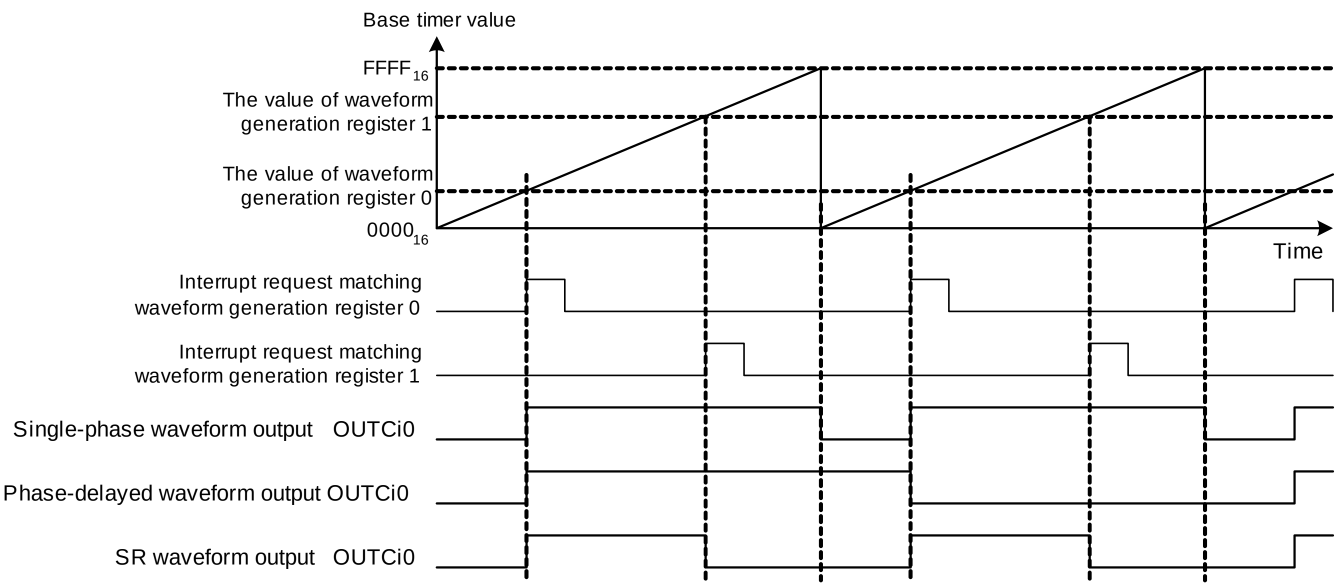


Figure 8 Waveform Generation Output Operation Timing

The following functions are selectable for each mode.
Initial value set function
Initial output level of the output compare pin can be set.

Output level inverse function
The output inverting circuit is the final step of the waveform generation circuit.
Output polarity can be inverted.

Base timer reset function by matching waveform generation register 0 with the base timer
The base timer reaches "0000_{16}" two clock cycles after the base timer value matches that of the waveform generation register 0.

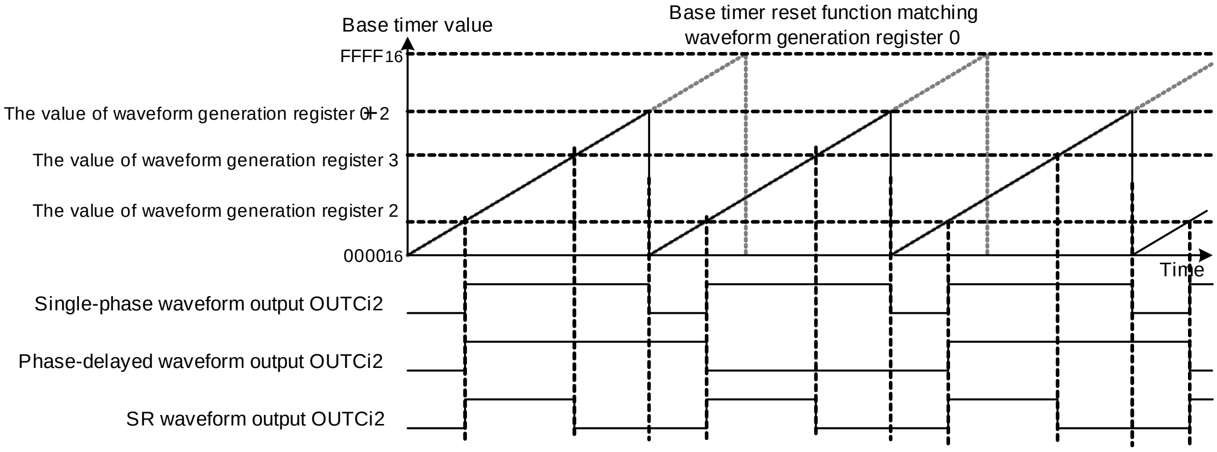


Figure 9 Base Timer Reset Operation Diagram

In figure 9, the base timer reaches "0000_{16}" two clock cycles after the base timer value matches that of the waveform generation register.

3.4.2 Application Example: 16-bit PWM Output

The following is an example of 16-bit PWM output by using the output compare function.

PWM frequency is set in the waveform generation register 0. Select “Reset the base timer by matching the base timer value with that of the waveform generation 0”.

“L” width of output compare is set in the waveform generation register 1 to 7.

In conventional M16C series, the frequency is fixed when 16-bit PWM output in timer A is achieved. When using Timer S, 16-bit PWM waveform output can be achieved with the variable frequency.

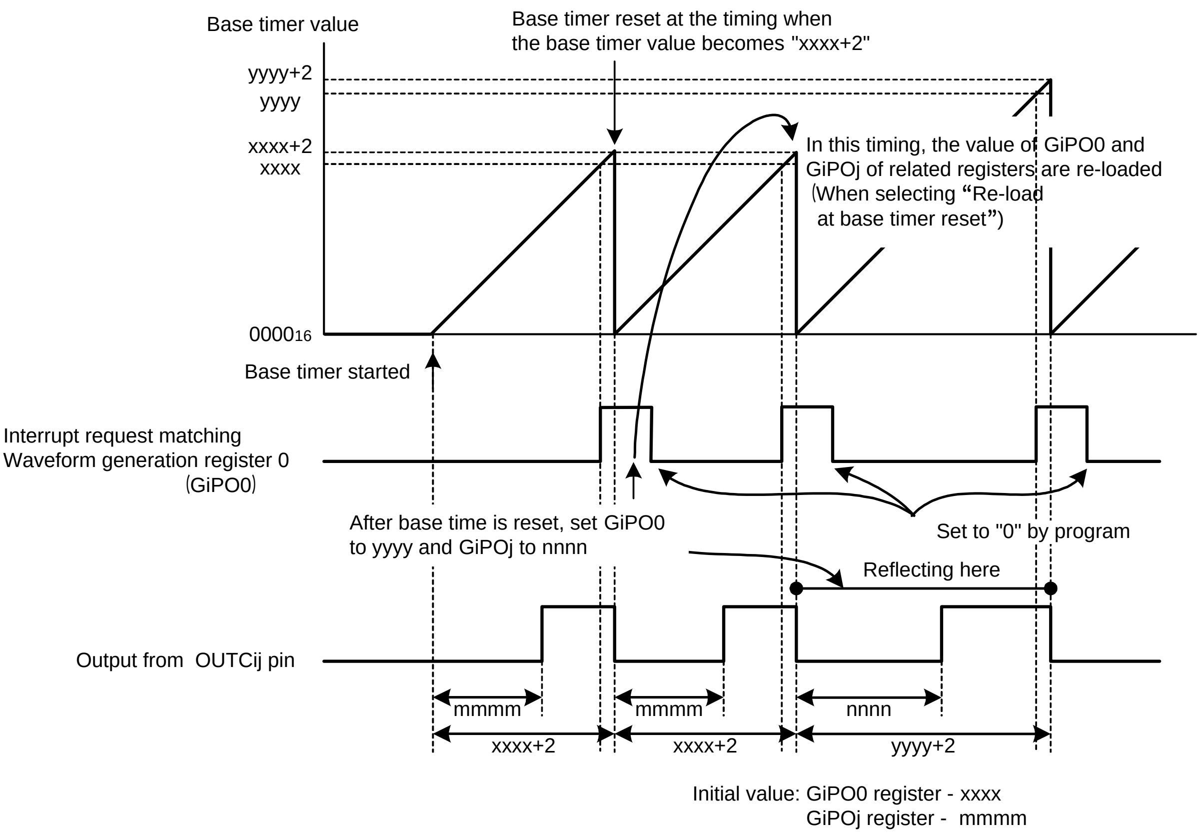


Figure 10 16-bit PWM Output Diagram

In figure 10, the GiPO0 register is set to ‘xxxx’ and the GiPOj register is set to ‘mmmm’ to start the base timer. An interrupt request is generated when the base timer value matches that of GiPO0 register, then the output of OUTij pin becomes “L” and the value of the base timer becomes “0000_{16}” 2 clock cycles later.

4. Reference

Hardware Manual

M16C/28 Group Hardware Manual

M16C/29 Group Hardware Manual

(The latest version is available on the website: http://www.renesas.com)

5. Website and Contact for Support

Renesas Website

http://www.renesas.com/

For technical information related to M16C family

E-mail: support_apl@renesas.com

REVISION HISTORY

Rev.	Date	Description	
		Page	Summary
1.00	2004.09.23	-	First edition issued