To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

Send any inquiries to http://www.renesas.com/inquiry.

Notice

1. All information included in this document is current as of the date this document is issued. Such information, however, is subject to change without any prior notice. Before purchasing or using any Renesas Electronics products listed herein, please confirm the latest product information with a Renesas Electronics sales office. Also, please pay regular and careful attention to additional and different information to be disclosed by Renesas Electronics such as that disclosed through our website.
2. Renesas Electronics does not assume any liability for infringement of patents, copyrights, or other intellectual property rights of third parties by or arising from the use of Renesas Electronics products or technical information described in this document. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
3. You should not alter, modify, copy, or otherwise misappropriate any Renesas Electronics product, whether in whole or in part.
4. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation of these circuits, software, and information in the design of your equipment. Renesas Electronics assumes no responsibility for any losses incurred by you or third parties arising from the use of these circuits, software, or information.
5. When exporting the products or technology described in this document, you should comply with the applicable export control laws and regulations and follow the procedures required by such laws and regulations. You should not use Renesas Electronics products or the technology described in this document for any purpose relating to military applications or use by the military, including but not limited to the development of weapons of mass destruction. Renesas Electronics products and technology may not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations.
6. Renesas Electronics has used reasonable care in preparing the information included in this document, but Renesas Electronics does not warrant that such information is error free. Renesas Electronics assumes no liability whatsoever for any damages incurred by you resulting from errors in or omissions from the information included herein.
7. Renesas Electronics products are classified according to the following three quality grades: "Standard", "High Quality", and "Specific". The recommended applications for each Renesas Electronics product depends on the product's quality grade, as indicated below. You must check the quality grade of each Renesas Electronics product before using it in a particular application. You may not use any Renesas Electronics product for any application categorized as "Specific" without the prior written consent of Renesas Electronics. Further, you may not use any Renesas Electronics product for any application for which it is not intended without the prior written consent of Renesas Electronics. Renesas Electronics shall not be in any way liable for any damages or losses incurred by you or third parties arising from the use of any Renesas Electronics product for an application categorized as "Specific" or for which the product is not intended where you have failed to obtain the prior written consent of Renesas Electronics. The quality grade of each Renesas Electronics product is "Standard" unless otherwise expressly specified in a Renesas Electronics data sheets or data books, etc.

   "Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; and industrial robots.

   "High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control systems; anti-disaster systems; anti-crime systems; safety equipment; and medical equipment not specifically designed for life support.

   "Specific": Aircraft; aerospace equipment; submersible repeaters; nuclear reactor control systems; medical equipment or systems for life support (e.g. artificial life support devices or systems), surgical implantations, or healthcare intervention (e.g. excision, etc.), and any other applications or purposes that pose a direct threat to human life.
8. You should use the Renesas Electronics products described in this document within the range specified by Renesas Electronics, especially with respect to the maximum rating, operating supply voltage range, movement power voltage range, heat radiation characteristics, installation and other product characteristics. Renesas Electronics shall have no liability for malfunctions or damages arising out of the use of Renesas Electronics products beyond such specified ranges.
9. Although Renesas Electronics endeavors to improve the quality and reliability of its products, semiconductor products have specific characteristics such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Further, Renesas Electronics products are not subject to radiation resistance design. Please be sure to implement safety measures to guard them against the possibility of physical injury, and injury or damage caused by fire in the event of the failure of a Renesas Electronics product, such as safety design for hardware and software including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult, please evaluate the safety of the final products or system manufactured by you.
10. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. Please use Renesas Electronics products in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. Renesas Electronics assumes no liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
11. This document may not be reproduced or duplicated, in any form, in whole or in part, without prior written consent of Renesas Electronics.
12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products, or if you have any other inquiries.

(Note 1) "Renesas Electronics" as used in this document means Renesas Electronics Corporation and also includes its majority-owned subsidiaries.

(Note 2) "Renesas Electronics product(s)" means any product developed or manufactured by or for Renesas Electronics.

R8C/25 Group

Timer RD in Input Caputure and Output Compare Functions

1. Abstract

This document describes a program for timer RD in the input capture and output compare functions.

2. Introduction

The application example described in this document applies to the following MCU and parameter(s):

- MCU : R8C/25 Group

This program can be used with other R8C/Tiny Series MCUs which have analogous special function registers (SFRs) as the R8C/25 Group. Check the manual for any additions and modifications to functions. Careful evaluation is recommended before using this application note.

3. Application Example Description

Timer RD has two 16-bit timers (channels 0 and 1). Each channel has four I/O pins.

Timer mode consists of two functions: Input capture and output compare. In the input capture and output compare functions, channels 0 and 1 have the equivalent functions, and functions can be selected individually for each pin. Also, a combination of these functions can be used in one channel.

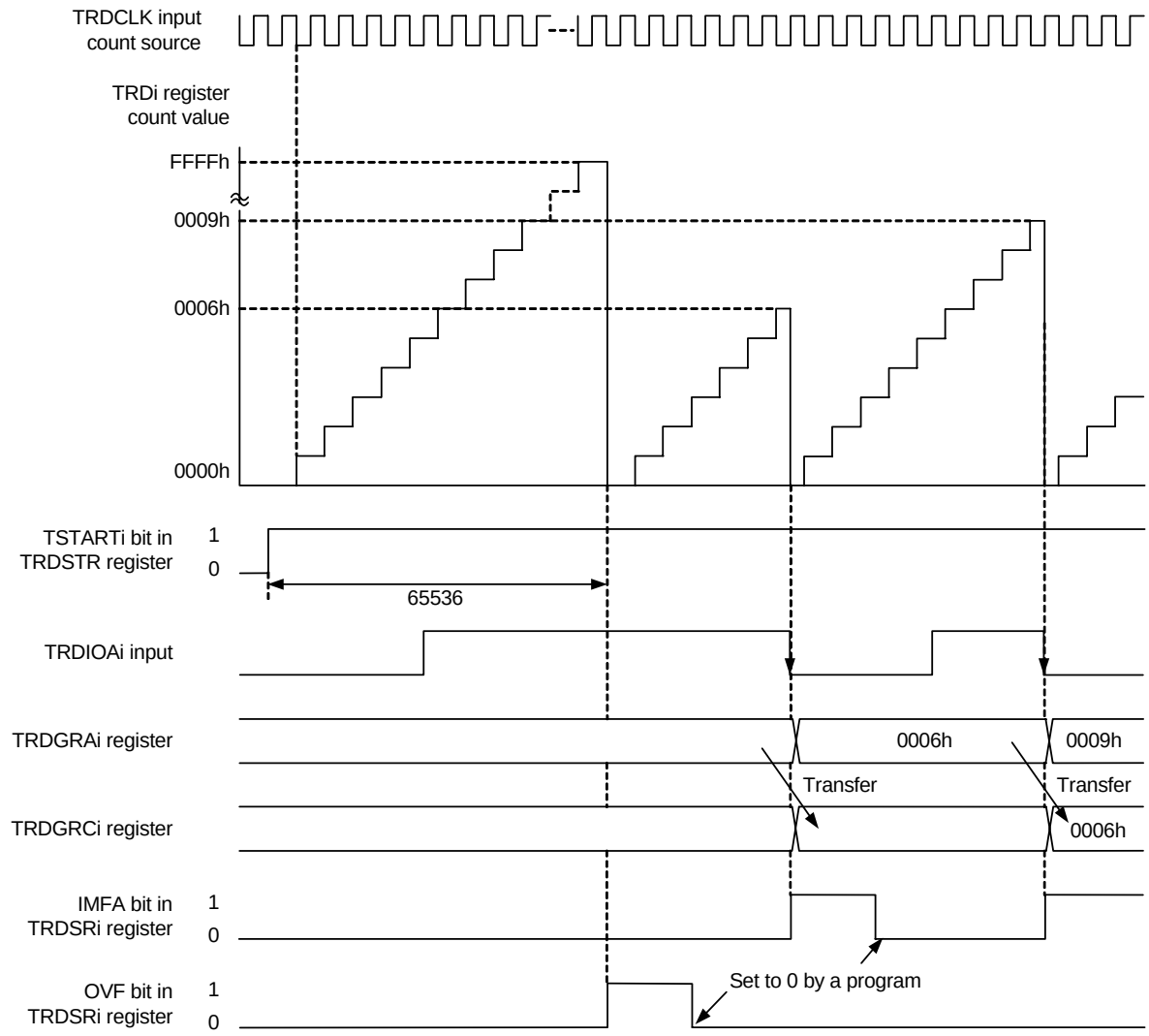
The input capture function measures the width or period of an external signal. An external signal input to the TRDIOji (i =0 or 1, j = A, B, C, or D) pin acts as a trigger for transferring the contents of the TRDi register (counter) to the TRDGRji register (input capture). Since this function is enabled with a combination of the TRDIOji pin and TRDGRji register, the input capture function, or any other mode or function, can be selected individually for each pin.
The TRDGRA0 register can also select fOCO128 as the input capture trigger input.

The output compare function detects matches (compare match) between the content of the TRDi (i = 0 or 1) register (counter) and the content of the TRDGRji (j = A, B, C, or D) register. When the contents match, a given level is output from the TRDIOji pin. Since this function is enabled with a combination of the TRDIOji pin and TRDGRji register, the output compare function, or any other mode or function, can be selected individually for each pin.

The setting conditions for this program are as follows:

- Channel used :This program uses only channel 0. Channel 1 is not used.
- Input capture input pin :TRDIOA0
- Output compare output pins :TRDIOB0 and TRDIOD0
- Timer RD synchronization :TRD0 and TRD1 operate independently
- TRDGRC0 register function :Buffer register of TRDGRA0 register
- TRDGRD0 register function :General register
- External clock input :Disabled
- Pin output enable :TRDIOB0 and TRDIOD0 pin output enabled; TRDIOA0 and TRDIOC0 pin output disabled
- Pulse output forced cutoff input :Disabled
- TRDIOB0 output level :Initial output “L”
- TRDIOD0 output level :Initial output “L”
- TRDIOA pin digital filter :Function is used; Clock is set as count source.
- Count source :f1
- TRD0 counter clear :Clear disabled (free-running operation)
- TRDGRA0 control :Input capture to TRDGRA0 at both edges
- Input capture input switch :TRDIOA0 pin input
- TRDGRB0 control :“H” output at TRDGRB0 compare match
- TRDGRD0 control :“H” output at TRDGRD0 compare match
- Interrupt enable :Interrupt by bits IMFA and OVF enabled; Interrupt by bits IMFB and IMFD disabled
- TRDGRB0 compare value
  :20000 – 1 (40 MHz × f2 (FRA2) × f1 (TCK0 to TCK2) × 20000 = 1 ms
  Compare match when 1 ms elapses after the TRD0 count starts
- TRDGRD0 compare value
  :40000 – 1 (40 MHz × f2 (FRA2) × f1 (TCK0 to TCK2) × 40000 = 2 ms
  Compare match when 2 ms elapses after the TRD0 count starts

Figure 3.1 shows an Operating Example of Input Capture Function and Figure 3.2 shows an Operating Example of Output Compare Function.

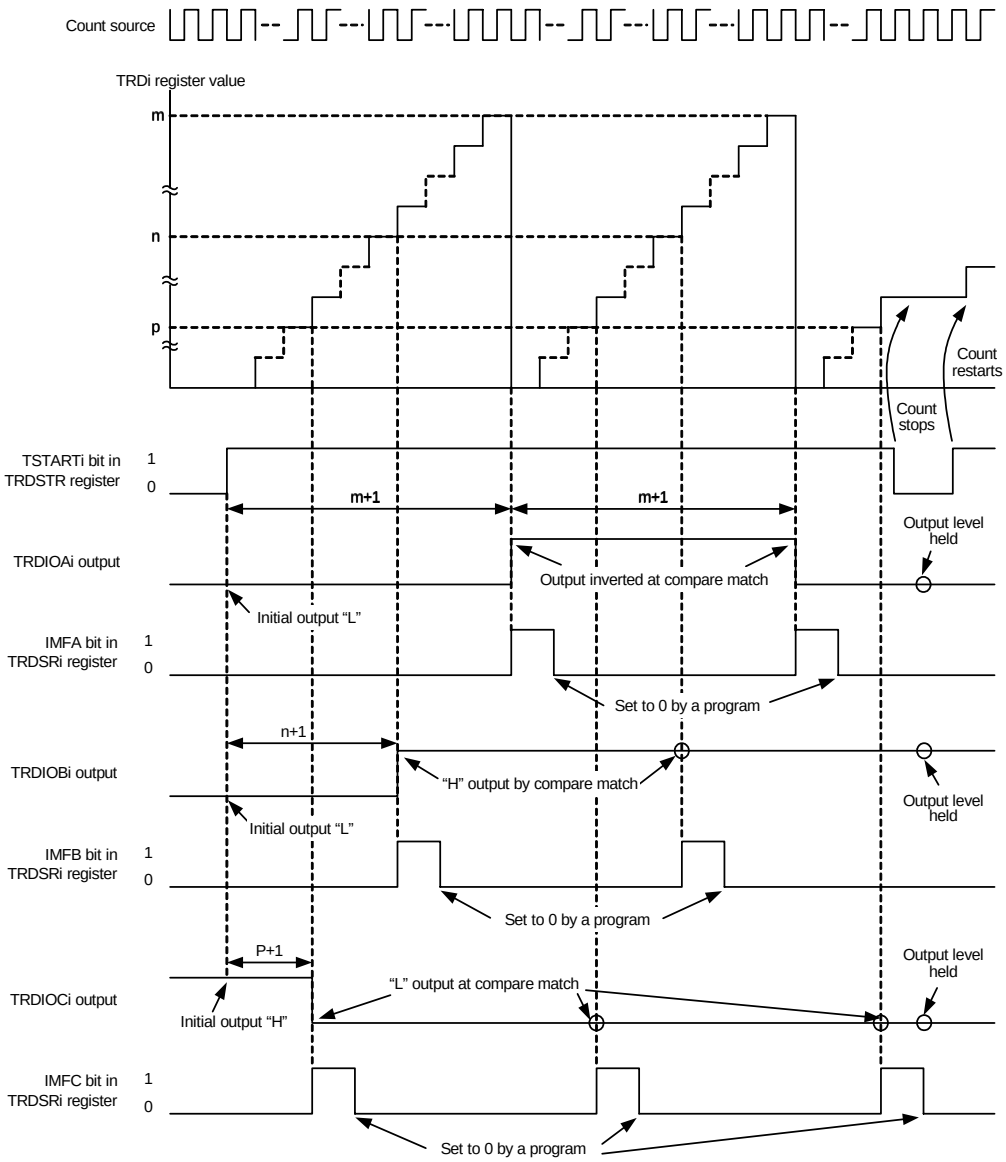


i = 0 or 1

The above applies under the following conditions:

Bits CCLR2 to CCLR0 in the TRDCRi register are set to 001b (the TRDi register is set to 0000h at the TRDGRAi register input capture).
Bits TCK2 to TCK0 in the TRDCRi register are set to 101b (TRDCLK input for the count source).
Bits CKEG1 to CKEG0 in the TRDCRi register are set to 01b (count at the falling edge for the count source).
Bits IOA2 to IOA0 in the TRDIORAi register are set to 101b (input capture at the falling edge of the TRDIOAi input).
The BFCi bit in the TRDMR register is set to 1 (the TRDGRCi register is used as a buffer register of the TRDGRAi register).

Figure 3.1 Operating Example of Input Capture Function



The above applies under the following conditions:
The CSELi bit in the TRDSTR register is set to 1 (the TRDi register does not stop at the counter clear compare match).
Bits BFCi and BFDi in the TRDMR register are set to 0 (registers TRDGRCi and TRDGRDi do not operate as buffers).
Bits EAi, EBi, and ECi in the TRDOER1 register are set to 0 (TRDIOAi, TRDIOBi, and TRDIOCi output enabled).
Bits CCLR2 to CCLR0 in the TRDCRi register are set to 001b (the TRDi register is set to 000h at the TRDGRAi register compare match).
Bits TOAi and TOBi in the TRDOCR register are set to 0 ("L" initial output until compare match) and the TOCi bit is set to 1 ("H" initial output until compare match).
Bits IOA2 to IOA0 in the TRDIORAi register are set to 011b (TRDIOAi output inverted at TRDGRAi register compare match).
Bits IOB2 to IOB0 in the TRDIORAi register are set to 010b ("H" TRDIOBi output at TRDGRBi register compare match).
Bits IOC3 to IOC0 in the TRDIORCi register are set to 1001b ("L" TRDIOCi output at TRDGRCi register compare match).
The IOD3 bit in the TRDIORCi register is set to 1 (the TRDGRDi register does not control the TRDIOBi pin output).

Figure 3.2 Operating Example of Output Compare Function

This sample program may include bit operations of unused functions for the SFR bit layout. Set these values according to the operating conditions of the user system.

3.1 Pins Used

Table 3.1 Pins Used and Their Function

Pin Name	I/O	Function
P2_0/TRDIOA0/TRDCLK	Input	Input capture input pin
P2_1/TRDIOB0	Output	Output compare output pin
P2_3/TRDIOD0	Output	Output compare output pin

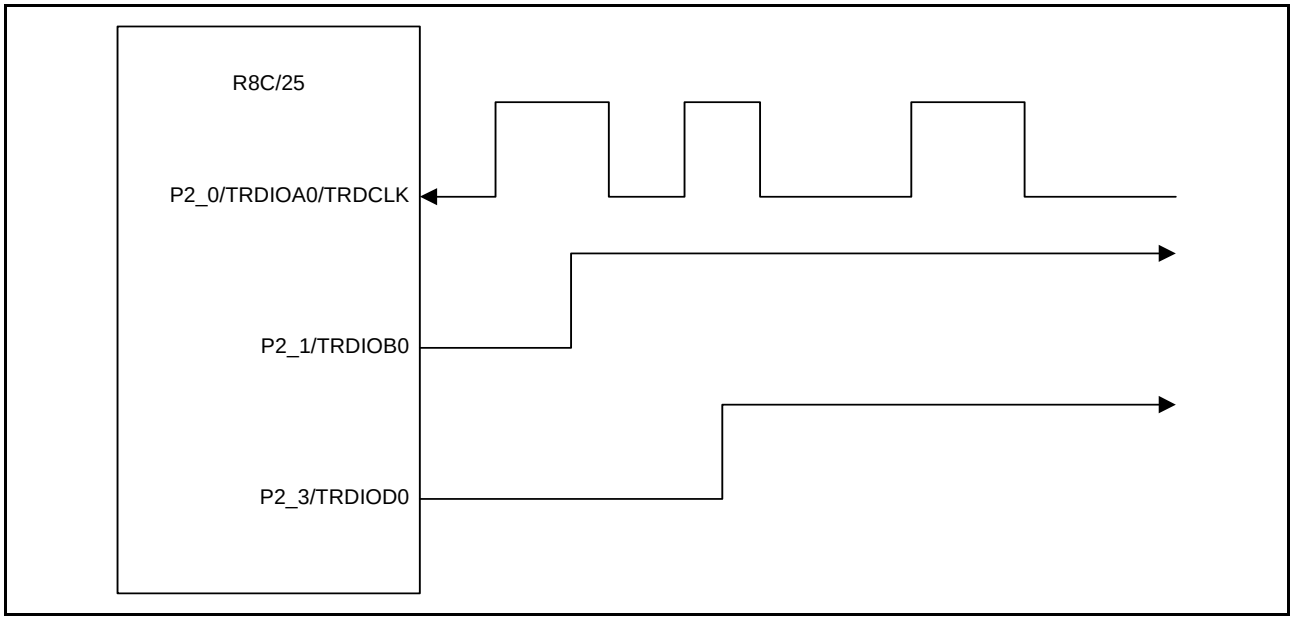


Figure 3.3 Pins Used

3.2 Memory Usage

Table 3.2 Memory Usage

Memory Usage	Size	Remarks
ROM	281 bytes	In main.c module
RAM	11 bytes	In main.c module
Maximum user stack usage	10 bytes	main function: 7 bytes timer_rd_init function: 3 bytes
Maximum interrupt stack usage	18 bytes	TRD0_int function: 18 bytes

Memory usage varies depending on the C compiler version and the compile option.
The above applies under the following conditions:

- C compiler: M16C/60, 30, 20, 10, Tiny, R8C/Tiny Series Compiler V.5.40 Release 00
- Compile option: -c -finfo; NOTE: -dir “$(CONFIGDIR)” -R8C

NOTE: Unavailable in the R8C/Tiny-exclusive free version.

4. Setup

This section shows the initial setting procedures and values to perform the example described in **3. Application Example Description**. Refer to the **R8C/25 Group Hardware Manual** for details on individual registers.

4.1 System Clock Setting

(1) Enable writing to registers CM0, CM1, OCD, FRA0, FRA1, and FRA2.

Protect Register

b7							b0		
							1	PRCR	[Address 000Ah]
								PRC0	Protect bit 0
									Writing to registers CM0, CM1, OCD, FRA0, FRA1, and FRA2 enabled

(2) Start the low-speed on-chip oscilltor.

System Clock Control Register 1

b7							b0		
			0					CM1	[Address 0007h]
								CM14	Low-speed on-chip oscillator oscillation stop bit
									Low-speed on-chip oscillator oscillates

(3) Set the division ratio of the high-speed on-chip oscillator clock.

High-Speed On-Chip Oscillator Control Register 2

b7							b0		
0	0	0	0	0	0	0	0	FRA2	[Address 0025h]
								FRA22 to FRA20	High-speed on-chip oscillator frequency switch bits
									Divide-by-2 mode
								($\overline{b7}$-$\overline{b3}$)	Reserved bits
									Set to 0.

(4) Start the high-speed on-chip oscilltor.

High-Speed On-Chip Oscillator Control Register 0

b7							b0		
							1	FRA0	[Address 0023h]
								FRA00	High-speed on-chip oscillator enable bit
									High-speed on-chip oscillator oscillates

(5) Wait until oscillation stabilizes.

(6) Select the high-speed on-chip oscillator.

High-Speed On-Chip Oscillator Control Register 0

b7							b0
						1	

FRA0 [Address 0023h]

FRA01 High-speed on-chip oscillator select bit

High-speed on-chip oscillator selected

(7) Set system clock division select bits 1.

System Clock Control Register 1

b7							b0
0	0						

CM1 [Address 0007h]

CM17 and CM16 System clock division select bits 1

No division mode

(8) Set system clock division select bit 0.

System Clock Control Register 0

b7							b0
	0						

CM0 [Address 0006h]

CM06 System clock division select bit 0

CM16 and CM17 enabled

(9) Disable writing to registers CM0, CM1, OCD, FRA0, FRA1, and FRA2.

Protect Register

b7							b0
							0

PRCR [Address 000Ah]

PRC0 Protect bit 0

Writing to registers CM0, CM1, OCD, FRA0, FRA1, and FRA2 disabled

4.2 Timer Mode (Input Capture and Output Compare Functions) Setting

(1) Set the port P2 direction register.

Port P2 Direction Register

b7							b0
							0

PD2 [Address 00E6h]

PD2_0 Port P2_0 direction bit
Input mode

(2) Set timer RD start register (TRD0 count stops).

Timer RD Start Register

b7							b0
0	0	0	0	1	1	0	0

TRDSTR [Address 0137h]

TSTART0 TRD0 count start flag
Count stops

TSTART1 TRD1 count start flag
Unavailable. Set to 0.

CSEL0 TRD0 count operation select bit
Set to 1 in the input capture function.

CSEL1 TRD1 count operation select bit
Unavailable. Set to 1.

($\overline{b7\text{-}b4}$) Nothing is assigned.
Set to 0.

NOTE:
1. Use the MOV instruction to set the TRDSTR register (do not use the bit handling instruction).

(3) Set the timer RD (channel 0) interrupt control register.

Timer RD (Channel 0) Interrupt Control Register

b7							b0
0	0	0	0	0	0	0	0

TRD0IC [Address 0048h]

ILVL2 to ILVL0 Interrupt priority level select bits 2 to 0
Level 0 (interrupt disabled)

IR Interrupt request bit
No interrupt request

($\overline{b7\text{-}b4}$) Nothing is assigned.
Set to 0.

(4) Set the timer RD mode register.

Timer RD Mode Register

b7							b0
0	0	0	1	0	0	0	0

TRDMR [Address 0138h]

SYNC	Timer RD synchronous bit TRD0 and TRD1 operate independently
($\overline{b3}$-$\overline{b1}$)	Nothing is assigned. Set to 0.
BFC0	TRDGRC0 register function select bit Buffer register of TRDGRA0 register
BFD0	TRDGRD0 register function select bit General register
BFC1	TRDGRC1 register function select bit Unavailable. Set to 0.
BFD1	TRDGRD1 register function select bit Unavailable. Set to 0.

(5) Set the timer RD PWM mode register.

Timer RD PWM Mode Register

b7							b0
0	0	0	0	0	0	0	0

TRDPMR [Address 0139h]

PWMB0	TRDIOB0 PWM mode select bit Set to 0 in timer mode.
PWMC0	TRDIOC0 PWM mode select bit Set to 0 in timer mode.
PWMD0	TRDIOD0 PWM mode select bit Set to 0 in timer mode.
($\overline{b3}$)	Nothing is assigned. Set to 0.
PWMB1	TRDIOB1 PWM mode select bit Unavailable. Set to 0.
PWMC1	TRDIOC1 PWM mode select bit Unavailable. Set to 0.
PWMD1	TRDIOD1 PWM mode select bit Unavailable. Set to 0.
($\overline{b7}$)	Nothing is assigned. Set to 0.

(6) Set the timer RD function control register.

Timer RD Function Control Register

b7						b0	
1	0					0	0

TRDFCR [Address 013Ah]

CMD1 and CMD0	Combination mode select bits	Set to 00b in timer mode.
OLS0	Normal-phase output level select bit	This bit is disabled in timer mode.
OLS1	Counter-phase output level select bit	This bit is disabled in timer mode.
ADTRG	A/D trigger enable bit	This bit is disabled in timer mode.
ADEG	A/D trigger edge select bit	This bit is disabled in timer mode.
STCLK	External clock input select bit	External clock input disabled
PWM3	PWM3 mode select bit	Set to 1 in timer mode.

(7) Set timer RD output master enable register 1.

Timer RD Output Master Enable Register 1

b7							b0
1	1	1	1	0	1	0	1

TRDOER1 [Address 013Bh]

EA0	TRDIOA0 output disable bit	This bit is disabled for use as input capture input
EB0	TRDIOB0 output disable bit	Output enabled
EC0	TRDIOC0 output disable bit	Output disabled (TRDIOC0 pin used as a programmable I/O port)
ED0	TRDIOD0 output disable bit	Output enabled
EA1	TRDIOA1 output disable bit	Output disabled (TRDIOA1 pin used as a programmable I/O port)
EB1	TRDIOB1 output disable bit	Output disabled (TRDIOB1 pin used as a programmable I/O port)
EC1	TRDIOC1 output disable bit	Output disabled (TRDIOC1 pin used as a programmable I/O port)
ED1	TRDIOD1 output disable bit	Output disabled (TRDIOD1 pin used as a programmable I/O port)

(8) Set timer RD output master enable register 2.

Timer RD Output Master Enable Register 2

b7							b0
0							

TRDOER2 [Address 013Ch]

PTO	Pulse output forced cutoff signal input $\overline{\text{INT0}}$ enable bit	
	0	Pulse output forced cutoff input disabled

(9) Set the timer RD output control register.

Timer RD Output Control Register

b7							b0
				0		0	

TRDOCR [Address 013Dh]

TOA0	TRDIOA0 output level select bit	
	0	Unavailable.
TOB0	TRDIOB0 output level select bit	
	0	Initial output “L”
TOC0	TRDIOC0 output level select bit	
	0	Unavailable.
TOD0	TRDIOD0 output level select bit	
	0	Initial output “L”
TOA1	TRDIOA1 output level select bit	
	0	Unavailable.
TOB1	TRDIOB1 output level select bit	
	0	Unavailable.
TOC1	TRDIOC1 output level select bit	
	0	Unavailable.
TOD1	TRDIOD1 output level select bit	
	0	Unavailable.

(10) Set timer RD digital filter function select register 0.

Timer RD Digital Filter Function Select Register 0

b7							b0	
1	1	0	0	0	0	0	1	TRDDF0 [Address 013Eh]

DFA	TRDIOA0 pin digital filter function select bit	Function used
DFB	TRDIOB0 pin digital filter function select bit	Function not used
DFC	TRDIOC0 pin digital filter function select bit	Function not used
DFD	TRDIOD0 pin digital filter function select bit	Function not used
($\overline{b5\text{-}b4}$)	Nothing is assigned.	Set to 0.
DFCK1 and DFCK0	Digital filter function clock select bits	Count source (clock selected by bits TCK2 to TCK0 in the TRDCR0 register)

(11) Set timer RD control register 0.

Timer RD Control Register 0

b7							b0	
0	0	0			0	0	0	TRDCR0 [Address 0140h]

TCK2 to TCK0	Count source select bits	f1 selected
CKEG1 and CKEG0	External clock edge select bits	Unavailable.
CCLR2 to CCLR0	TRD0 counter clear select bits	Clear disabled (free-running operation)

(12) Set timer RD I/O control register A0.

Timer RD I/O Control Register A0

b7	b6	b5	b4	b3	b2	b1	b0
0	0	1	0	1	1	1	0

TRDIORA0 [Address 0141h]

IOA1 and IOA0	TRDGRA control bits Input capture to TRDGRA0 at both edges
IOA2	TRDGRA mode select bit Set to 1 in the input capture function.
IOA3	Input capture input switch bit TRDIOA0 pin input
IOB1 and IOB0	TRDGRB control bits “H” output at TRDGRB0 compare match
IOB2	TRDGRB mode select bit Set to 0 in the output compare function.
($\overline{b7}$)	Nothing is assigned. Set to 0.

(13) Set timer RD/IO control register C0.

Timer RD I/O Control Register C0

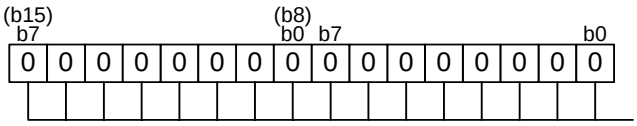
b7	b6	b5	b4	b3	b2	b1	b0
1	0	1	0	1	1		

TRDIORC0 [Address 0142h]

IOC1 and IOC0	TRDGRC control bits Unavailable.
IOC2	TRDGRC mode select bit To select 1 (buffer register of TRDGRA0 register) by the BFC0 bit in the TRDMR register, set the IOC2 bit in the TRDIORC0 register to the same value as the IOA2 bit in the TRDIORA0 register.
IOC3	TRDGRC register function select bit Set to 1 in the input capture function.
IOD1 and IOD0	TRDGRD control bits “H” output at TRDGRD0 compare match
IOD2	TRDGRD mode select bit Set to 0 in the output compare function.
IOD3	TRDGRD register select bit General register or buffer register

(14) Set timer RD counter 0.

Timer RD Counter 0



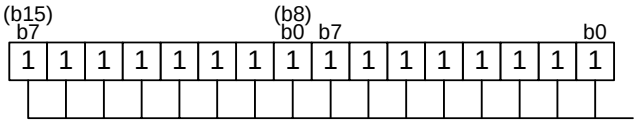
TRD0 [Address 0147h to 0146h]

Initialization

0 (0x0000) setting

(15) Set timer RD general register A0.

Timer RD General Register A0



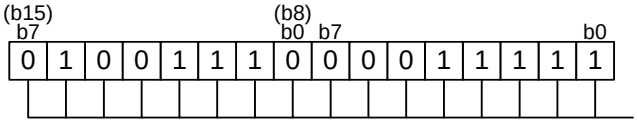
TRDGRA0 [Address 0149h to 0148h]

Initialization

0xFFFF setting

(16) Set timer RD general register B0.

Timer RD General Register B0



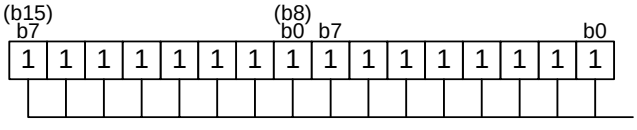
TRDGRB0 [Address 014Bh to 014Ah]

The compare value with the TRD0 register (counter) is stored

20000 – 1 (0x4E1F) setting

(17) Set timer RD general register C0.

Timer RD General Register C0



TRDGRC0 [Address 014Dh to 014Ch]

Initialization

0xFFFF setting

(18) Set timer RD general register D0.

Timer RD General Register D0

(b15) b7							(b8) b0	b7						b0
1	0	0	1	1	1	0	0	0	0	1	1	1	1	1	1

TRDGRD0 [Address 014F to 014Eh]

The compare value with the TRD0 register is stored

40000 – 1 (0x9C3F) setting

(19) Set timer RD interrupt enable register 0.

Timer RD Interrupt Enable Register 0

b7							b0
0	0	0	1	0	0	0	1

TRDIER0 [Address 0144h]

IMIEA	Input capture/compare match interrupt enable bit A Interrupt (IMIA) by IMFA bit enabled
IMIEB	Input capture/compare match interrupt enable bit B Interrupt (IMIB) by IMFB bit disabled
IMIEC	Input capture/compare match interrupt enable bit C Interrupt (IMIC) by IMFC bit disabled
IMIED	Input capture/compare match interrupt enable bit D Interrupt (IMID) by IMFD bit disabled
OVIE	Overflow/underflow interrupt enable bit Interrupt (OVI) by OVF bit enabled
($\overline{b7}$-$\overline{b5}$)	Nothing is assigned. Set to 0.

(20) Set timer RD status register 0.

Timer RD Status Register 0

b7	b6	b5	b4	b3	b2	b1	b0	TRDSR0 [Address 0143h]
0	0	0	0	0	0	0	0	

IMFA	Input capture/compare match flag A	Set to 0.
IMFB	Input capture/compare match flag B	Set to 0.
IMFC	Input capture/compare match flag C	Set to 0.
IMFD	Input capture/compare match flag D	Set to 0.
OVF	Overflow flag	Set to 0.
($\overline{b7}$-$\overline{b5}$)	Nothing is assigned.	Set to 0.

(21) Set the timer RD (channel 0) interrupt control register.

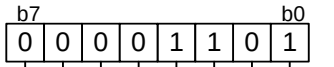
Timer RD (Channel 0) Interrupt Control Register

b7	b6	b5	b4	b3	b2	b1	b0	TRD0IC [Address 0048h]
0	0	0	0	0	1	1	1	

ILVL2 to ILVL0	Interrupt priority level select bits 2 to 0	Level 7
IR	Interrupt request bit	No interrupt request
($\overline{b7}$-$\overline{b4}$)	Nothing is assigned.	Set to 0.

(22) Set the timer RD start register (TRD0 count starts).

Timer RD Start Register



TRDSTR [Address 0137h]

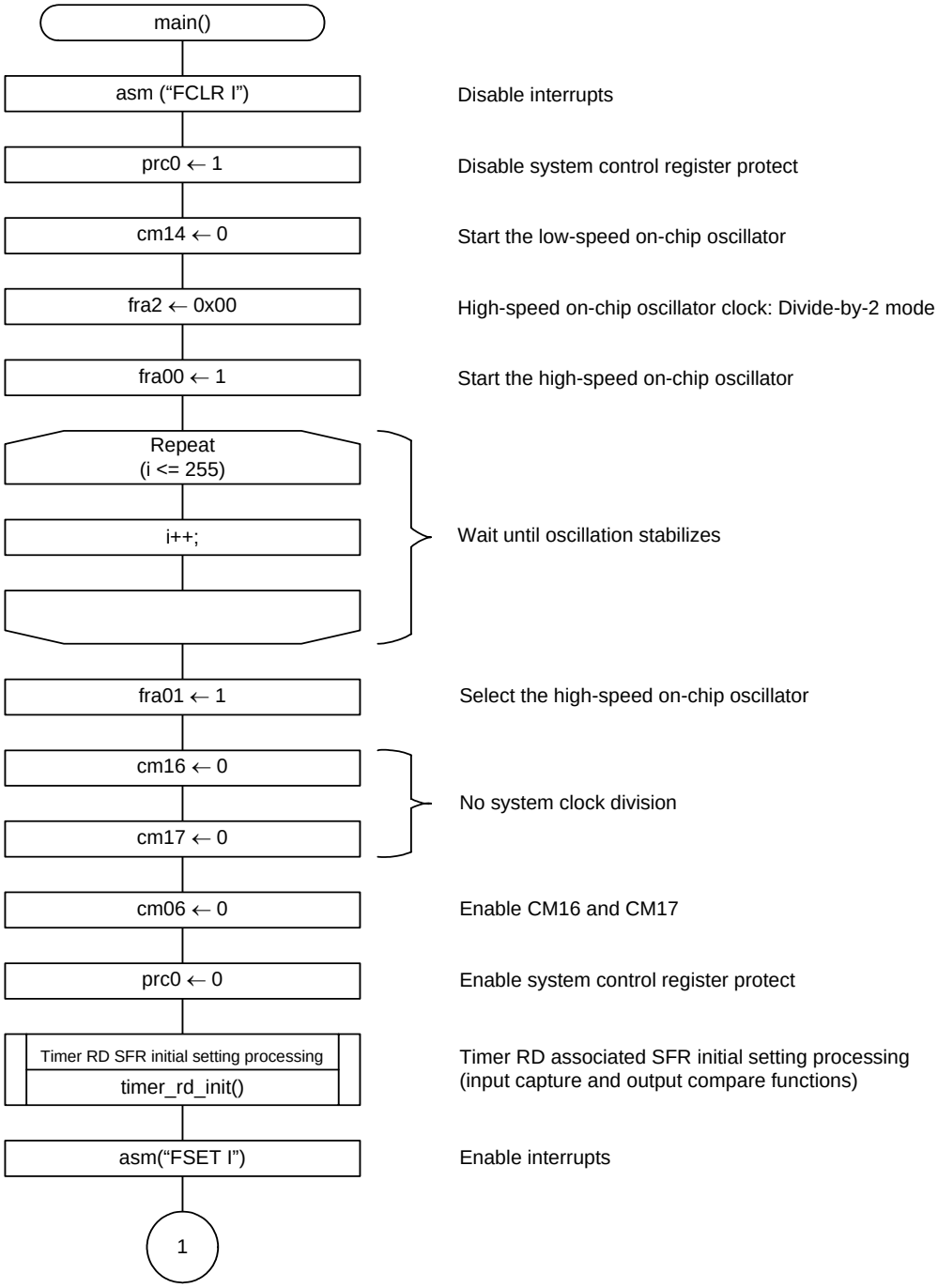
TSTART0	TRD0 count start flag Count starts
TSTART1	TRD1 count start flag Unavailable. Set to 0.
CSEL0	TRD0 count operation select bit Set to 1 in the input capture function.
CSEL1	TRD1 count operation select bit Unavailable. Set to 0.
($\overline{b7\text{-}b4}$)	Nothing is assigned. Set to 0.

NOTE:
1. Use the MOV instruction to set the TRDSTR register (do not use the bit handling instruction).

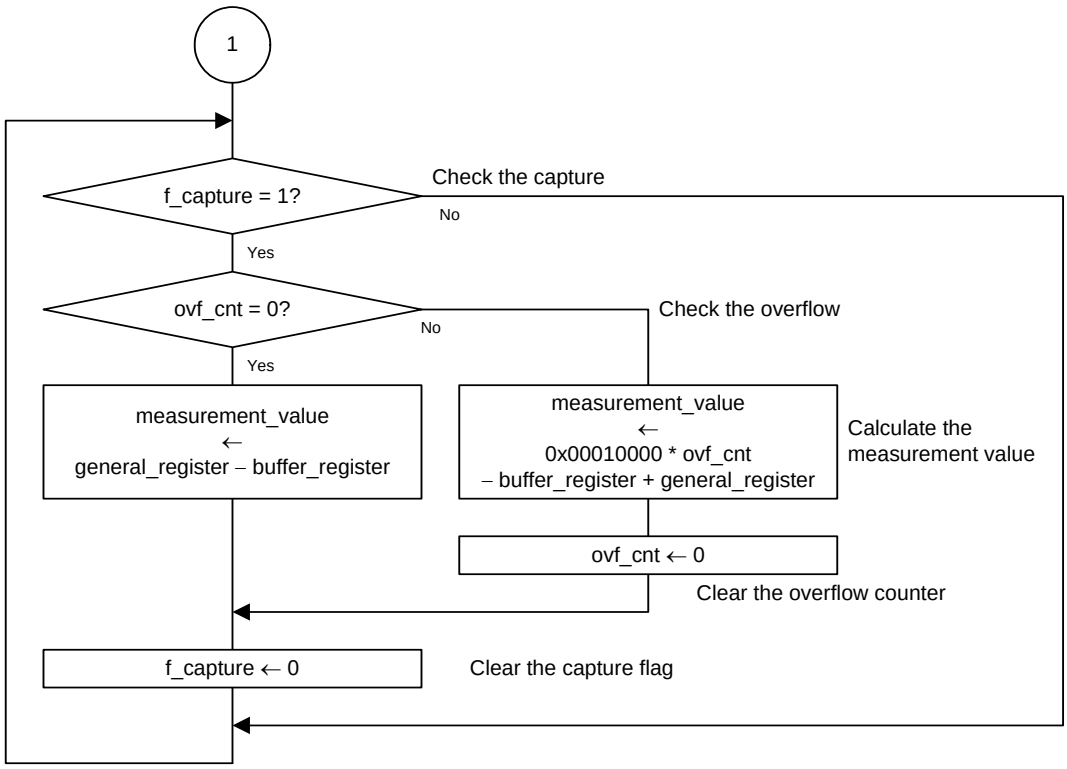
5. Flowchart

5.1 Main Function

5.1.1 Main Function 1

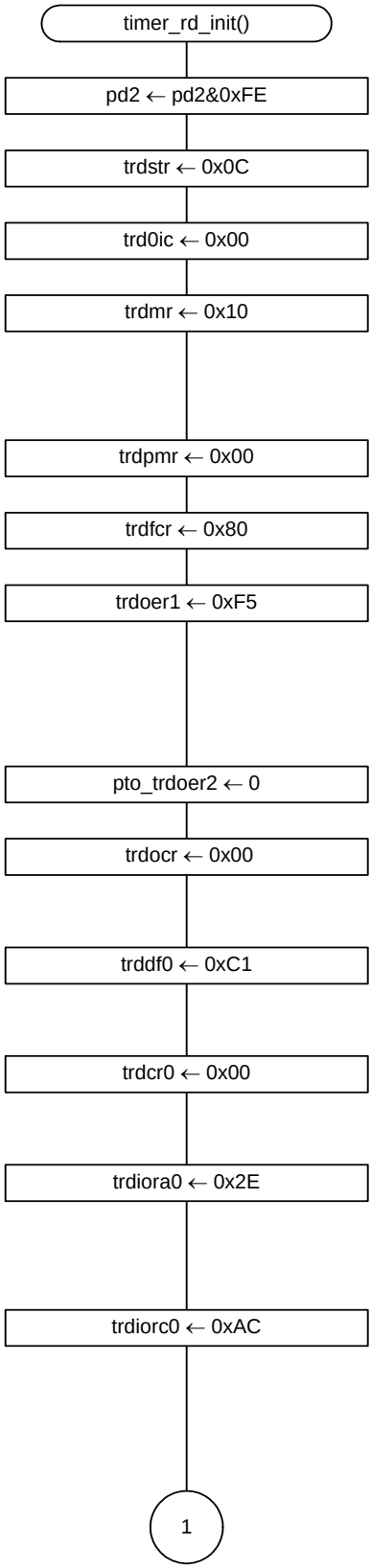


5.1.2 Main Function 2



5.2 Timer RD Associated SFR Initial Setting Processing

5.2.1 Timer RD Associated SFR Initial Setting Processing 1



P2_0 (TRDIOA0) pin: Set to an input port

Stop the TRD0 count

TRD0 interrupt: Interrupt level 0 (interrupt disabled)

Operate TRD0 and TRD1 independently
Operate the TRDGRC0 register as a buffer register of the TRDGRA0 register
Operate the TRDGRD0 register as a general register

Initialization

Disable the external clock input

TRDIOA0 pin: Disable output
TRDIOB0 pin: Enable output
TRDIOC0 pin: Disable output
TRDIOD0 pin: Enable output

Disable the pulse output forced cutoff input

TRDIOB0 pin: Initial output “L”
TRDIOD0 pin: Initial output “L”

TRDIOA pin: Digital filter function used
Digital filter function clock: Select the count source

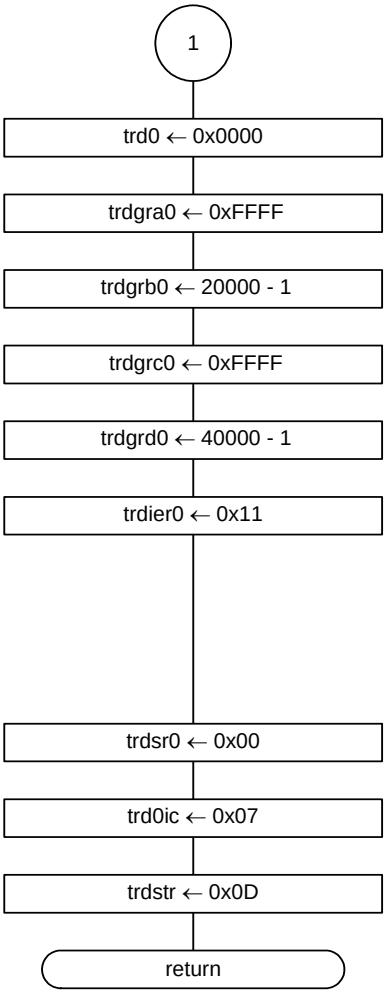
Count source: Select f1
TRD0 counter: Disable clear (free-running operation)

TRDIOA0 input: Input capture to TRDGRA0 at both edges
Input capture input: TRDIOA0 pin
Output “H” at the TRDGRB0 compare match

To select 1 (buffer register of TRDGRA0 register) by the BFC0 bit in the TRDMR register, set the IOC2 bit in the TRDIORC0 register to the same value as the IOA2 bit in the TRDIORA0 register.

Output “H” at the TRDGRD0 compare match

5.2.2 Timer RD Associated SER Initial Setting Processing 2



Initialize the TRD0 register count value to 0x0000.

Initialize the TRDGRA0 register count value to 0xFFFF.

Count period: Set to 1 ms (25 ns × f2 (FRA2) × f1 (TCK0 to TCK2) × 20000 = 1 ms)

Initialize the TRDGRC0 register count value to 0xFFFF.

Count period: Set to 2 ms (25 ns × f2 (FRA2) × f1 (TCK0 to TCK2) × 40000 = 2 ms)

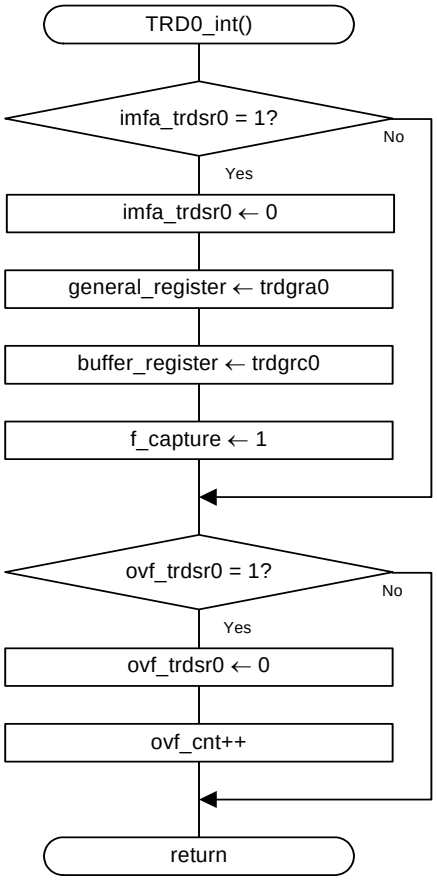
Enable interrupt (IMIA) by the IMFA bit
Disable interrupt (IMIB) by the IMFB bit
Disable interrupt (IMIC) by the IMFC bit
Disable interrupt (IMID) by the IMFD bit
Enable interrupt (OVI) by the OVF bit

Initialize timer RD status register 0

TRD0 interrupt: Interrupt priority level 7

Start the TRD0 count

5.3 Timer RD0 Interrupt Handling



Is an input capture signal to the TRDIOA0 pin detected?

Clear input capture flag A

Read the TRDGRA0 register

Read the TRDGRC0 register

Set the capture flag

Overflow?

Clear the overflow flag

Increment the overflow counter

6. Sample Programming Code

A sample program can be downloaded from the Renesas Technology website.
To download, click “Application Notes” in the left-hand side menu of the R8C/Tiny Series page.

7. Reference Documents

Hardware Manual
R8C/25 Group Hardware Manual
The latest version can be downloaded from the Renesas Technology website.

Technical Update/Technical News
The latest information can be downloaded from the Renesas Technology website.

Website and Support

Renesas Technology website
http://www.renesas.com/

Inquiries
http://www.renesas.com/inquiry
csc@renesas.com

REVISION HISTORY	R8C/25 Group Timer RD in Input Caputure and Output Compare Functions

Rev.	Date	Description	
		Page	Summary
1.00	June 29, 2007	–	First Edition issued

Notes regarding these materials

1. This document is provided for reference purposes only so that Renesas customers may select the appropriate Renesas products for their use. Renesas neither makes warranties or representations with respect to the accuracy or completeness of the information contained in this document nor grants any license to any intellectual property rights or any other rights of Renesas or any third party with respect to the information in this document.
2. Renesas shall have no liability for damages or infringement of any intellectual property or other rights arising out of the use of any information in this document, including, but not limited to, product data, diagrams, charts, programs, algorithms, and application circuit examples.
3. You should not use the products or the technology described in this document for the purpose of military applications such as the development of weapons of mass destruction or for the purpose of any other military use. When exporting the products or technology described herein, you should follow the applicable export control laws and regulations, and procedures required by such laws and regulations.
4. All information included in this document such as product data, diagrams, charts, programs, algorithms, and application circuit examples, is current as of the date this document is issued. Such information, however, is subject to change without any prior notice. Before purchasing or using any Renesas products listed in this document, please confirm the latest product information with a Renesas sales office. Also, please pay regular and careful attention to additional and different information to be disclosed by Renesas such as that disclosed through our website. (http://www.renesas.com)
5. Renesas has used reasonable care in compiling the information included in this document, but Renesas assumes no liability whatsoever for any damages incurred as a result of errors or omissions in the information included in this document.
6. When using or otherwise relying on the information in this document, you should evaluate the information in light of the total system before deciding about the applicability of such information to the intended application. Renesas makes no representations, warranties or guaranties regarding the suitability of its products for any particular application and specifically disclaims any liability arising out of the application and use of the information in this document or Renesas products.
7. With the exception of products specified by Renesas as suitable for automobile applications, Renesas products are not designed, manufactured or tested for applications or otherwise in systems the failure or malfunction of which may cause a direct threat to human life or create a risk of human injury or which require especially high quality and reliability such as safety systems, or equipment or systems for transportation and traffic, healthcare, combustion control, aerospace and aeronautics, nuclear power, or undersea communication transmission. If you are considering the use of our products for such purposes, please contact a Renesas sales office beforehand. Renesas shall have no liability for damages arising out of the uses set forth above.
8. Notwithstanding the preceding paragraph, you should not use Renesas products for the purposes listed below:
   (1) artificial life support devices or systems
   (2) surgical implantations
   (3) healthcare intervention (e.g., excision, administration of medication, etc.)
   (4) any other purposes that pose a direct threat to human life
   Renesas shall have no liability for damages arising out of the uses set forth in the above and purchasers who elect to use Renesas products in any of the foregoing applications shall indemnify and hold harmless Renesas Technology Corp., its affiliated companies and their officers, directors, and employees against any and all damages arising out of such applications.
9. You should use the products described herein within the range specified by Renesas, especially with respect to the maximum rating, operating supply voltage range, movement power voltage range, heat radiation characteristics, installation and other product characteristics. Renesas shall have no liability for malfunctions or damages arising out of the use of Renesas products beyond such specified ranges.
10. Although Renesas endeavors to improve the quality and reliability of its products, IC products have specific characteristics such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Please be sure to implement safety measures to guard against the possibility of physical injury, and injury or damage caused by fire in the event of the failure of a Renesas product, such as safety design for hardware and software including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other applicable measures. Among others, since the evaluation of microcomputer software alone is very difficult, please evaluate the safety of the final products or system manufactured by you.
11. In case Renesas products listed in this document are detached from the products to which the Renesas products are attached or affixed, the risk of accident such as swallowing by infants and small children is very high. You should implement safety measures so that Renesas products may not be easily detached from your products. Renesas shall have no liability for damages arising out of such detachment.
12. This document may not be reproduced or duplicated, in any form, in whole or in part, without prior written approval from Renesas.
13. Please contact a Renesas sales office if you have any questions regarding the information contained in this document, Renesas semiconductor products, or if you have any other inquiries.