R32C/100 Series

Timer A Operation Using the Gate Function in Timer Mode

R01AN0177EJ0100
Rev.1.00
Oct. 30, 2010

1. Abstract

This document describes the gate function in timer Ai mode for controlling count start and count stop by the level specified by the input level on the TAiIN pin (i = 0 to 4).

2. Introduction

The application example described in this document applies to the following microcomputers (MCUs):

MCUs: R32C/116 Group, R32C/117 Group, and R32C/118 Group

This application note can be used with other R32C/100 Series MCUs which have the same special function registers (SFRs) as the above groups. Check the manuals for any modifications to functions. Careful evaluation is recommended before using the program described in this application note.

3. Application Example

This section describes how to count using the timer while the input level on the TA0IN pin is held at high. Table 3.1 lists the Clock Frequency Settings.

Table 3.1 Clock Frequency Settings

Clock	Frequency
Main clock	16 MHz
PLL clock	100 MHz
Base clock	50 MHz
CPU clock	50 MHz
Peripheral bus clock	25 MHz
Peripheral function clock source	25 MHz

3.1 Explanation

(1) When the TA0S bit in the TABSR register is 1 (count started) and the input signal to the TA0IN pin is held at high, the counter decrements the count source.

(2) When the input signal to the TA0IN pin is held at low, the counter holds its count value and stops.

(3) If the counter underflows, the counter reloads the settings of the reload register and continues counting. At the same time, the IR bit in the TA0IC register becomes 1 (interrupt requested).

(4) Setting the TA0S bit to 0 (count stopped) causes the counter to hold and stop its count value.

Notes:
1. The pulse width of pulses input to the TA0IN pin should be two or more cycles of the count source.
2. When using timers A1, A2, and A4, set the IFS00 bit in the IFS0 register to assign pins TA1IN, TA2IN, and TA4IN to a corresponding port.

Figure 3.1 shows Timer Mode Operation When the Gate Function is Selected.

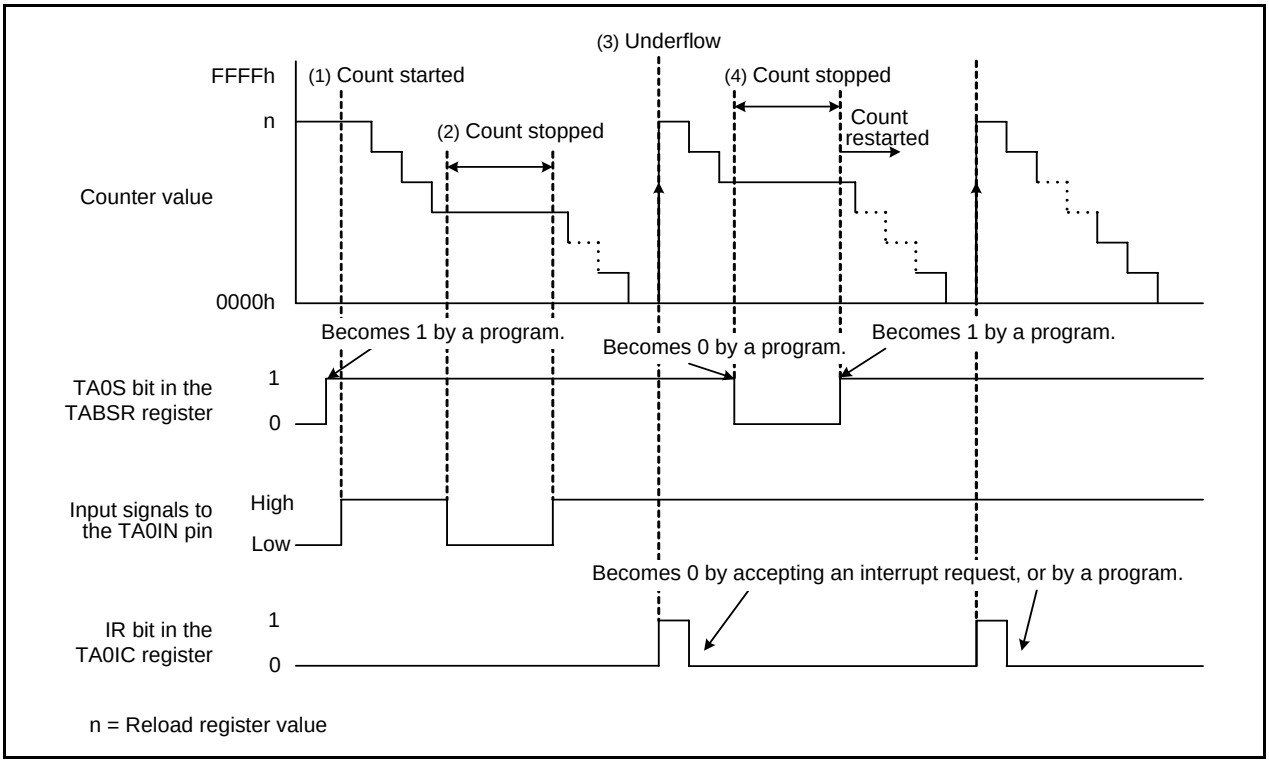
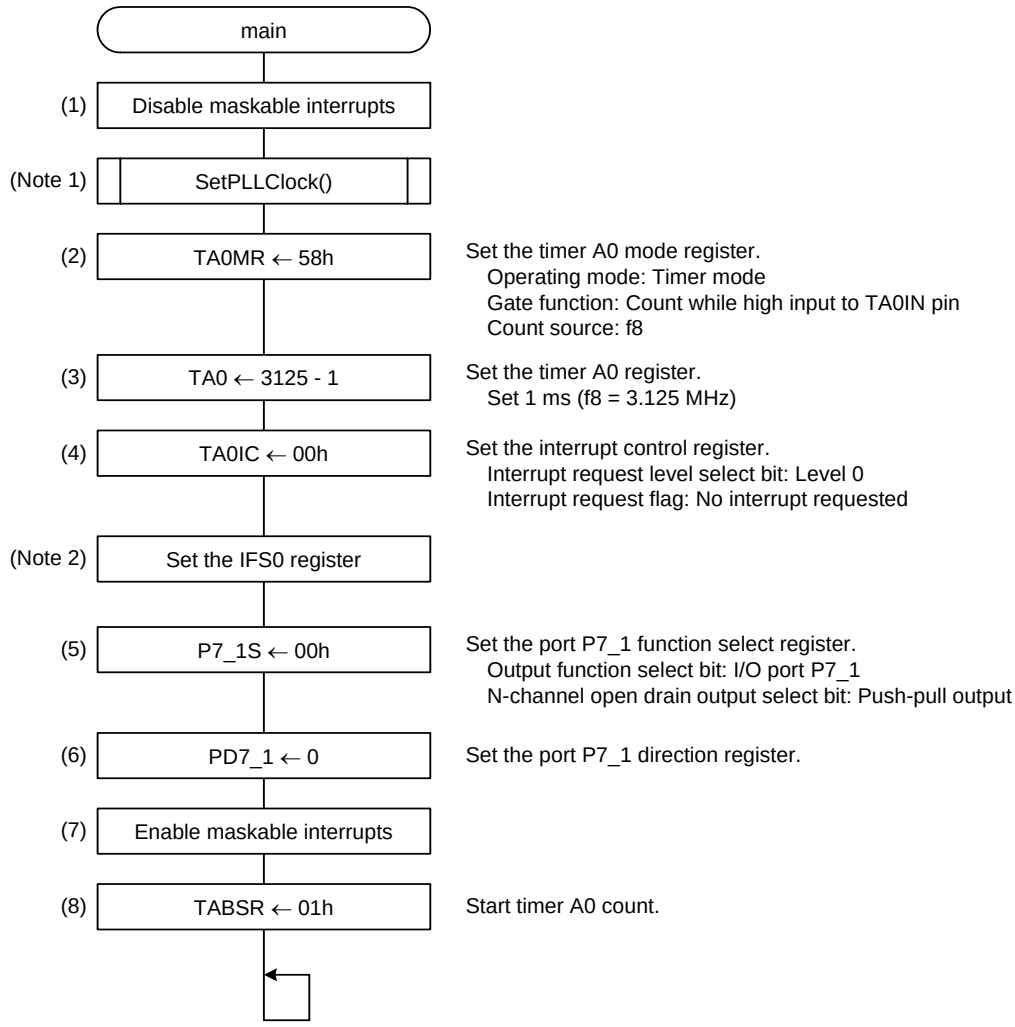


Figure 3.1 Timer Mode Operation When the Gate Function is Selected

3.2 Flowchart

Figure 3.2 shows the Main Function.



Notes:
1. Refer to the hardware user's manual for initializing the clock.
2. When using timers A1, A2, and A4, set the IFS00 bit in the IFS0 register to assign pins TA1IN, TA2IN, and TA4IN to a corresponding port.

Figure 3.2 Main Function

4. Sample Program

A sample program can be downloaded from the Renesas Electronics website.

5. Reference Documents

User's Manuals
R32C/116 Group User's Manual: Hardware Rev.1.00
R32C/117 Group User's Manual: Hardware Rev.1.00
R32C/118 Group User's Manual: Hardware Rev.1.00
The latest versions can be downloaded from the Renesas Electronics website.

Technical Update/Technical News
The latest information can be downloaded from the Renesas Electronics website.

C Compiler Manual
R32C/100 Series C Compiler Package V.1.02 C Compiler User's Manual Rev.2.00
The latest version can be downloaded from the Renesas Electronics website.

Website and Support

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REVISION HISTORY	R32C/100 Series Timer A Operation Using the Gate Function in Timer Mode

Rev.	Date	Description	
		Page	Summary
1.00	Oct. 30, 2010	-	First edition issued

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

   — The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

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