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# H8SX Family

## Synchronous DRAM interface

### Introduction

The DRAM interface is employed to connect synchronous RAM to an H8SX microcontroller.

### Target Device

H8SX/1663 Group

### Preface

The writing of this application note is in accord with the hardware manual for the H8SX/1663 Group. The program covered in this application note can be run on the target device indicated above. However, since some functional modules may be changed for the addition of functionality etc., be sure to perform a thorough evaluation by confirming the details with the hardware manual for the target device.

### Contents

## 1. Specification

A synchronous DRAM interface can be implemented by setting the bus controller (BSC) of the H8SX/1664 microcontroller so that area 2 of external space is treated as a synchronous DRAM space. Up to 8 Mbytes (64 Mbits) of synchronous DRAM are directly connectable via the synchronous DRAM interface, which allows for synchronous DRAM with CAS latencies from two to four.

- In this example we employ the synchronous DRAM interface to initialize synchronous DRAM.
- The H8SX/1664 microcontroller and synchronous DRAM are connected via a 16-bit-wide bus.
- The circuit for connection of synchronous DRAM is shown in figure 1, and table 1 gives the specifications of the synchronous DRAM used in this task.

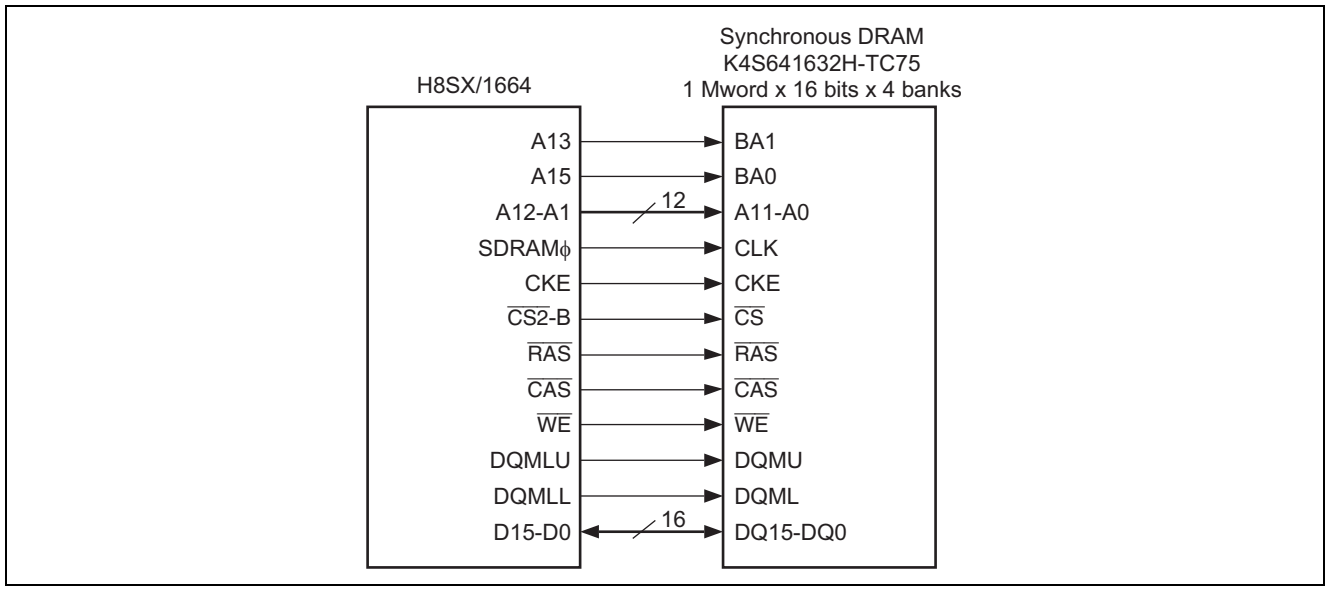



**Figure 1 Example of a Circuit for Synchronous DRAM Connection**

**Table 1 Specifications of the Synchronous DRAM**

| Item | Description |
|---|---|
| Product name | K4S641632H-TC75 (Samsung Electronics) |
| Configuration | 1 Mword × 16 bits × 4 banks |
| Capacity | 64 Mbits |
| CAS latency | 2 or 3 (programmable) |
| Refresh interval | 4096 refresh cycles every 64 ms |
| Row address | A11 – A0 |
| Column address | A7 – A0 |
| Number of banks | Four; operation is controlled by BA0, BA1. |

## 2. Applicable Conditions

**Table 2 Applicable Conditions**

| Item | Description |
|---|---|
| Operating frequency | Input clock: 12 MHz<br>System clock (Iϕ): 48 MHz<br>Peripheral module clock (Pϕ): 24MHz<br>External bus clock (Bϕ): 48MHz |
| Operating mode | Mode 6 (MD2 = 1, MD1 = 1, MD0 = 0)<br>SDRAM interface enabled (MD3 = 1) |

# 3. Description of Functions Used

## 3.1 Synchronous DRAM Interface

Area 2 can be specified as an SDRAM space by using the DRAME and DTYPE bits in DRAMCR. Table 3 lists the relationships between the settings of the DRAME and DTYPE bits and the way the area 2 interface functions.
In the SDRAM space, pins PB2, PB3, and PB4 are used as the $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ signals. A PFCR setting selects the PB1 pin for the CS2 signal, and setting the OEE bit in DRAMCR to 1 selects the PB5 pin for the CKE signal.
The bus specifications for the SDRAM space depend on the settings for area 2. Neither pin-controlled nor program-controlled wait insertion is available for the SDRAM space.

Through combinations of the $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ signals and the precharge-sel command (Precharge-sel) that produces output on the higher-order bits of the column address, commands for synchronous DRAM are possible.

The H8SX/1664 supports the following commands. It does not support commands for bank control.

- NOP
- Auto-refresh (REF)
- Self-refresh (SELF)
- All-bank precharge (PALL)
- Bank active (ACTV)
- Read (READ)
- Write (WRIT)
- Mode register setting (MRS)

**Table 3 Relationship between the DRAME and DTYPE Settings and the Area 2 Interface**

| DRAME | DTYPE | Area 2 Interface |
|---|---|---|
| 0 | X | Basic bus space (initial state)/byte-control SRAM space |
| 1 | 0 | DRAM space |
| 1 | 1 | SDRAM space |

[Legend] X: Don't care

## 3.2 Memory Map

The 16-Mbyte address space is divided into eight areas for the bus controller, so that bus control for access to the external address space is implemented in area units. Chip-selection signals (CS0–CS7) can be output the respective areas.

Figure 2 shows how the 16-Mbyte space is divided into areas. In this example, an 8-Mbyte synchronous DRAM is connected in area 2.

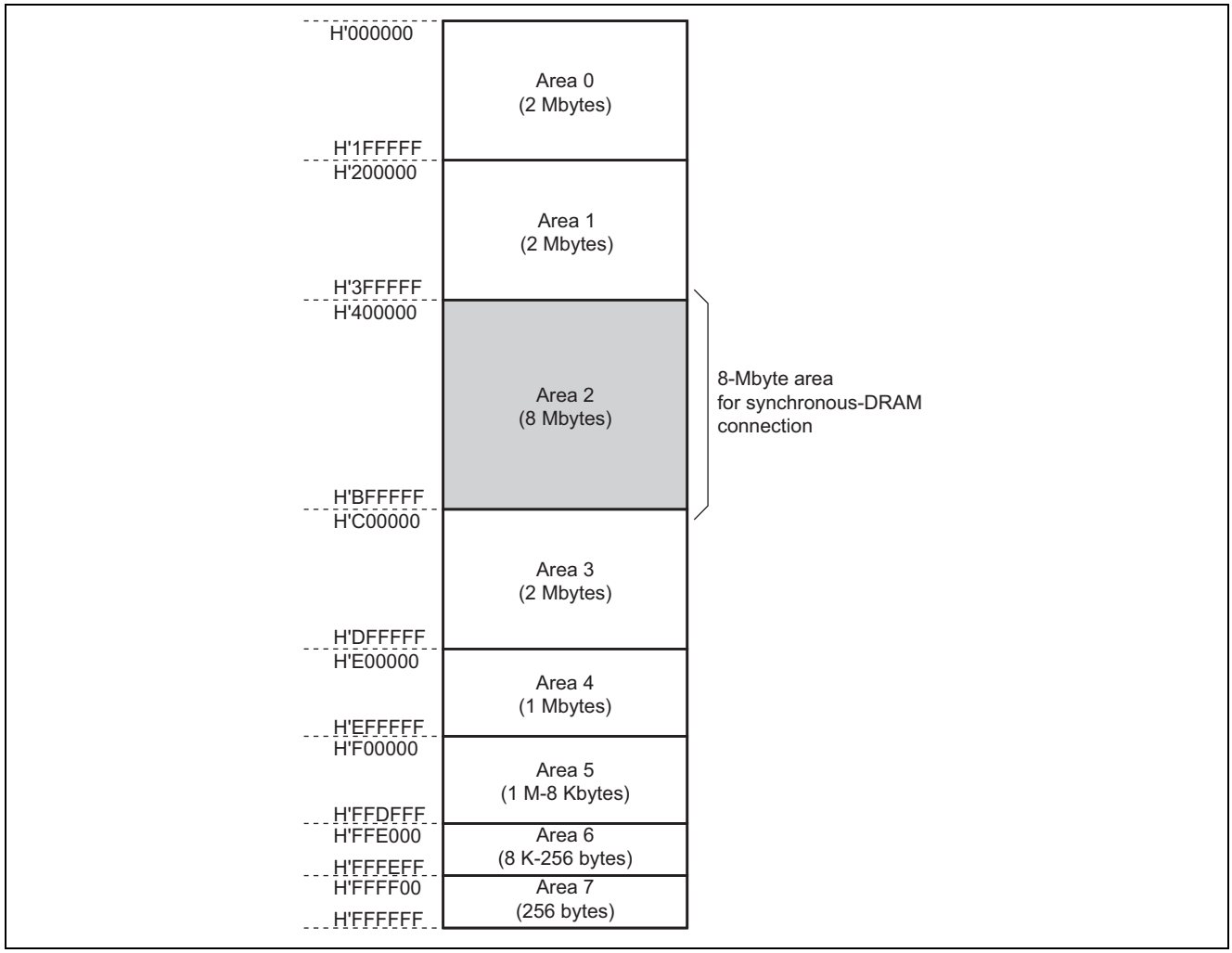



**Figure 2 Memory Map**

## 3.3 Address-Multiplexed Bus

Row and column addresses for the synchronous DRAM space are multiplexed. In address multiplexing, the MXC1 and MXC0 bits of DRAMCR define an amount of shift for the row addresses. Furthermore, when settings for the synchronous DRAM interface are made, higher-order bits of the column address are used in output of the address-precharge setting command (Precharge-sel). Table 4 shows the output pins for multiplexed addresses when the row addresses are shifted by eight bits (MXC1 = 0, MXC0 = 0) and the data-bus width is 16 bits.

**Table 4 Multiplexed-Address Output (Amount of Shift: 8 Bits, Data-Bus Width: 16 Bits)**

| H8SX/1664 pin | Row Address | Column Address | SDRAM Pin | Function |
|---|---|---|---|---|
| A15 | A23 | A23 | BA0 | Bank specification |
| A14 | A22 | A22 | – | Not used |
| A13 | A21 | A21 | BA1 | Bank specification |
| A12 | A20 | A20 | A11 | Address |
| A11 | P/A19 | P | A10 | Address/precharge setting |
| A10 | A18 | A10 | A9 | Address |
| A9 | A17 | A9 | A8 | Address |
| A8 | A16 | A8 | A7 | Address |
| A7 | A15 | A7 | A6 | Address |
| A6 | A14 | A6 | A5 | Address |
| A5 | A13 | A5 | A4 | Address |
| A4 | A12 | A4 | A3 | Address |
| A3 | A11 | A3 | A2 | Address |
| A2 | A10 | A2 | A1 | Address |
| A1 | A9 | A1 | A0 | Address |
| A0 | A8 | A0 | – | Not used |

## 3.4 Specifying Banks

In this example, row-address signal A23 is connected to bank-address pin BA0, and row-address signal A21 is connected to bank-address pin BA1. Table 5 shows the relationship between address ranges in area 2 memory and banks A to D of the synchronous DRAM.

**Table 5 Specifying Banks**

| Address in Area 2 Memory | Row Address | | | Bank Address | | Bank of the Synchronous DRAM |
|---|---|---|---|---|---|---|
| | A23 | A22 | A21 | BA0 | BA1 | |
| H'400000–H'5FFFFF | 0 | 1 | 0 | Low | Low | Bank A |
| H'600000–H'7FFFFF | 0 | 1 | 1 | Low | High | Bank B |
| H'800000–H'9FFFFF | 1 | 0 | 0 | High | Low | Bank C |
| H'A00000–H'BFFFFF | 1 | 0 | 1 | High | High | Bank D |

## 3.5 Mode Register of the Synchronous DRAM

The H8SX/1664 microcontroller does not support burst read and burst write modes for synchronous DRAM. When setting the mode register of the synchronous DRAM, select burst read/single write with a burst length of one. Ensure that the settings of the mode register for the synchronous DRAM match the settings for the bus controller. Figure 3 and table 6 to 9 give examples of values to place in the mode register.

| | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | OPCODE | | | | | 0 | LMODE | | | BT | BL | | | |
| Address pins of the synchronous DRAM | BA1 | BA0 | A10 | A9 | A8 | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 | |
| Address pins of the H8SX/1664 | A13 | A15 | A11 | A10 | A9 | A8 | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 |

**Figure 3 Placement of Bits in the Mode Register (16-Bit Bus Width)**

**Table 6 OPCODE (Operation Code)**

| BA1 | BA0 | A10 | A9 | A8 | Write-Mode Setting | Possible with the H8SX/1664? |
|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | Burst read/burst write | No |
| 0 | 0 | X | 0 | 1 | (Reserved) | No |
| 0 | 0 | X | 1 | 0 | Burst read/single write | Yes |
| 0 | 0 | X | 1 | 1 | (Reserved) | No |

[Legend] X: Don't care

**Table 7 LMODE (CAS Latency Setting)**

| A6 | A5 | A4 | CAS latency | Possible with the H8SX/1664? |
|---|---|---|---|---|
| 0 | 0 | 0 | (Reserved) | No |
| 0 | 0 | 1 | (Reserved) | No |
| 0 | 1 | 0 | 2 | Yes |
| 0 | 1 | 1 | 3 | Yes |
| 1 | X | X | (Reserved) | No |

[Legend] X: Don't care

**Table 8 BT (Burst Type)**

| A3 | Burst Type | Possible with the H8SX/1664? |
|---|---|---|
| 0 | Sequential | Don't care |
| 1 | Interleaved | Don't care |

**Table 9 BL (Burst Length)**

| A2 | A1 | A0 | Burst Length | Possible with the H8SX/1664? |
|---|---|---|---|---|
| 0 | 0 | 0 | 1 | Yes |
| 0 | 0 | 1 | 2 | No |
| 0 | 1 | 0 | 4 | No |
| 0 | 1 | 1 | 8 | No |
| 1 | 0 | 0 | (Reserved) | No |
| 1 | 0 | 1 | (Reserved) | No |
| 1 | 1 | 0 | (Reserved) | No |
| 1 | 1 | 1 | BT = 0: Full page<br>BT = 1: (reserved) | No |

## 3.6 Power-on Sequence

To use the synchronous DRAM, mode settings must be made after power has been supplied.

Setting the MRSE bit in SDCR to one enables setting of the synchronous DRAM's mode register and thus its mode. After that, writing of bytes to the synchronous DRAM space proceeds. In the table below, x indicates the value to be set in the synchronous DRAM's mode register, and writing to locations in the corresponding spaces will set the value x in the mode register.

**Table 10 Addresses for Writing to the Mode Register of the Synchronous DRAM**

| Bus Configuration of the Synchronous DRAM | Addresses for Writing to the Synchronous DRAM |
|---|---|
| 8 bits | Locations of the form H'4000000/H'400000 + x |
| 16 bits | Locations of the form H'4000000/H'400000 + 2x |

The mode register of the synchronous DRAM takes in settings from address signals at the point where an MRS is issued.

Figure 4 illustrates timing of mode settings for the synchronous DRAM. Addresses in area 2 at the time of write access to the synchronous DRAM's mode register are listed in table 11.

**Table 11 Access to Synchronous DRAM Addresses in Writing to the Mode Register (Area 2)**

| Data-Bus Width | CAS Latency | Burst Read/Single Write (Burst Length = 1) | |
|---|---|---|---|
| | | Address | External Address Pins |
| 8 bit | 2 | H'400220 | H'0220 |
| | 3 | H'400230 | H'0230 |
| 16 bit | 2 | H'400440 | H'0440 |
| | 3 | H'400460 | H'0460 |

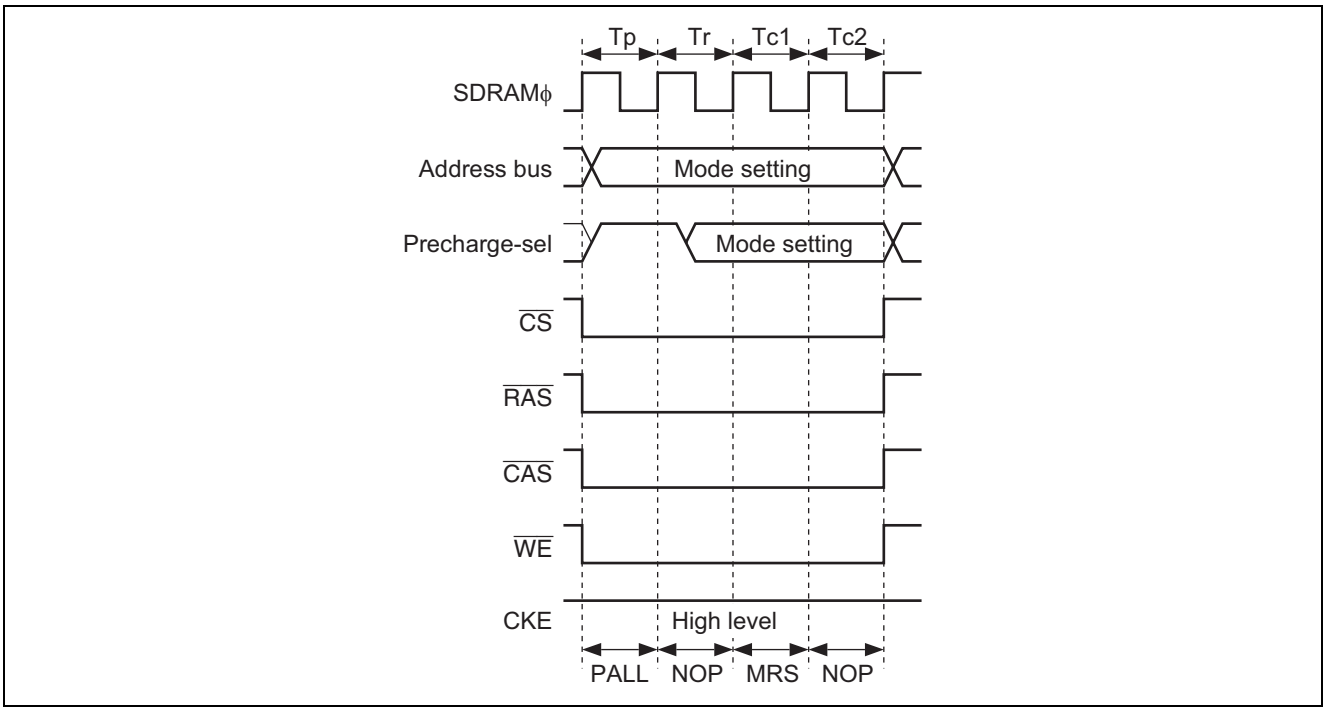



**Figure 4 Timing of Mode Settings for the Synchronous DRAM**

The settings given below are made for the mode register of the synchronous DRAM in this example. In this case, the setting of the mode register is made by access to address H'400460.

Figure 5 shows the connection between the setting for the mode register and the address for access.

- Burst length: Burst read/single write (burst length 1)
- Data bus width: 16 bits
- Burst type: Sequential
- CAS latency: 3 cycles

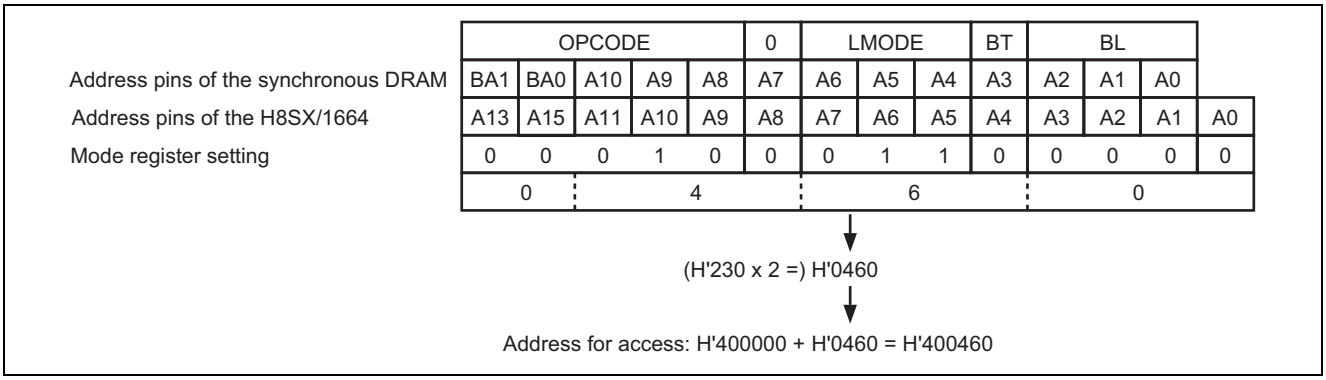



**Figure 5 Connection between Mode Register Setting and Address for Access**

# 4. Principles of Operation

## 4.1 Timing of Read Operations

Figure 6 shows an example of timing for single-read access to the synchronous DRAM in this sample application.

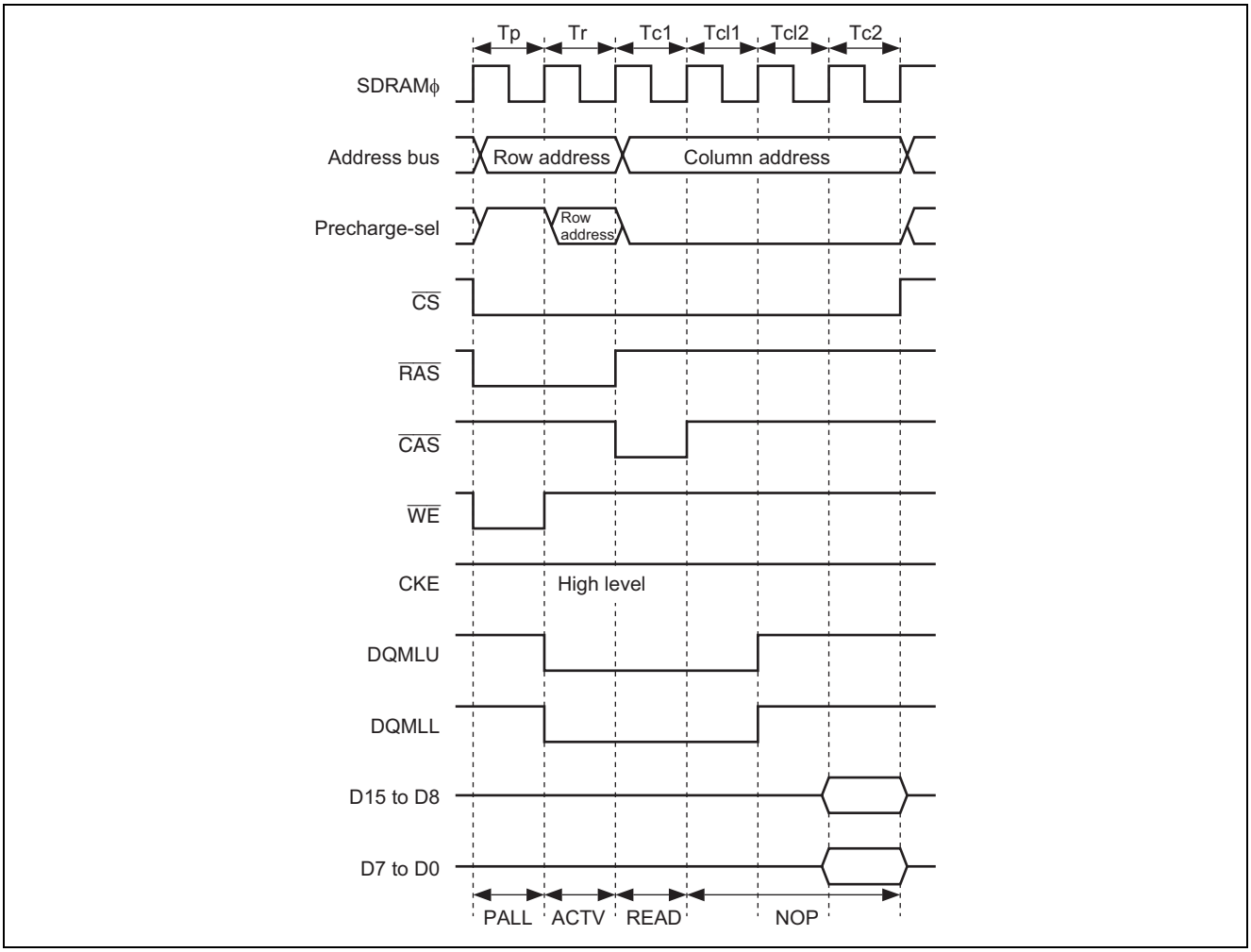



**Figure 6 Timing of Single-Read Access to the Synchronous DRAM**

## 4.2 Timing of Write Operations

Figure 7 shows an example of timing for single-write access to the synchronous DRAM in this sample application.

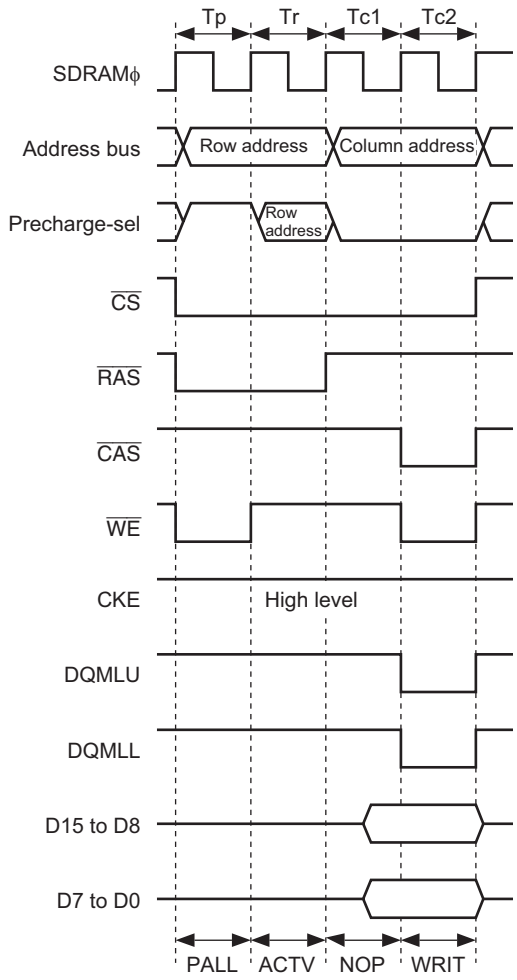



**Figure 7 Timing of Single-Write Operation for the Synchronous DRAM (Example)**

# 5. Description of Software

## 5.1 Operating Environment

**Table 12 Operating Environment**

| Item | Description |
|---|---|
| Development tool | High-performance Embedded Workshop Ver.4.01.01 |
| C/C++ compiler | H8S, H8/300 Series C/C++ Compiler Ver.6.01.02<br>(manufactured by Renesas Technology) |
| Compiler options | -cpu = h8sxa:24:md, -code = machinecode, -optimize = 1, -regparam = 3<br>-speed = (register, shift, struct, expression) |

**Table 13 Section Settings**

| Address | Section Name | Description |
|---|---|---|
| H'001000 | P | Program area |
| H'400000 | BCS2 | Area 2, synchronous DRAM area |
| H'FF6000 | B | Non-initialized data area (RAM area) |

**Table14 Vector Table for Exception Handling**

| Source for Exception Handling | Vector Number | Address of Vector-Table Entry | Destination Function |
|---|---|---|---|
| Reset | 0 | H'000000 | init |

## 5.2 List of Functions

**Table 15 Functions in File main.c**

| Function Name | Purpose |
|---|---|
| init | Initialization routine<br>Sets the CCR and configures the clocks, releases the required modules from module stop mode, and calls the main function. |
| main | Main routine<br>Calls the BscInit function, handles processing to confirm access to the synchronous DRAM (SDRAM). |
| BscInit | Synchronous DRAM (SDRAM) initialization |

## 5.3 RAM Usage

**Table 16 RAM Usage**

| Type | Variable Name | Description | Used in Function: |
|---|---|---|---|
| unsigned char | area2[128] | Synchronous DRAM area | main |
| unsigned char | buf[128] | Internal RAM area | main |

## 5.4 Macro Definition

**Table 17 Macro Definition**

| Defined Name | Setting | Description | Used in Function |
|---|---|---|---|
| SDRAM_MD_SET | H'400460 | Through byte access to the address at right, settings are made in the synchronous DRAM's mode register. | BscInit |

## 5.5 Description of Functions

### 5.5.1 Function init

1. Functional overview

Initialization routine, which releases the required modules from module stop mode, configures the clocks, and calls the main function.

2. Arguments

None

3. Return value

None

4. Description of Internal Registers

Usage of internal registers in this function of the sample task is described below. Note that the settings shown below are not the initial values but the values used in this sample task.

- Mode control register (MDCR) Number of bits: 16 Address: H'FFFDC0

| Bit | Bit Name | Setting | R/W | Description |
|---|---|---|---|---|
| 15 | MDS7 | Undefined* | R | Indicates the value set by a mode pin (MD3). When MDCR is read, the input level on the MD3 pin is latched. This latching is released by a reset. |
| 11 | MDS3 | Undefined* | R | Mode Select 3 to 0 |
| 10 | MDS2 | Undefined* | R | These bits indicate the operating mode selected by the mode pins (MD2 to MD0) (see table 18). When MDCR is read, the signal levels input on pins MD2 to MD0 are latched into these bits. These latches are released by a reset. |
| 9 | MDS1 | Undefined* | R | |
| 8 | MDS0 | Undefined* | R | |

Note: * Determined by the settings on pins MD3 to MD0.

**Table 18 Settings of Bits MDS3 to MDS0**

| MCU Operating Mode | Pins | | | MDCR | | | |
|---|---|---|---|---|---|---|---|
| | MD2 | MD1 | MD0 | MDS3 | MDS2 | MDS1 | MDS0 |
| 2 | 0 | 1 | 0 | 1 | 1 | 0 | 0 |
| 4 | 1 | 0 | 0 | 0 | 0 | 1 | 0 |
| 5 | 1 | 0 | 1 | 0 | 0 | 0 | 1 |
| 6 | 1 | 1 | 0 | 0 | 1 | 0 | 1 |
| 7 | 1 | 1 | 1 | 0 | 1 | 0 | 0 |

- System clock control register (SCKCR) Number of bits: 16 Address: H'FFFDC4

| Bit | Bit Name | Setting | R/W | Description |
|---|---|---|---|---|
| 10 | ICK2 | 0 | R/W | System Clock (Iϕ) Select |
| 9 | ICK1 | 0 | R/W | These bits select the frequency of the system clock, which is provided to the CPU, DMAC, and DTC. |
| 8 | ICK0 | 0 | R/W | 000: Input clock × 4 |
| 6 | PCK2 | 0 | R/W | Peripheral Module Clock (Pϕ) Select |
| 5 | PCK1 | 0 | R/W | These bits select the frequency of the peripheral module clock. |
| 4 | PCK0 | 1 | R/W | 001: Input clock × 2 |
| 2 | BCK2 | 0 | R/W | External Bus Clock (Bϕ) Select |
| 1 | BCK1 | 0 | R/W | These bits select the frequency of the external bus clock. |
| 0 | BCK0 | 0 | R/W | 000: Input clock × 4 |

- MSTPCRA, B and C control module stop mode. Setting a bit to 1 makes the corresponding module enter the module stop state, while clearing the bit to 0 releases the module from module stop state.
- Module stop control register A (MSTPCRA) Number of bits: 16 Address: H'FFFDC8

| Bit | Bit Name | Setting | R/W | Description |
|---|---|---|---|---|
| 15 | ACSE | 0 | R/W | All-Module-Clock-Stop Mode Enable<br>Enables/disables all-module-clock-stop mode for reducing current consumption by stopping operation of the bus controller and I/O ports when the CPU executes the SLEEP instruction after the module stop state has been set for all of the on-chip peripheral modules controlled by MSTPCR.<br>0: All-module-clock-stop mode disabled.<br>1: All-module-clock-stop mode enabled. |
| 13 | MSTPA13 | 1 | R/W | DMA controller (DMAC) |
| 12 | MSTPA12 | 1 | R/W | Data transfer controller (DTC) |
| 9 | MSTPA9 | 1 | R/W | 8-bit timer (TMR_3 and TMR_2) |
| 8 | MSTPA8 | 1 | R/W | 8-bit timer (TMR_1 and TMR_0) |
| 5 | MSTPA5 | 1 | R/W | D/A converter (channels 1 and 0) |
| 3 | MSTPA3 | 1 | R/W | A/D converter (unit 0) |
| 0 | MSTPA0 | 1 | R/W | 16-bit timer pulse unit (TPU channels 5 to 0) |

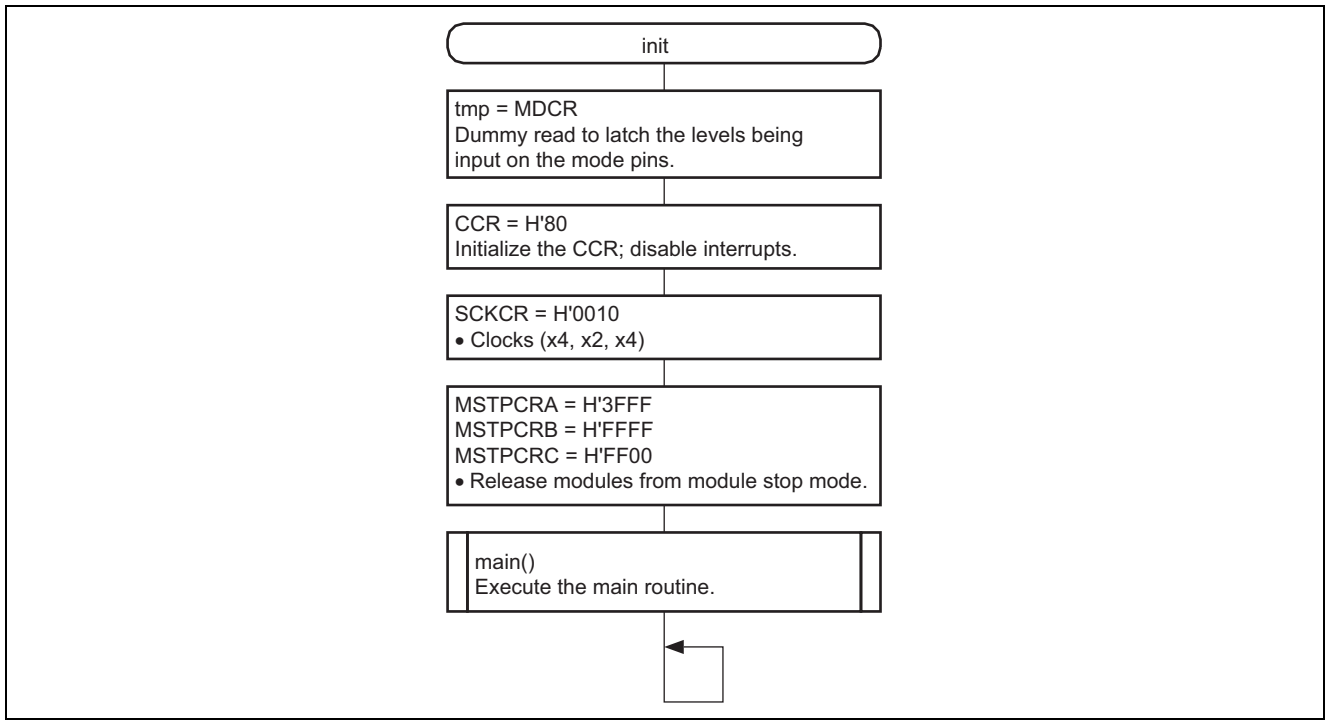
- Module stop control register B (MSTPCRB) Number of bits: 16 Address: H'FFFDCA

| Bit | Bit Name | Setting | R/W | Description |
|---|---|---|---|---|
| 15 | MSTPB15 | 1 | R/W | Programmable pulse generator (PPG) |
| 12 | MSTPB12 | 1 | R/W | Serial communications interface_4 (SCI_4) |
| 10 | MSTPB10 | 1 | R/W | Serial communications interface_2 (SCI_2) |
| 9 | MSTPB9 | 1 | R/W | Serial communications interface_1 (SCI_1) |
| 8 | MSTPB8 | 1 | R/W | Serial communications interface_0 (SCI_0) |
| 7 | MSTPB7 | 1 | R/W | $I^2C$ bus Interface_1 (IIC_1) |
| 6 | MSTPB6 | 1 | R/W | $I^2C$ bus Interface_0 (IIC_0) |

- Module stop control register C (MSTPCRC) Number of bits: 16 Address: H'FFFDCC

| Bit | Bit Name | Setting | R/W | Description |
|---|---|---|---|---|
| 15 | MSTPC15 | 1 | R/W | Serial communications interface_5 (SCI_5), (IrDA) |
| 14 | MSTPC14 | 1 | R/W | Serial communications interface_6 (SCI_6) |
| 13 | MSTPC13 | 1 | R/W | 8-bit timers (TMR_4, TMR_5) |
| 12 | MSTPC12 | 1 | R/W | 8-bit timers (TMR_6, TMR_7) |
| 11 | MSTPC11 | 1 | R/W | Universal serial bus interface (USB) |
| 10 | MSTPC10 | 1 | R/W | Cyclic redundancy check module |
| 4 | MSTPC4 | 0 | R/W | On-chip RAM_4 (H'FF2000 to H'FF3FFF) |
| 3 | MSTPC3 | 0 | R/W | On-chip RAM_3 (H'FF4000 to H'FF5FFF) |
| 2 | MSTPC2 | 0 | R/W | On-chip RAM_2 (H'FF6000 to H'FF7FFF) |
| 1 | MSTPC1 | 0 | R/W | On-chip RAM_1 (H'FF8000 to H'FF9FFF) |
| 0 | MSTPC0 | 0 | R/W | On-chip RAM_0 (H'FFA000 to H'FFBFFF) |

5. Flowchart


init
tmp = MDCR
Dummy read to latch the levels being input on the mode pins.
CCR = H'80
Initialize the CCR; disable interrupts.
SCKCR = H'0010
• Clocks (x4, x2, x4)
MSTPCRA = H'3FFF
MSTPCRB = H'FFFF
MSTPCRC = H'FF00
• Release modules from module stop mode.
main()
Execute the main routine.

### 5.5.2 Function main

1. Functional overview

Calls function BscInit and handles processing to confirm synchronous DRAM (SDRAM) operations.

2. Arguments

None

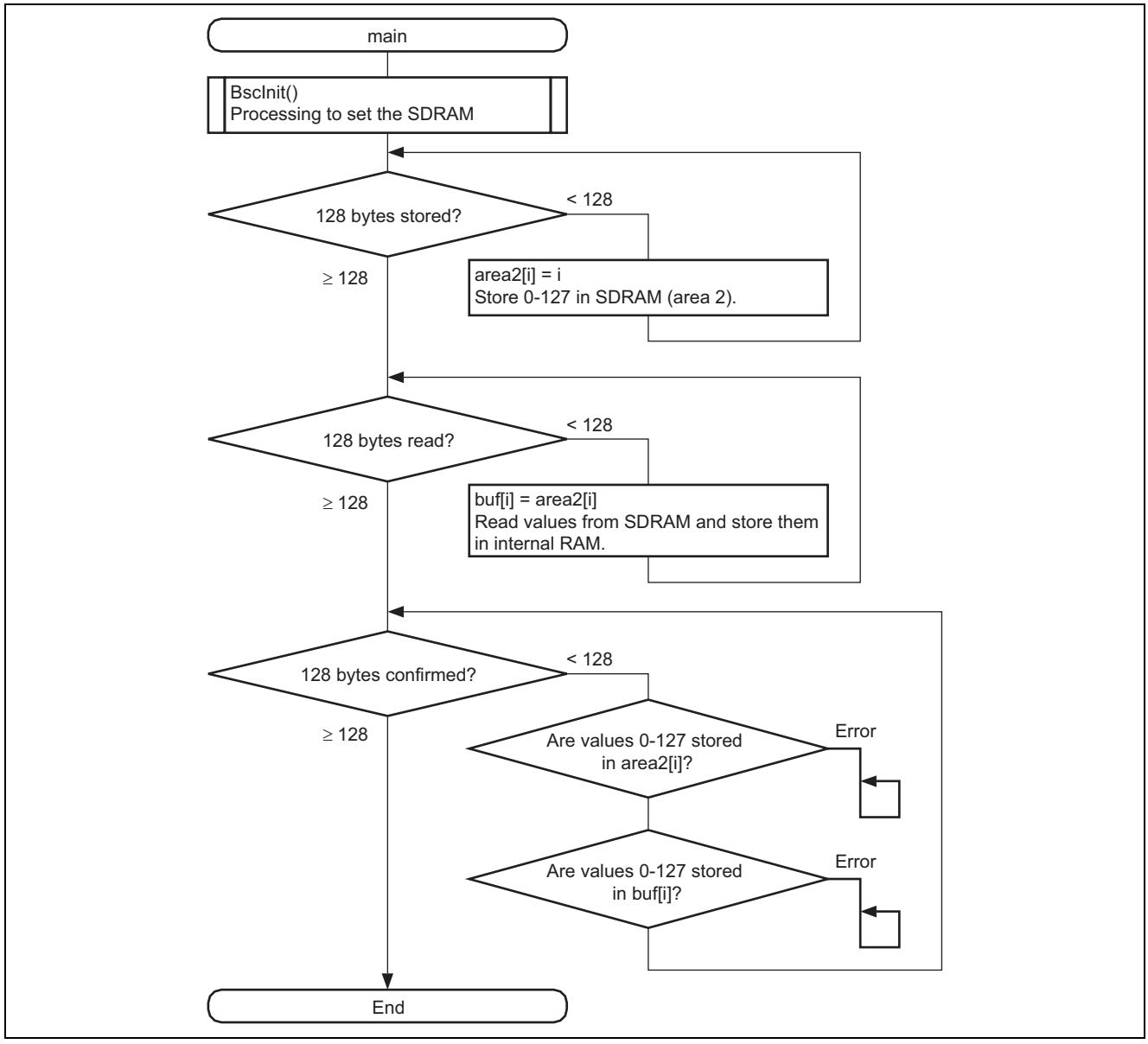
3. Return value

None

4. Description of Internal Register

None

5. Flowchart



### 5.5.3 Function BscInit

1. Functional overview

Initialization settings for the synchronous DRAM (SDRAM)

2. Arguments

None

3. Return value

None

4. Description of Internal Register

Usage of internal registers in this sample task is described below. Note that the settings shown below are not the initial values but the values used in this sample task.

- Port D data direction register (PDDDR) Number of bits: 8 Address: H'FFFB8C

Function: Setting pins PD7 to PD0 as outputs (for address output)
Setting: H'FF

- Port E data direction register (PEDDR) Number of bits: 8 Address: H'FFFB8D

Function: Setting pins PE7 to PE0 as outputs (for address output)
Setting: H'FF

- Port function control register 0 (PFCR0) Number of bits: 8 Address: H'FFFBC0

| Bit | Bit Name | Setting | R/W | Description |
|---|---|---|---|---|
| 2 | CS2E | 1 | R/W | CS2 Enable<br>This bit enables/disables the $\overline{CS2}$ output.<br>0: Pin functions as I/O port.<br>1: Pin functions as $\overline{CS2}$ output pin. |

- Port function control register 2 (PFCR2) Number of bits: 8 Address: H'FFFBC2

| Bit | Bit Name | Setting | R/W | Description |
|---|---|---|---|---|
| 6 | CS2S | 1 | R/W | $\overline{CS2}$ Output Select<br>0: When $\overline{CS2}$ output is enabled (CS2E = 1), PB2 is selected as the $\overline{CS2}$-A output pin.<br>1: When $\overline{CS2}$ output is enabled (CS2E = 1), PB1 is selected as the $\overline{CS2}$-B output pin. |

- Port function control register 4 (PFCR4) Number of bits: 8 Address: H'FFFBC4

| Bit | Bit Name | Setting | R/W | Description |
|---|---|---|---|---|
| 7 | A23E | 1 | R/W | Address A23 Enable<br>0: Disables the A23 output.<br>1: Enables the A23 output. |
| 6 | A22E | 1 | R/W | Address A22 Enable<br>0: Disables the A22 output.<br>1: Enables the A22 output. |
| 5 | A21E | 1 | R/W | Address A21 Enable<br>0: Disables the A21 output.<br>1: Enables the A21 output. |
| 4 | A20E | 1 | R/W | Address A20 Enable<br>0: Disables the A20 output.<br>1: Enables the A20 output. |
| 3 | A19E | 1 | R/W | Address A19 Enable<br>0: Disables the A19 output.<br>1: Enables the A19 output. |
| 2 | A18E | 1 | R/W | Address A18 Enable<br>0: Disables the A18 output.<br>1: Enables the A18 output. |
| 1 | A17E | 1 | R/W | Address A17 Enable<br>0: Disables the A17 output.<br>1: Enables the A17 output. |
| 0 | A16E | 1 | R/W | Address A16 Enable<br>0: Disables the A16 output.<br>1: Enables the A16 output. |

- Bus width control register (ABWCR) Number of bits: 16 Address: H'FFFD84

Function: Setting 16-bit access for areas 0 to 7
Setting: H'00FF

- Wait control register A (WTCRA) Number of bits: 16 Address: H'FFFD88

Function: Inserting programmed wait periods for areas 4 to 7
Setting: H'0000

- Wait control register B (WTCRB) Number of bits: 16 Address: H'FFFD8A

Function: Inserting programmed wait periods for areas 1, 2, and 3. When DRAM is to be connected in area 2, set the CAS latency to 3.
Setting: H'0200

- DRAM control register (DRAMCR) Number of bits: 16 Address: H'FFFDA0

| Bit | Bit Name | Setting | R/W | Description |
|---|---|---|---|---|
| 15 | DRAME | 1 | R/W | Area 2 DRAM Interface Select<br>0: Basic bus interface or byte-control SRAM interface<br>1: DRAM/SDRAM interface |
| 14 | DTYPE | 1 | R/W | DRAM Select<br>Selects the type of DRAM to be used in area 2.<br>0: DRAM is used in area 2.<br>1: SDRAM is used in area 2. |
| 11 | OEE | 1 | R/W | $\overline{OE}$ Output Enable<br>0: CKE signal output disabled when SDRAM is connected.<br>1: CKE signal enabled when SDRAM is connected. |
| 7 | BE | 0 | R/W | Burst Access Enable<br>0: Access to the DRAM/SDRAM is full access.<br>1: Access to the DRAM/SDRAM is in high-speed paged mode. |
| 6 | RCDM | 0 | R/W | RAS Down Mode<br>Selects the $\overline{RAS}$ signal state while a DRAM access is halted when a basic bus interface area or an on-chip I/O register is accessed: keep the $\overline{RAS}$ signal low ($\overline{RAS}$ down mode) and high ($\overline{RAS}$ up mode).<br>This bit is effective when BE = 1. Clearing this bit to 0 with RCDM = 1 in $\overline{RAS}$ down mode cancels the $\overline{RAS}$ down mode and the $\overline{RAS}$ signal goes high.<br>When the $\overline{RAS}$ down mode is selected for the SDRAM interface, the READ/WRIT command is issued without issuance of the ACTV command when the same row address is accessed consecutively.<br>0: RAS up mode when the DRAM/SDRAM is accessed<br>1: RAS down mode when the DRAM/SDRAM is accessed |
| 1 | MXC1 | 0 | R/W | Multiplexed Address Bit Select |
| 0 | MXC0 | 0 | R/W | Select the number of bits by which a row address multiplexed with a column address is shifted to the lower-order side. At the same time, these bits select the row-address bits to be compared during burst access to the DRAM/SDRAM interface.<br>00: Shifted by 8 bits<br>A23 to A8 are compared for an 8-bit-access space<br>A23 to A9 are compared for a 16-bit-access space |

- DRAM access control register (DRACCR) Number of bits: 16 Address: H'FFFDA2

| Bit | Bit Name | Setting | R/W | Description |
|---|---|---|---|---|
| 13 | TPC1 | 0 | R/W | Precharge Cycle Control |
| 12 | TPC0 | 0 | R/W | Select the number of cycles for RAS-precharging in normal access and in refresh operations.<br>00: One cycle for a cycle of RAS precharging |
| 9 | RCD1 | 0 | R/W | $\overline{RAS}$-$\overline{CAS}$ Wait Control |
| 8 | RCD0 | 0 | R/W | Select the number of cycles whether to be inserted or not as a period of waiting between $\overline{RAS}$ and $\overline{CAS}$ cycles.<br>00: No waiting is inserted between cycles of $\overline{RAS}$ and $\overline{CAS}$ assertion. |

- Synchronous DRAM control register (SDCR) Number of bits: 16 Address: H'FFFDA4

| Bit | Bit Name | Setting | R/W | Description |
|---|---|---|---|---|
| 15 | MRSE | 0/1 | R/W | Mode Register Set Enable<br>Enables the setting in the SDRAM mode register.<br>0: Disables setting of the SDRAM mode register<br>1: Enables setting of the SDRAM mode register |
| 7 | CKSPE | 0 | R/W | Clock Suspend Enable<br>Enables the clock-suspension mode, in which the output of read data is extended. Setting this bit to 1 extends the period of output of data read from SDRAM by one cycle.<br>0: Disables the clock-suspension mode.<br>1 Enables the clock-suspension mode. |
| 0 | TRWL | 0 | R/W | Write-Precharge Delay Control<br>Specifies the time until the precharge command is issued after a write command has been issued to the SDRAM. Setting this bit to 1 inserts a wait of one cycle after a write command has been issued.<br>0: No wait inserted.<br>1: One wait inserted after the write command is issued. |

- Refresh control register (REFCR) Number of bits: 16 Address: H'FFFDA6

| Bit | Bit Name | Setting | R/W | Description |
|---|---|---|---|---|
| 14 | CMIE | 0 | R/W | Compare Match Interrupt Enable<br>Enables or disables an interrupt request (CMI) when the CMF flag is set to 1.<br>This bit is effective when refresh control is not performed (RFSHE = 0). When refresh control is performed (RFSHE = 1), this bit is always cleared to 0. This bit cannot be modified.<br>0: Disables an interrupt request by the CMF flag.<br>1: Enables an interrupt request by the CMF flag. |
| 10 | RTCK2 | 0 | R/W | Refresh Counter Clock Select<br>Select the clock to drive counting by the refresh counter from among seven internal clocks generated by dividing the on-chip peripheral module clock (Pϕ). Once the clock is selected, the refresh counter starts to count up.<br>001: Counts cycles of Pϕ/2 |
| 9 | RTCK1 | 0 | R/W | |
| 8 | RTCK0 | 1 | R/W | |
| 7 | RFSHE | 1 | R/W | Refresh Control<br>Enables or disables refresh control. When refresh control is disabled, the refresh timer can be used as an interval timer.<br>In single-chip activation mode, the setting of this bit should be made after setting the EXPE bit in SYSCR to 1.<br>0: Refresh control not applied<br>1: Refresh control applied |
| 6 | RLW2 | 0 | R/W | Refresh Cycle Wait Control<br>Select a wait for the number of cycles to be inserted during a CAS before an RAS refresh cycle for the DRAM interface and an auto-refresh cycle for the SDRAM interface.<br>000: No waiting inserted to CBR refresh/auto-refresh. |
| 5 | RLW1 | 0 | R/W | |
| 4 | RLW0 | 0 | R/W | |
| 3 | SLFRF | 0 | R/W | Self-Refresh Enable<br>Selects the self-refresh mode for the DRAM/SDRAM interface when a transition to the software standby mode is made with this bit set to 1. This bit is effective when refresh cycles are applied by setting the RFSHE bit to 1.<br>To apply self-refreshing when the SDRAM interface is selected, enable the CKE output by setting the OEE bit in DRAMCR.<br>0: Disables self-refreshing in software standby mode.<br>1: Enables self-refreshing in software standby mode. |
| 2 | TPCS2 | 0 | R/W | Precharge Cycle Control during Self-Refresh<br>Selects the number of cycles for a precharge cycle immediately after a self-refresh cycle. The actual number for the precharge cycle is the sum of the numbers indicated by these bits and by bits TPC1 and TPC0.<br>000: No waiting is inserted immediately after the self-refresh value. |
| 1 | TPCS1 | 0 | R/W | |
| 0 | TPCS0 | 0 | R/W | |

- Refresh timer counter (RTCNT) Number of bits: 8 Address: H'FFFDA8

Function: RTCNT counts cycles of the internal clock selected by bits RTCS2 to RTCK0 in REFCR. When the RTCNT value matches the RTCOR value (compare match), the CMF flag in REFCR is set to 1 and RTCNT is initialized to H'00. At this time, when the RFSHE bit in REFCR is set to 1, a refresh cycle is generated. When the RFSHE bit is cleared to 0 and the CMIE bit in REFCR is set to 1, a compare match interrupt (CMI) is generated.

Setting: H'00

- Refresh timer constant register (RTCOR) Number of bits: 8 Address: H'FFFDA9

Function: RTCOR specifies the intervals at which compare-matches of RTCOR and RTCNT will be generated. The value of RTCOR is constantly compared with that of RTCNT. When they match, the CMF flag in REFCR is set to 1 and RTCNT is initialized to H'00.

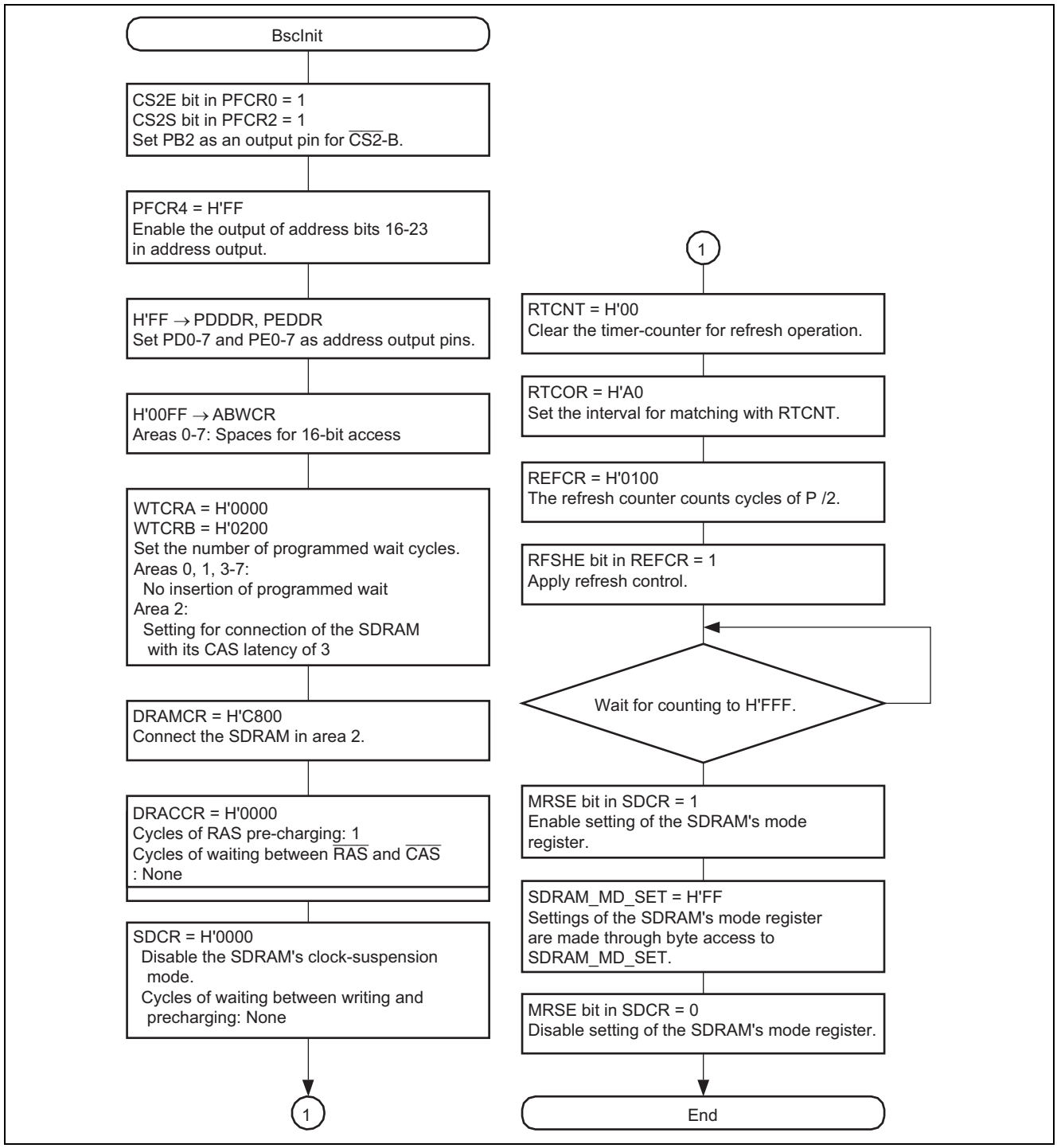
Setting: H'A0

- System control register (SYSCR) Number of bits: 16 Address: H'FFFDC2

| Bit | Bit Name | Setting | R/W | Description |
|---|---|---|---|---|
| 9 | EXPE | Undefined* | R/W | External Bus Mode Enable<br>Selects external bus mode. In external expansion mode, this bit is fixed to 1 and cannot be changed. In single-chip mode, the initial value of this bit is 0, and it can be read from or written to.<br>Do not attempt external bus access after reading this bit as 1 and then writing 0 to it.<br>This is because the resulting external bus cycle may be carried out in parallel with an internal bus cycle, depending on the setting of the write data buffer function.<br>Note that in this sample task, mode 6 (external expansion mode) is not used to set the EXPE bit.<br>0: External bus disabled.<br>1: External bus enabled. |

Note: * The initial value depends on the LSI initiation mode.

5. Flowchart


BscInit
CS2E bit in PFCR0 = 1
CS2S bit in PFCR2 = 1
Set PB2 as an output pin for CS2-B.
PFCR4 = H'FF
Enable the output of address bits 16-23 in address output.
H'FF → PDDDR, PEDDR
Set PD0-7 and PE0-7 as address output pins.
H'00FF → ABWCR
Areas 0-7: Spaces for 16-bit access
WTCRA = H'0000
WTCRB = H'0200
Set the number of programmed wait cycles.
Areas 0, 1, 3-7:
No insertion of programmed wait
Area 2:
Setting for connection of the SDRAM with its CAS latency of 3
DRAMCR = H'C800
Connect the SDRAM in area 2.
DRACCR = H'0000
Cycles of RAS pre-charging: 1
Cycles of waiting between RAS and CAS
: None
SDCR = H'0000
Disable the SDRAM's clock-suspension mode.
Cycles of waiting between writing and precharging: None
1
1
RTCNT = H'00
Clear the timer-counter for refresh operation.
RTCOR = H'A0
Set the interval for matching with RTCNT.
REFCR = H'0100
The refresh counter counts cycles of P /2.
RFSHE bit in REFCR = 1
Apply refresh control.
Wait for counting to H'FFF.
MRSE bit in SDCR = 1
Enable setting of the SDRAM's mode register.
SDRAM_MD_SET = H'FF
Settings of the SDRAM's mode register are made through byte access to SDRAM_MD_SET.
MRSE bit in SDCR = 0
Disable setting of the SDRAM's mode register.
End

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## Revision Record

| | | Description | |
|---|---|---|---|
| **Rev.** | **Date** | **Page** | **Summary** |
| 1.00 | Jun.18.07 | — | First edition issued |
| 2.00 | Feb.15.08 | 1, 3, 6 | Page 1: Target device changed<br>Page 1: “Preface” added<br>Page 3: Table 2 modified<br>Page 6: Table 4 modified |
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