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M16C/64 Group

Stop Mode Setup

1. Abstract

In stop mode, all clock oscillations stop. This causes the CPU clock and peripheral function clock to stop, so that the CPU and peripheral functions driven by these clocks stop operating. In this mode, the least amount of power is consumed.

The sample program uses an $\overline{INT0}$ interrupt for the cause of return from stop mode.

Table 1 lists the resets and interrupts usable for the cause of return from stop mode and the condition under which they can be used.

Table 1. Resets and Interrupts Usable for the Cause of Return from Stop Mode and Usage Conditions

Reset and interrupt	Condition
$\overline{NMI}$ interrupt	Usable
Key input interrupt	Usable
$\overline{INT}$ interrupt	Usable
Timer A interrupt Timer B interrupt	Usable when the timer is counting external pulses in event count mode
Serial interface interrupt	Usable when external clock is selected
Voltage-down detection interrupt	Usable
Hardware reset 1	Usable
Hardware reset 2	Usable when digital filter is disabled (VW0C = 1)

2. Introduction

The application example described in this document applies to the following MCU:

・MCU: M16C/64 group

This application note can be used with other M16C Family MCUs which have the same special function registers (SFRs) as the above group. Check the manual for any modifications to functions. Careful evaluation is recommended before using the program described in this application note.

3. Setup Procedure

The following explains how to set the registers to enter stop mode and how the device will operate in stop mode. The setup procedure is shown in Figures 1.1 and 1.2.

(1) Set the I flag to 0.
(2) Set up the ILVL2–ILVL0 bits (interrupt priority level).
・When using a hardware reset, $\overline{\text{NMI}}$ interrupt or voltage-down detection interrupt to return from stop mode
Set all of the ILVL2–ILVL0 bits for peripheral function interrupts to 000b (interrupt disabled).
・When using a peripheral function interrupt to return from stop mode
Set the interrupt priority level in the ILVL2–ILVL0 bits for the peripheral function interrupt used for return from stop mode.
Set the ILVL2–ILVL0 bits for the peripheral function interrupts not used for return from stop mode to 000b (interrupt disabled).
(3) Set the PRC0 bit of the PRCR register to 1 (write enabled).
(4) If the CM11 bit of the CM1 register is 1 (PLL clock selected for the CPU clock), set the CM11 bit to 0 (main clock selected for the CPU clock) and then set the PLC07 bit of the PLC register to 0 (PLL turned off).
(5) If oscillation stop detection is used, set the CM20 bit of the CM2 register to 0 (oscillation turned off, reoscillation detection disabled).
(6) Set the I flag to 1.
(7) Set the CM10 bit of the CM1 register to 1 (all clocks turned off) to enter stop mode. [Note 1, Note 2]

Note 1: When stop mode is entered, the CM06 bit of the CM0 register is fixed to 1 (divide-by-8 mode) and the CM15 bit of the CM1 register is fixed to 1 (main clock oscillator circuit drive capability HIGH).

Note 2: For the CPU clock after return from stop mode, the following applies:
・If the selected CPU clock prior to mode transition was a sub-clock,
then the device returns with the sub-clock.
・If the selected CPU clock prior to mode transition was the main clock,
then the device returns with the main clock divided by 8.
・If the selected CPU clock prior to mode transition was the 125 kHz on-chip oscillator clock,
then the device returns with the 125 kHz on-chip oscillator clock divided by 8.

Processing before transition to stop mode

(1) Set the interrupt enable flag (I flag) to 0.

(2) Set the interrupts used for return from stop mode and those not used.

Interrupt control register

|	
TBiIC(i=0~5)	[Timer Bi]
BCNIC	[UART2 bus collision detection]
DMiIC(i=0~3)	[DMAi]
KUPIC	[Key input interrupt]
ADIC	[A/D]
SiTIC(i=0~2,5~7)	[UARTi transmit complete]
SiRIC(i=0~2,5~7)	[UARTi receive complete]
TAiIC(i=0~4)	[Timer Ai]
UiBCNIC(i=0,1,5~7)	[UART1 bus collision detection]

b7 ... b0
ILVL2~ILVL0
Interrupt priority level select bits
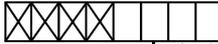
INTiIC(i=0~7)
[INTi external interrupt]
SiIC(i=3,4)[SI/Oi]

b7 ... b0
ILVL2~ILVL0
Interrupt priority level select bits

(3) Lift protection.
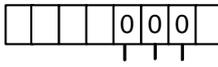
b7 ... b0
0 | 0 0 | | | 1
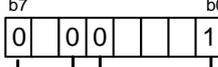
Protect register
(PRCR)

PRC0   CM0, CM1, CM2, PLC0, PCLKR register write enable
1: Enables write
Reserved bits
Set these bits to 0.

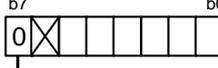**If the selected CPU clock is the PLL clock**

(4) Select the main clock for the CPU clock.

b7 ... b0
| | | 0 0 0 | |

System clock control register 1
(CM1)

CM11 System clock select bit 1
0: Main clock
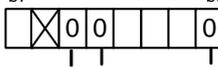Reserved bits
Set these bits to 0.

b7 ... b0
0 ⊠ | | | | | |

PLL control register 0
(PLC0)

PLC07 Operation enable bit
0: Turns PLL off

If oscillation stop detection is used

(5) Disable the oscillation stop and reoscillation detection.

b7 ... b0
⊠ 0 0 | | | 0

Oscillation stop detection register
(CM2)

CM20 Oscillation stop and reoscillation detection enable bit
0: Disables oscillation stop and reoscillation detection
Reserved bits
Set these bits to 0.

(6) Set the interrupt enable flag (I flag) to 1.

Go to the next page

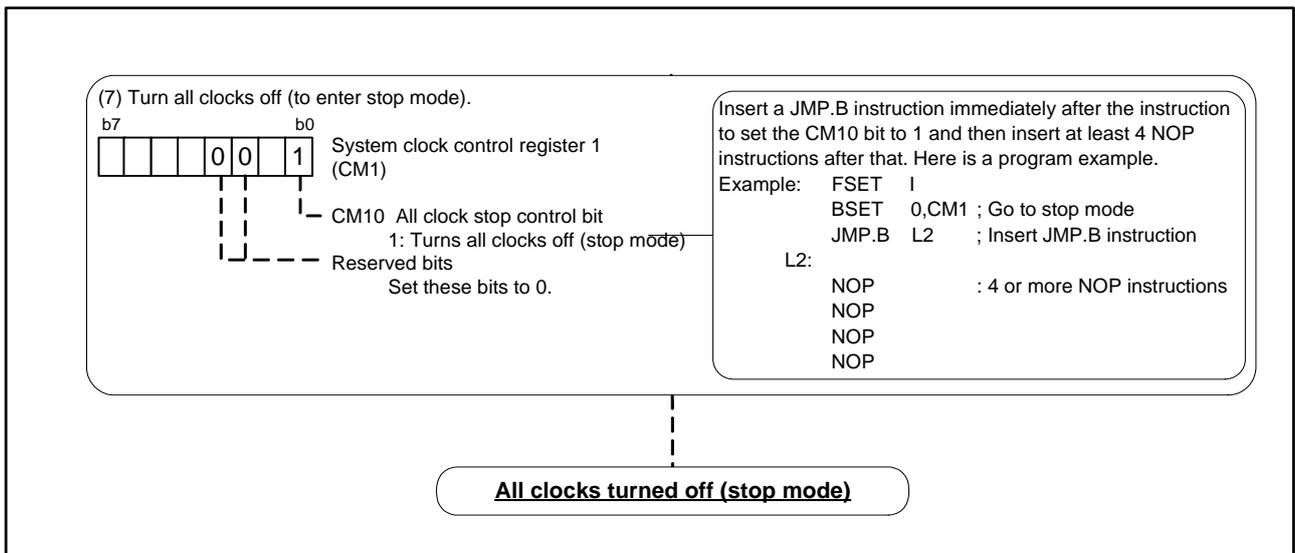Figure 1.1   Example for Setting Up Registers to Enter Stop Mode

Figure 1.2   Example of Register Setup for Entering Stop Mode

4.   Sample Programming Code

A sample program can be downloaded from the Renesas Technology website.
To download, click "Application Notes" in the left-hand side menu of the M16C Family page.

5.   Reference Documents

Hardware manual

M16C/64 Group Hardware Manual
(Get the latest version from the Renesas Technology website.)

Technical updates and technical news

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