Smart Configurator for RZ

How to Check for Contention between Pin Assignments Made by the FSP Smart Configurator and the Smart Configurator for RZ

Introduction

This document describes a function that can be used to check for contention between pin assignments made by the FSP (Flexible Software Package) Smart Configurator and the Smart Configurator for RZ. It will be helpful in recognizing and avoiding contention between pin assignments when developers using the FSP and Linux software package with RZ Family devices are deciding on pin configurations.

Target Devices

RZ Family devices supported by both the FSP and Linux software package, are listed below.

・RZ/T2H, RZ/N2H, RZ/G2L, RZ/G2LC, RZ/G2UL, RZ/G3S, RZ/V2L, RZ/V2H, RZV2N (Apr. 2025)

Detailed supported devices information by FSP and Linux Software Package, can be found on the following page.

https://www.renesas.com/design-support/software

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1. Supported Versions of e² studio, FSP, and Smart Configurator for RZ

The features described in this document are available in the following environment.

- e² studio: 2024-01 or later
- FSP (Flexible Software Package)
  - RZ/G: v2.0.0 or later
  - RZ/N: v2.1.0 or later
  - RZ/T: v2.2.0 or later
  - RZ/V: v2.0.0 or later
- Smart Configurator for RZ: v1.16.0 or later

This document describes functions used in the following environment.

- RZ Family device: RZ/T2H
- e² studio: 2024-10
- FSP
  - RZ/T: v2.2.0
- Smart Configurator for RZ: v1.18.0

2. Method of Checking for Contention between Pin Assignments

Checking for contention between pin assignments is handled by building an FSP project to generate a Smart bundle file (*.sbd) and then importing the file to the Smart Configurator for RZ.

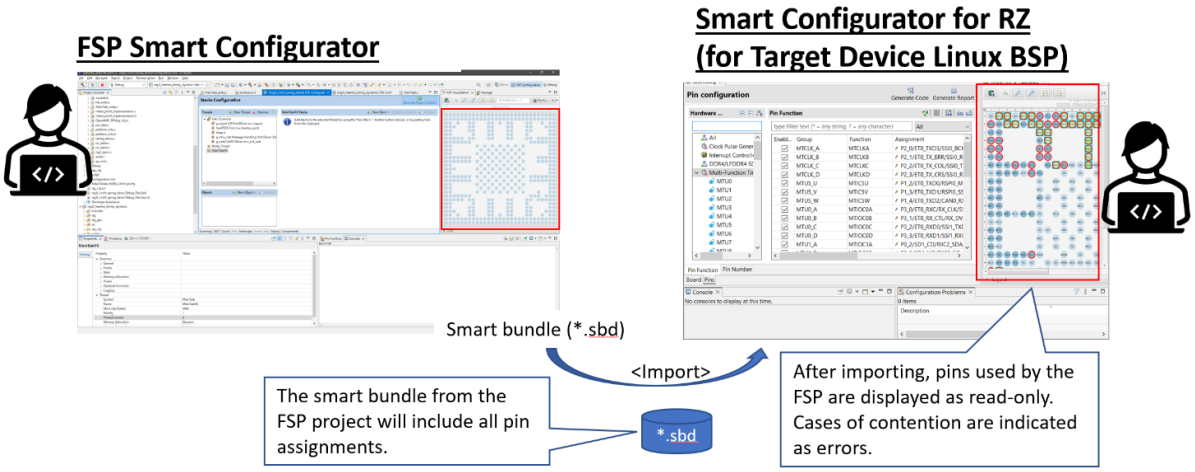

Figure 1. Overall Flow of Checking for Contention between Pin Assignments

Note. Checking for contention between pin assignments is available only between FSP Smart Configurator project and RZ Smart Configurator project which their device part numbers belong to same device group and have same package.

e.g. Device part numbers of the same group and same package: Available

- FSP Smart Configurator (RZ/T2H, 729 pins):
  R9A09G077M04GBG, R9A09G077M08GBG, R9A09G077M24GBG, …
- RZ Smart Configurator (RZ/T2H, 729 pins): R9A09G077M

Device part numbers for different groups: Not available

- FSP Smart Configurator (RZ/T2H, 729 pins):
  R9A09G077M04GBG, R9A09G077M08GBG, R9A09G077M24GBG, …
- RZ Smart Configurator (RZ/N2H, 576 pins): R9A09G087M

2.1 Generating a Smart bundle file

After having configured all required pins in the FSP Smart Configurator for e² studio, build an FSP project for use with the target RZ Family device and confirm that a smart bundle file has been generated.
The smart bundle file will be in the <FSP Project folder>\Debug folder.

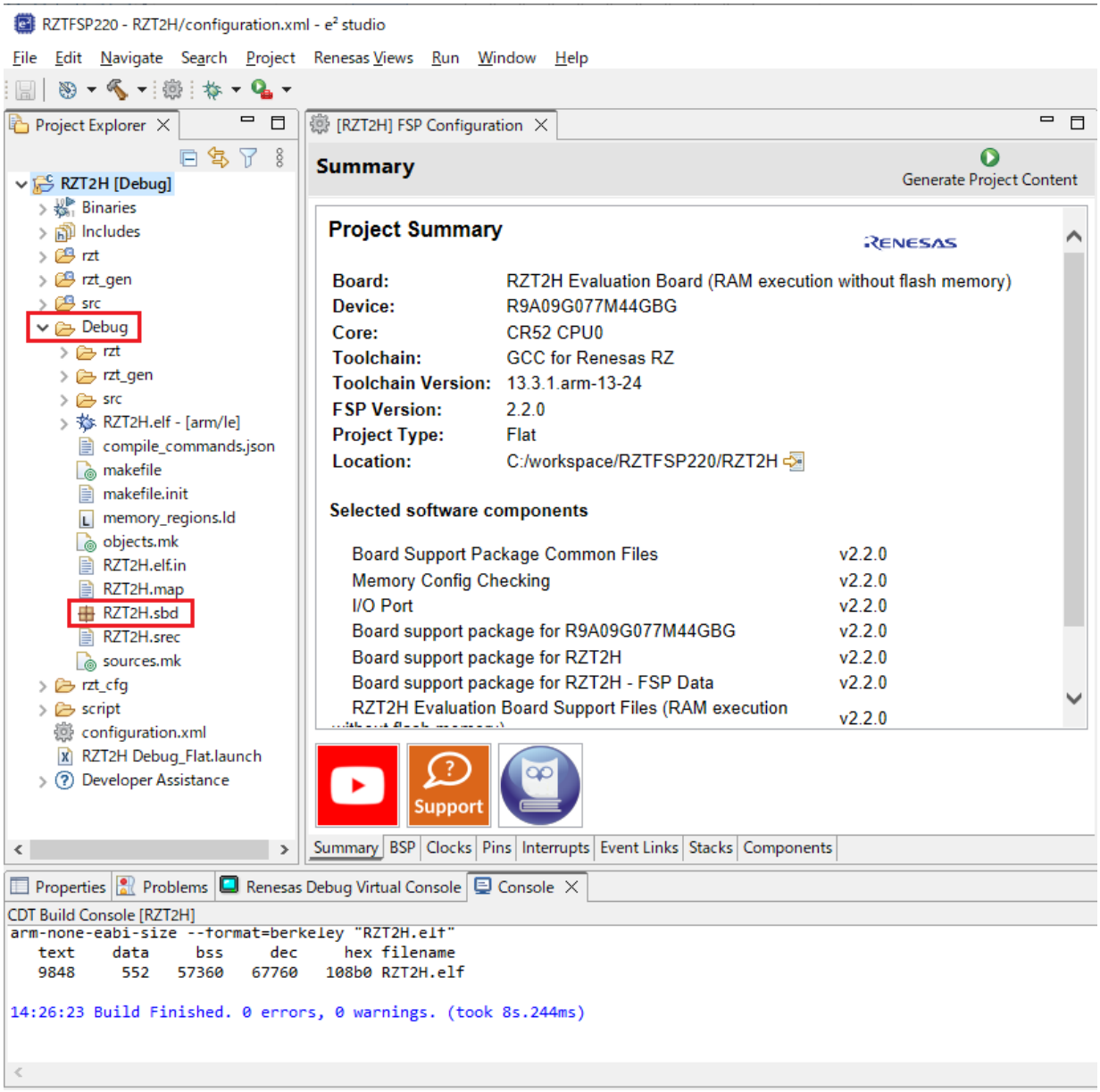

Figure 2. Generated Smart bundle file

2.2 Importing a Smart bundle file to the Smart Configurator for RZ

Import Smart bundle file to the Smart Configurator for RZ by following steps in below.

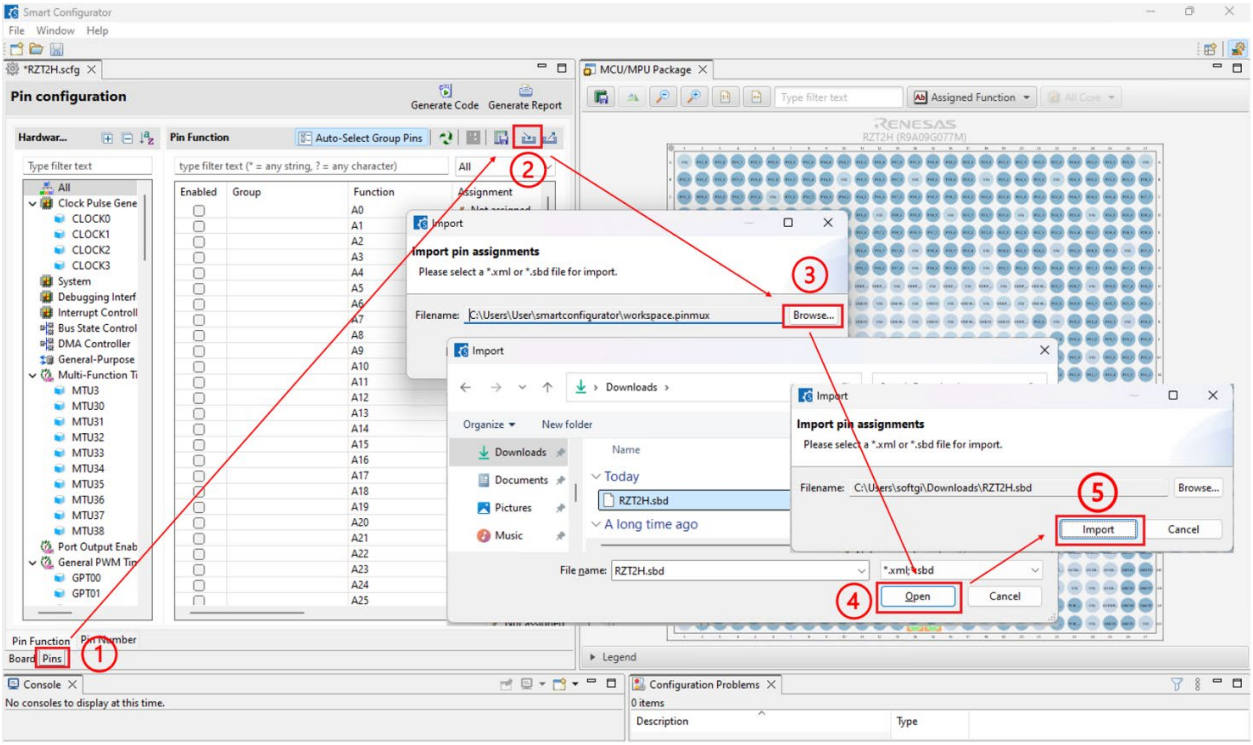

Figure 3. Importing a Smart bundle file to the Smart Configurator for RZ

① Create or open a project of the Smart Configurator for RZ for RZ Family devices. Select the [Pins] panel.
② Click on the (import) button.
③ Click the ‘Browse…’ button.
④ Select and open the smart bundle file from the FSP project in e^2 studio
⑤ Click on the [Import] button.

When smart bundle file is imported to the Smart Configurator for RZ, the ‘Device mismatch’ warning message will be displayed. However, if the device part numbers set in the smart bundle file and in the project of the Smart Configurator for RZ are from the same device group and package, checking for contention between pin assignments works well.

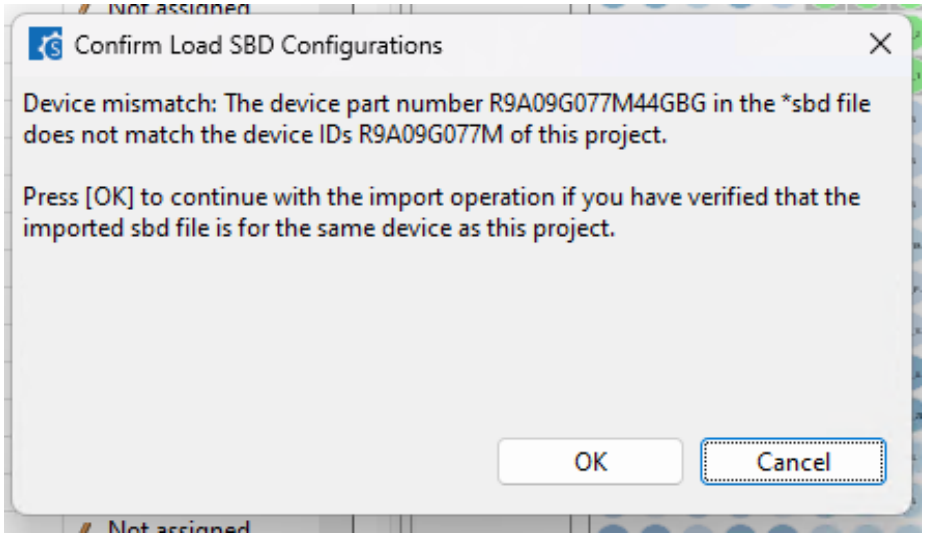

Figure 4. Warning Message: Device Mismatch’

In the case of Figure 4, device part numbers belong to the same group and package as shown below. Therefore, ignore the warning message and press the "OK" button.

- FSP Smart Configurator:
  R9A09G077M44GBG (RZ/T2H, 729 pins)

- RZ Smart Configurator:
  R9A09G077M(RZ/T2H, 729 pins)

2.3 Checking for Contention between Pin Assignments

After a smart bundle file has been imported to the Smart Configurator for RZ, the [Console] view lists the new pin assignments from the smart bundle file as shown at Figure 5.

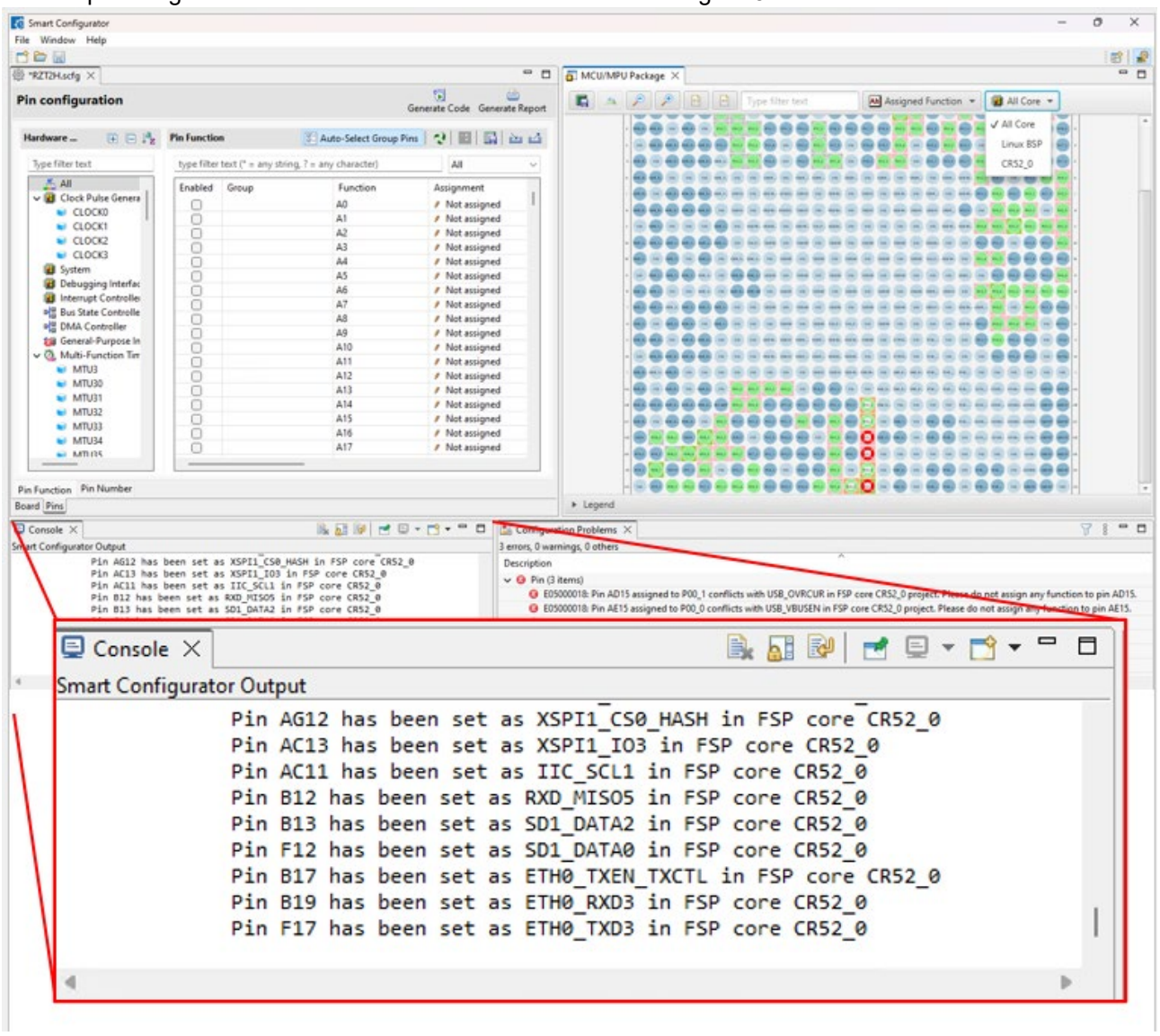

Figure 5. Checking for Contention between Pin Assignments: [Console] View

If pin assignments are in contention, the [Configuration Problems] view will display the corresponding error messages as shown at Figure 6.

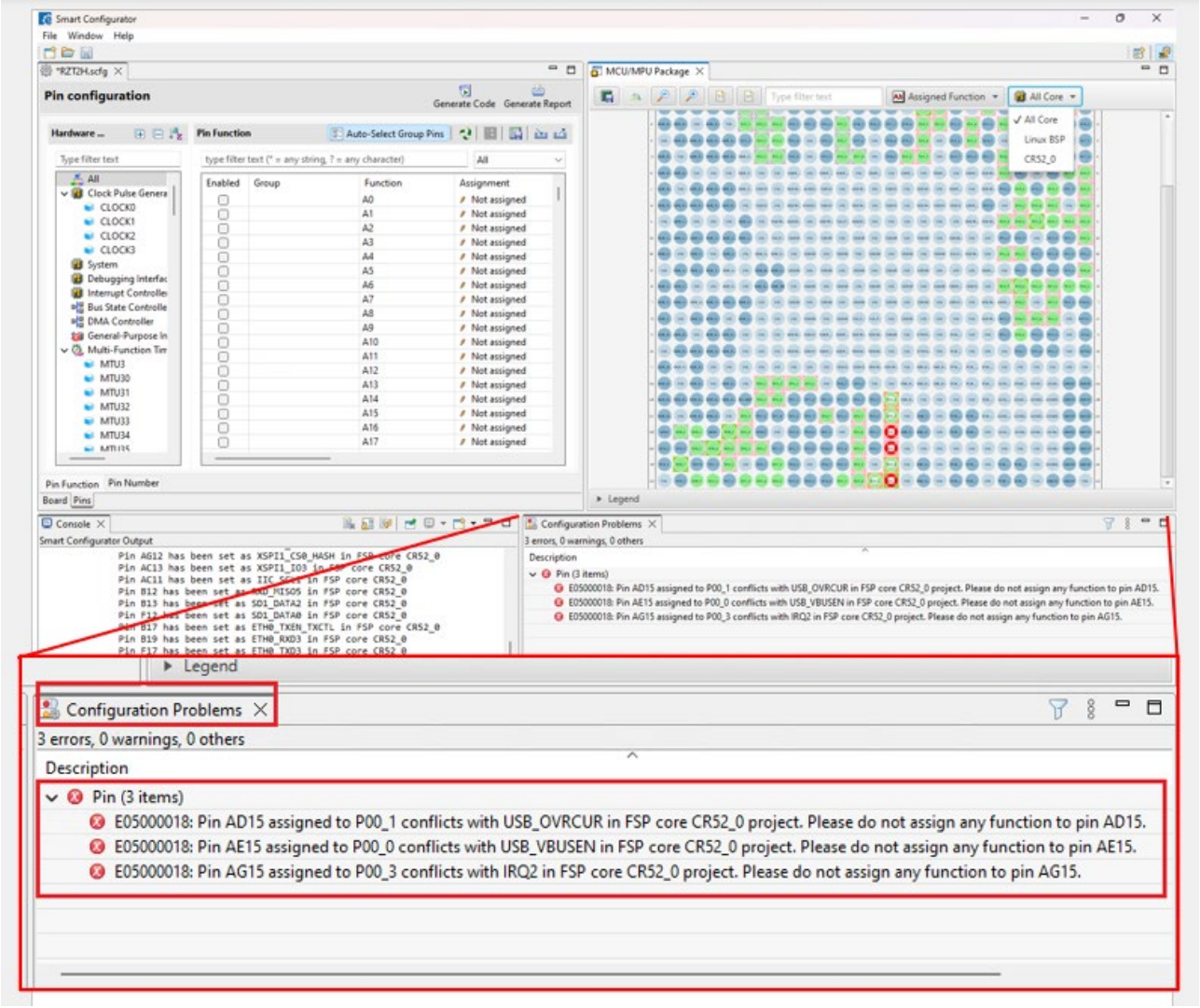

Figure 6. Checking for Contention between Pin Assignments: [Configuration Problems] View

The [MCU/MPU Package] view indicates pins for which usage is in contention. In Figure 7, selecting ‘All core’ shows pins in contention are displayed in red. In addition, pin assignments are displayed for each core. In Figure 7, selecting ‘Linux BSP’ shows the pin assignments set by the Smart Configurator for RZ and selecting CR52_0 shows pin assignments set by the FSP Smart Configurator.

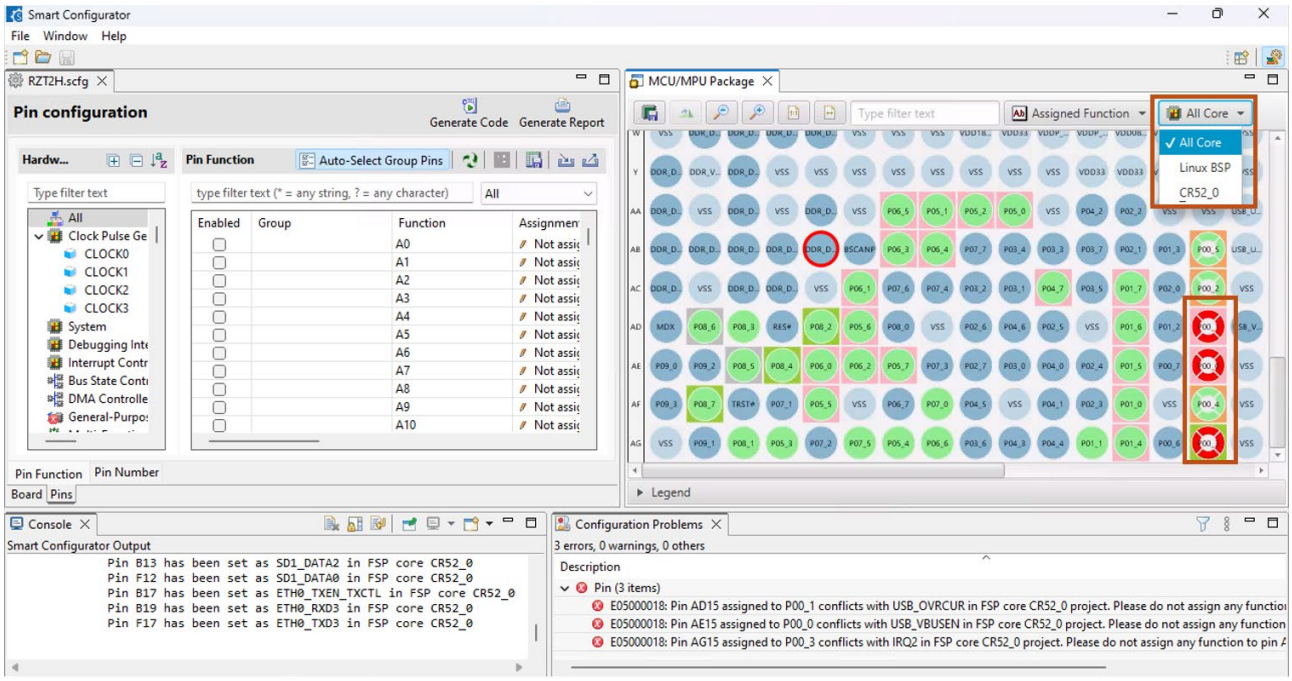

Figure 7. Checking for Contention between Pin Assignments: [MCU/MPU Package] View

If contention between pin assignments is confirmed, only the pin assignment of the Linux BSP can be changed Smart Configurator for RZ. If the pin assignment for other cores needs to be changed, you can do so in the FSP Smart Configurator.

Revision History

Rev.	Date	Description	
		Page	Summary
1.0	May.9.25	—	First Edition issued

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

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1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
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   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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